A 635pW Battery Voltage Supervisory Circuit for Miniature Sensor Nodes

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Abstract

We propose a low power battery voltage supervisory circuit for micro-scale sensor systems that provides power-on reset, brown-out detection, and recovery detection to prevent malfunction and battery damage. Ultra-low power is achieved using a 57pA, fast stabilizing two-stage voltage reference and an 81pA leakage-based oscillator and clocked comparator. The supervisor was fabricated in 180nm CMOS and integrated with a complete 1 mm^3 sensor system. It consumes 635pW at 3.6V supply voltage, which is an 850× reduction over the best prior work.

Introduction

A number of mm-scale sensor nodes were recently proposed for use in new embedded application areas, including medical, security, and resource exploration [1][2]. In general, mm-scale systems are equipped with a harvesting unit (e.g., solar cells [2]) to recharge their battery. They therefore require a *battery supervisory system* (BSS) to perform three critical functions (Fig. 1): 1) *Power on Reset* (PoR) detects power-on when the battery is initially connected and properly resets the sensor electronics; 2) *Brown Out Detection* (BOD) detects dangerously low battery voltages that can damage the battery or cause unpredictable circuit operation, upon which it disconnects the battery from the system; 3) *Recovery Detection* senses sufficient harvested voltage to reactivate system operation . A BSS is one of the few components in a sensor node that is continually connected to the battery. Given a total average power limit of a few nW for typical mm-scale systems, BSS current draw is therefore limited to <1nA to avoid dominating the overall power budget. While commercial PoR/BODs are widely available, they typically consume on the order of 0.1-1μA [3], motivating work on ultra-low power BSS designs to enable the emerging class of ultra-small sensor nodes.

This paper demonstrates a novel ultra-low power BSS implemented in 180nm CMOS. The BSS is integrated in a 1 mm^3-sensor system [2] and system functionality is shown with silicon measurements. The BSS controls the reset functionality of electronics on its own die as well as orchestrates the reset of other chips in the complete sensor system by modulating power supply voltages that are monitored by secondary reset detectors on those dies.

Proposed Circuit

A conventional BSS typically consists of a voltage reference, a battery voltage divider, a comparator, and a delay generator (Fig. 2). The comparator generates an internal compare signal when the divided battery voltage is lower than the reference voltage. The delay generator then adds a minimum delay before releasing the reset signal. This delay is needed to allow various circuits in the system to stabilize, such as voltage regulators, references, and clock generators. In addition, a controlled amount of hysteresis in the comparator is necessary to avoid oscillation.

Fig. 3 shows the circuit diagram of the proposed BSS. A leakage-based voltage reference using two different threshold voltages is used due to its low power consumption [4]. However, its original implementation employs a large decoupling capacitance to ground for noise purposes, leading to a large settling time of >7.4ms in nominal conditions, which is slower than the battery voltage divider. This introduces the risk that, with a fast rising battery voltage, the battery voltage divider exceeds the reference temporarily while the reference is stabilizing, causing a false reset release that could be fatal to system operation. Hence, we remove the decoupling capacitance and reduce gate length to decrease settling time. However, with the decoupling capacitance removed the reference output voltage becomes strongly coupled to the battery voltage, leading to the danger that a fast battery voltage drop will lower the reference voltage and suppress a valid triggering of reset. To reduce coupling to the battery voltage, we use a two-stage reference. A stacked *reference preconditioner* generates a supply voltage for the second reference stage. This decouples the reference from the battery voltage while the elimination of decoupling capacitance and reduced gate length ensure fast stabilization (<0.7ms) with a simulated total reference current draw of 57pA.

To reduce the power consumption of the battery voltage divider, it is implemented using a 23-transistor PMOS diode stack. By shorting out the top PMOS in response to the reset signal, the division ratio is changed from 11.5 to 11.0, introducing 220mV hysteresis [5]. Decoupling capacitance at the output reduces coupling to the battery voltage and ensures that V_{bat_div} rises slower than V_{ref} during a fast battery voltage ramp, preventing false reset release.

The two-stage comparator consists of a continuous comparator followed by a clocked comparator. The 1st stage uses a PMOS input stage to accommodate the relatively low V_{ref} of 0.3V. The bias voltage (V_{bias}), generated from the PTAT reference preconditioner, mitigates increased tail current at high temperature, reducing power consumption by 36% at 80°C (to 1.4nA). The second stage uses a clocked comparator driven by a 0.2Hz leakage-based oscillator to reduce power to 81pA (simulated), including the oscillator. The oscillator uses thyristor-based gain stages operating with leakage current [6]. Finally, since the clocked comparator and flip-flop trigger off opposite clock edges, a minimum reset delay of ½ the clock period is introduced (805ms). However, when the battery voltage drops below $V_{trigger}$, reset assertion is immediate.

A low battery voltage protector overrides the BSS at very low voltages to prevent comparator and flip-flop malfunction. This circuit consists of a chain of inverters and decoupling capacitors and uses transistor stacking and diodes to reduce static current to 6pA (simulated). The input of the inverter chain is connected to the 0.6V output of the reference preconditioner, resulting in the release of HOLD at a battery voltage of 1.1V, providing guardband to ensure correct BSS circuit operation.

The proposed BSS was implemented in the control processor of a 1 mm^3-sensor system, consisting of 5 stacked die layers: 1) solar cells and timer, 2) 1μAh thin-film Li battery, 3) DSP processor, 4) control processor and power management unit (PMU), and 5) radio and sensor interface. The BSS must reset and control the processor on its own layer as well as the electronics on other layers. Since the mm-scale form factor prevents additional reset signals from being wirebonded between the layers, the BSS instead overrides the PMU to send a reset "command" to the other dies. This is accomplished by disabling the 0.6V supply being output from the PMU while the 1.2V supply from the PMU remains enabled. Secondary reset detectors on the other layers detect this power condition and then reset their individual layers, as shown in Fig. 4.

Measurements

Fig. 5 shows measured operation of the BSS and the secondary reset detector in the complete sensor system as observed in silicon under several different battery voltage behaviors. Good control of the primary and secondary reset signal is seen in all cases. Fig. 6 shows measured $V_{release}$ and $V_{trigger}$ threshold voltages, and their hysteresis, across temperature with two different battery transition speeds (0.25mV/s and 0.8MV/s). Results from 15 dies show these threshold voltages as a function of battery transition speeds at 25°C and demonstrate tight spreads (< 2.3% σ/μ) and excellent immunity from coupling to the battery (< 20mV). Fig. 7 shows power-on reset delay as a function of final battery voltage and temperature, which is mainly determined by the period of the leakage-based oscillator. Fig. 8 gives the measured power consumption over 15 dies across temperature and battery voltage, and includes the power breakdown for each component based on simulation.

The die photo and comparison to recent work are shown in Fig. 9 and Table 1, respectively. The power on reset delay of the proposed BOD is longer than typical, which was required to allow the ultra-low power PMU of the mm3 sensor node to stabilize. The designed BSS consumes 850× lower power than prior art, enabling its use in general miniaturized battery-operated and harvesting-capable nodes with aggressive power budgets.

References

[1] E. Y. Chow *et al*., ISSCC, 2010, pp. 236-237.
[2] Y. Lee *et al*., ISSCC, 2012.
[3] TPS3836 Datasheet, Texas Instruments
[4] M. Seok *et al*., ESSCIRC, 2010, pp. 110-113.
[5] J. Guo *et al*., MWSCAS, 2010, pp. 21-24.
[6] M. Wieckowski *et al*., VLSI, 2009, pp. 166-167.
[7] H. Le *et al*., TCAS2, 2011, pp. 778-782.

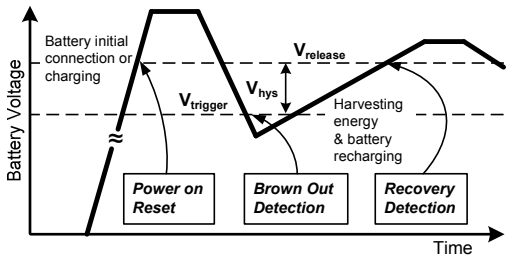

Figure 1. Varying battery voltage and required functions of battery supervisory system (BSS).

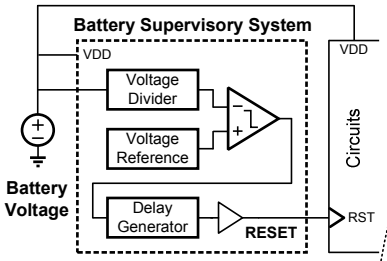

Figure 2. Conventional BSS circuit structure.

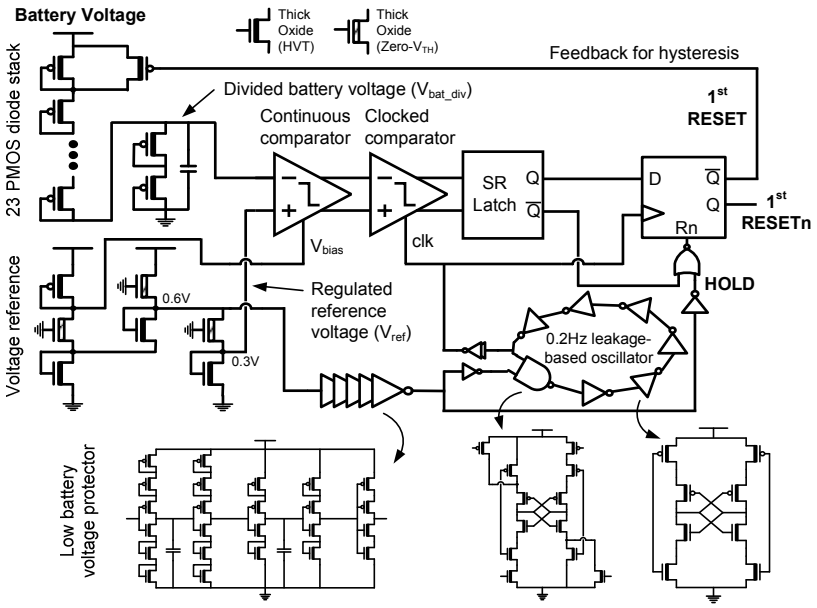

Figure 3. Proposed BSS circuit diagrams.

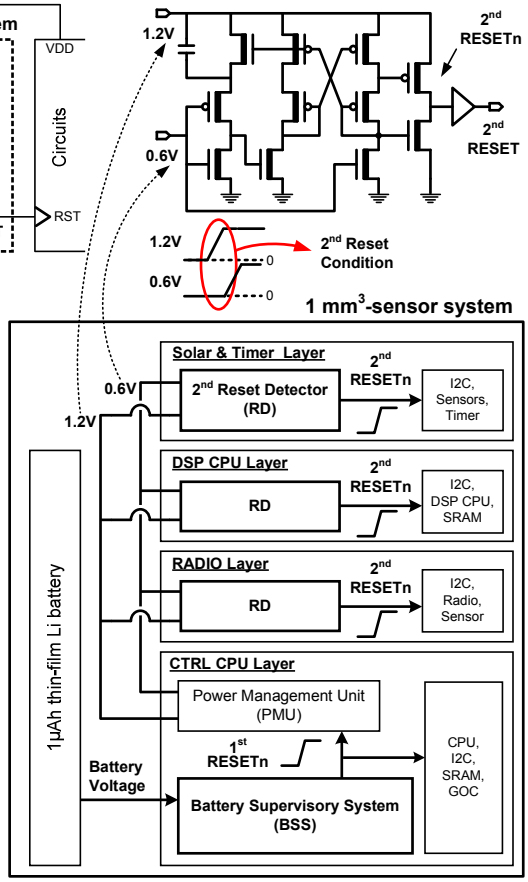

Figure 4. Reset propagation strategy to each layer in the mm³-scale sensor node.

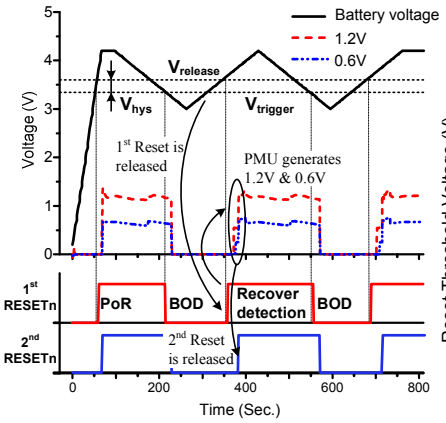

Figure 5. Measured operation of the BSS and secondary reset detector in a complete sensor system

Total 15 BSSs @ 25°C (V)

	0.25mV/s Battery Voltage Transition			0.8MV/s Battery Voltage Transition		
	Vrelease	Vtrigger	Vhys	Vrelease	Vtrigger	Vhys
µ	3.58	3.36	0.22	3.58	3.36	0.22
σ	0.081	0.066	0.032	0.080	0.064	0.033

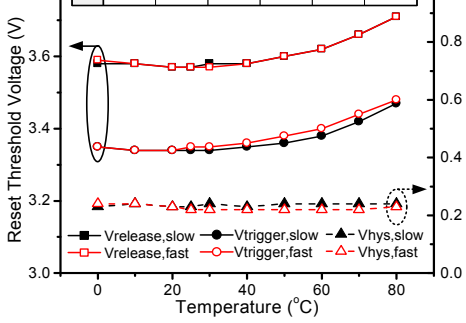

Figure 6. Measured reset threshold voltages and their hysteresis over temperature with two different battery transition speeds.

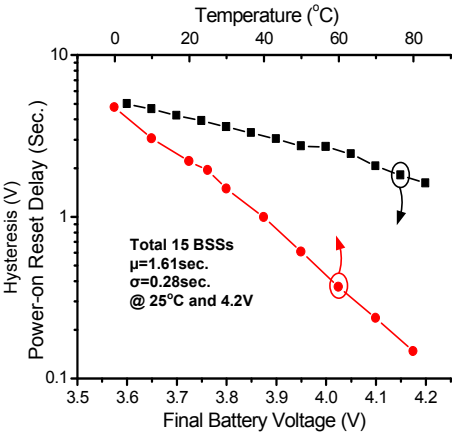

Figure 7. Measured power-on reset delay (Temperature sweep performed at 4.2V; voltage sweep performed at 25°C).

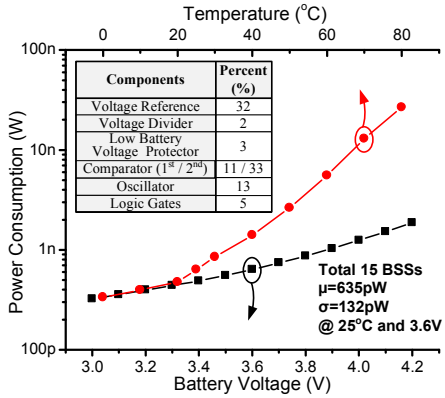

Figure 8. Measured power consumption and power breakdown (3.6V for temperature sweep and 25°C for voltage sweep).

CTRL CPU Layer in the mm³-scale sensor

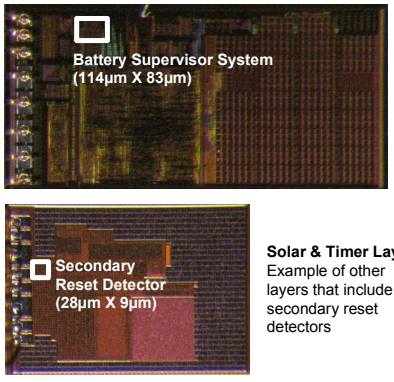

Figure 9. Die photo.

Table 1. Performance summary and comparison.

Parameters	This Work	[3]	[5]	[7]
Process	180nm	N/A	90nm	180nm
Supply	3.6V	3.6V	1.0V	1.8V
Power	635pW	900nW	540nW*	3.6µW*
Reset Delay	1.94 sec.	10ms /200ms	150ns	100ms
Hysteresis	200mV	40mV	432mV*	N/A
Comments	Lowest power consumption	Commercial Product	Power of voltage reference is not included.	Vrelease is not provided.

* Calculated for 3.6V supply voltage for comparison.