A Fully-Integrated 71 nW CMOS Temperature Sensor for Low Power Wireless Sensor Nodes

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***Abstract*—We propose a fully-integrated temperature sensor for battery-operated, ultra-low power microsystems. Sensor operation is based on temperature independent/dependent current sources that are used with oscillators and counters to generate a digital temperature code. A conventional approach to generate these currents is to drop a temperature sensitive voltage across a resistor. Since a large resistance is required to achieve nWs of power consumption with typical voltage levels (100 s of mV to 1 V), we introduce a new sensing element that outputs only 75 mV to save both power and area. The sensor is implemented in 0.18 μm CMOS and occupies 0.09 mm^2 while consuming 71 nW. After 2-point calibration, an inaccuracy of $+1.5^\circ\mathrm{C}/-1.4^\circ\mathrm{C}$ is achieved across 0°C to 100°C. With a conversion time of 30 ms, 0.3°C (rms) resolution is achieved. The sensor does not require any external references and consumes 2.2 nJ per conversion. The sensor is integrated into a wireless sensor node to demonstrate its operation at a system level.**

***Index Terms*—Fully integrated, subthreshold, temperature sensor, ultra-low power, wireless sensor node.**

I. Introduction

ULTRA-LOW power wireless microsystems are emerging as a new class of computing. These systems can be used in a wide range of application areas such as medical, surveillance, and environmental monitoring by equipping them with the appropriate sensors [1]–[3]. Among various sensor modalities, temperature is one of the most common and therefore low-power temperature sensors become an important design element of such microsystems.

The design of a temperature sensor for these miniaturized wireless microsystems poses several challenges, with many of the limitations arising due to a limited battery size and correspondingly small energy capacity. While average power consumption is critical as a result, the large internal resistance of the battery also limits the maximum instantaneous current that can be drawn from the battery. For example, the targeted thin-film Li battery has a limited maximum current draw of less than 20 μA [4]. Given that the temperature sensor power is only one component of total system power, this limitation is a major bottleneck. Further, the sensor should be fully-integrated and self-contained since accurate external references are not readily available in highly integrated microsystems.

Various types of temperature sensors have been designed in CMOS technology. Most conventional temperature sensors are based on bipolar junction transistors (BJTs). These sensors measure temperature by comparing a temperature-dependent voltage to a temperature-insensitive voltage. These two voltages are developed using two well-defined temperature characteristics of a vertical PNP transistor; 1) the complementary-to-absolute temperature (CTAT) characteristic of the base-emitter voltage ($\mathrm{V_{BE}}$) and 2) the proportional-to-absolute temperature (PTAT) characteristic of the difference between two base-emitter voltages ($\Delta\mathrm{V_{BE}}$). The ratio between the PTAT and reference voltages is fed to an analog-to-digital converter (ADC) to be digitized. With the choice of precision $\Sigma\Delta$-ADCs, these sensors offer high resolution, up to 0.002°C [5]–[7]. Sensing error in BJT-based sensors mainly arises due to process variation of the saturation current ($\mathrm{I_S}$) [8]. This error can be reduced to less than $\pm0.2^\circ$C after 1-point calibration. One example state-of-the-art temperature sensor achieves 0.02°C resolution with inaccuracy of $\pm0.15^\circ$C by combining two-step zoom ADC, chopping and dynamic element matching (DEM) [9]. However, such sensors show power consumption in μW range, making them unsuitable for miniaturized battery-powered applications.

As a result, MOSFET-based temperature sensors targeted for wireless system have been introduced. For low power operation, time-to-digital [10], [11] or frequency-to-digital conversion [12], [13] is used instead of ADCs. Temperature can be calculated using a reference clock and a temperature-dependent frequency or pulse. These sensors consume less power than BJT-based sensors at the expense of resolution and accuracy. While power consumption is reduced to hundreds of nW, an external clock is needed as a reference. The performance of these sensors highly depends on the accuracy of the reference clock, which is not typically available in a wireless microsystem. Moreover, the reference clock itself can increase power consumption significantly. On the other hand, a temperature sensor that uses an on-chip time reference while consuming sub-μW has been reported [14]. However, it exhibits larger inaccuracy compared to others due to the non-ideal characteristics of the reference clock. Recently, a temperature sensor based on dynamic threshold MOSTs (DTMOSTs) is introduced [15]. The sensor achieves high resolution (0.063°C) and accuracy ($\pm0.4^\circ$C) after single point trimming, but with sub-μW of power consumption (excluding clock generation power).

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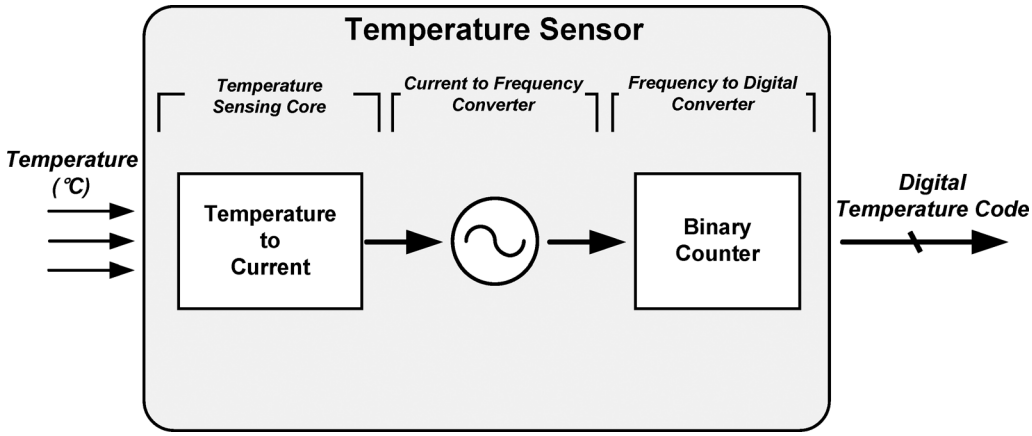


Fig. 1. Simplified block diagram of a proposed temperature sensor.

This work proposes a new temperature sensor topology that improves temperature inaccuracy while consuming very low power and energy. A novel MOSFET-based sensing element is introduced to translate external temperature into a voltage with pWs of power consumption. Furthermore, conventional voltage-to-current converter and current mirror structures are modified to reduce the required current consumption by half. With these techniques, the sensor consumes 71 nW of power and dissipates 2.2 nJ of energy per conversion with inaccuracy of $+1.5°\mathrm{C}/-1.4°\mathrm{C}$ and resolution of $0.3°\mathrm{C_{rms}}$ from 0 to 100°C temperature range.

The remainder of the paper is structured as follows. Section II introduces the proposed topology for the low power sensor with detailed description and analysis. Section III presents measured results of the test chip. Section IV demonstrates implementation of proposed sensor in an ultra-low power sensor node. Finally, Section V concludes the work.

II. Temperature Sensor Design and Analysis

Fig. 1 shows a block diagram of the proposed temperature sensor. The structure has three major components: 1) a temperature sensing core, 2) a current to frequency converter, and 3) a frequency to digital converter. The temperature sensing core converts temperature into a current. An oscillator is then used to convert this current into a frequency. Finally, a binary counter translates frequency into a digital output code. For temperature sensors that use a similar scheme, the total power consumption is dominated by the magnitude of current generated in the sensing core. This is because the generated current determines oscillator frequency, which directly relates to the counter dynamic power consumption. Therefore, generating a small current with well-defined temperature dependency is crucial to designing a low-power temperature sensor.

A. Temperature Sensing Element

Fig. 2 shows a conventional approach for generating a temperature-dependent current through a resistor ($\mathrm{I_R}$) using a voltage source ($\mathrm{V_{source}}$). In this structure, the output of a voltage source is copied across a resistor to generate a current. With this approach, either a very large resistor or very small voltage is required to achieve low power consumption. Using

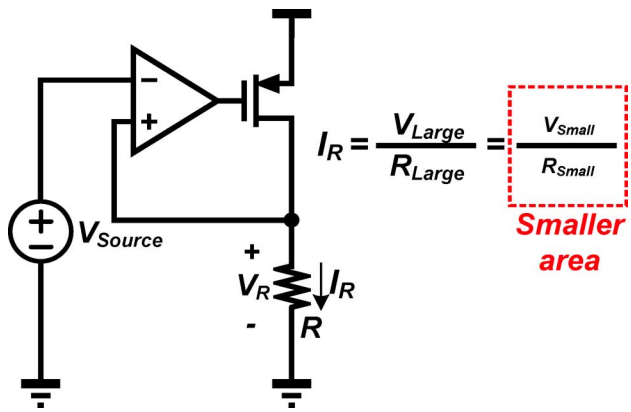


Fig. 2. Conventional voltage-to-current converter.

a typical bandgap voltage reference of ∼1V, a resistance of $>20\ \mathrm{M\Omega}$ is required to achieve sub-100 nW power consumption, which is impractical in area-constrained microsystems. To achieve nW range power consumption without incurring a large area penalty, we propose reducing $\mathrm{V_R}$ well below 100 mV by introducing a new sensing element (Fig. 3, right). The sensing element generates a linearly increasing output voltage with temperature while drawing only pA. A key component of the sensing element is based on a 2-Transistor (2T) voltage reference (Fig. 3, left) [16].

A prior implementation of the 2T voltage reference uses two different types of transistors (with highly disparate threshold voltages) to 1) increase the reference voltage as much as possible (>300 mV) and 2) compensate output voltage temperature dependence. By equating currents through $\mathrm{M_1}$ and $\mathrm{M_2}$, an analytical solution for the output voltage ($\mathrm{V_{Referece}}$) can be obtained as

$$V_{\mathrm{Reference}} = \frac{m_1 m_2}{m_1 + m_2}(V_{\mathrm{th2}} - V_{\mathrm{th1}}) + \frac{m_1 m_2}{m_1 + m_2} V_T ln\left(\frac{\mu_1 C_{\mathrm{ox1}} W_1 L_2}{\mu_2 C_{\mathrm{ox2}} W_2 L_1}\right) \quad (1)$$

where $\mathrm{V_{th}}$ is the threshold voltage, $\mathrm{V_T = kT/q}$ is the thermal voltage, m is the subthreshold swing coefficient, μ is mobility, and $\mathrm{C_{ox}}$ is gate oxide capacitance of the transistor [16]. From (1), it can be seen that compensation is achieved by combining

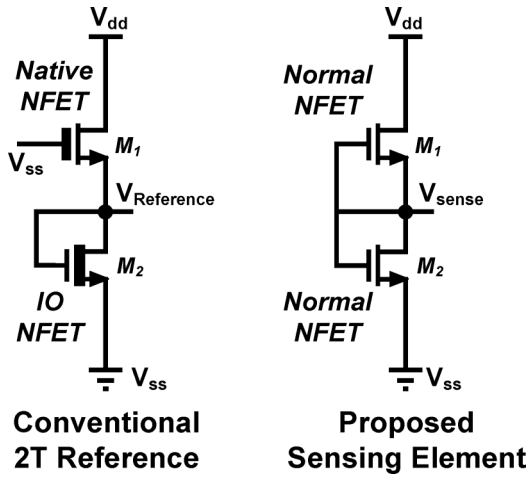


Fig. 3. Circuit diagram of a conventional 2T reference [16] and proposed sensing unit.

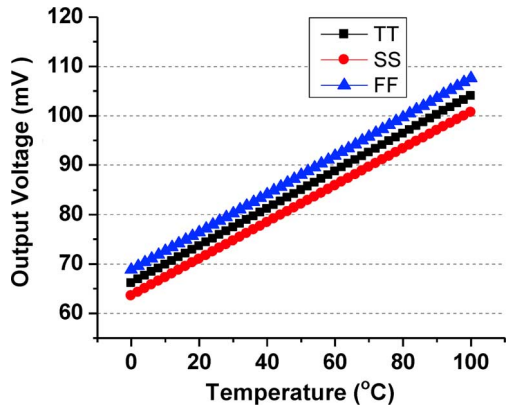


Fig. 4. Simulated output voltage of proposed sensing element.

the CTAT characteristic of the threshold voltage and PTAT characteristic of the thermal voltage. The reference output voltage can also be made PTAT or CTAT with proper sizing, which can be used to sense temperature. However, a high reference voltage increases power consumption. Furthermore, the use of different threshold transistors causes its output voltage to vary widely across process, resulting in degraded linearity and sensing error.

We therefore propose to use the same type of transistors for both devices in the 2T reference to eliminate the threshold voltage dependence in (1). The output voltage of the sensing element can be modeled using a subthreshold current equation that considers the body effect and DIBL [17] as follows:

$$I = \mu_0 C_{\rm ox}\left(\frac{W}{L}\right) V_T^2 e^{1.8} e^{\frac{-\Delta V_{\rm th}}{\eta V_T}} \times e^{(V_{\rm gs}-V_{\rm th}-\gamma' V_{\rm sb}+\eta V_{\rm ds})/mV_T} \times \left(1-e^{-V_{\rm ds}/V_T}\right) \quad (2)$$

where μ_0 is zero bias mobility, V_{th0} is zero bias threshold voltage, γ' is linearized body coefficient, η is the DIBL coefficient, and ΔV_{th} is a term introduced to account for transistor-to-transistor leakage variations. Assuming an output voltage greater than $3V_T$ ($\sim$75 mV), subthreshold current becomes independent of drain to source voltage (Vds). Also, DIBL becomes negligible due to the use of long channel devices. Therefore, current through each transistor M_1 and M_2 can be expressed as (3) and (4). The resulting output voltage can be found as (5) by equating I_1 and I_2, and V_{th1} and V_{th2}.

$$I_1 = \mu_1 C_{\rm ox1}\left(\frac{W_1}{L_1}\right) V_T^2 e^{1.8} e^{\frac{-\Delta V_{\rm th1}}{\eta V_T}} \times e^{(0-V_{\rm th1}-\gamma_1' V_{\rm sense})/m_1 V_T}. \quad (3)$$

$$I_2 = \mu_2 C_{\rm ox2}\left(\frac{W_2}{L_2}\right) V_T^2 e^{1.8} e^{\frac{-\Delta V_{\rm th2}}{\eta V_T}} \times e^{(V_{\rm sense}-V_{\rm th2}-\gamma_2' 0)/m_2 V_T}. \quad (4)$$

$$V_{\rm sense} = \frac{m_1 m_2}{m_1+\gamma_1' m_2} V_T \ln\left(\frac{\mu_1 C_{\rm ox1} W_1 L_2}{\mu_2 C_{\rm ox2} W_2 L_1}\right). \quad (5)$$

It can be seen that threshold voltage is eliminated and mobility is cancelled out. By eliminating these process/temperature dependent terms, low variability is achieved. As a result, the output voltage shows PTAT behavior with good linearity due to the thermal voltage V_T. Also, compared to the conventional structure, higher temperature sensitivity is achieved by connecting the gate of top transistor (M_1) to the output ($m_2 > (m_1 m_2)/(m_1+m_2)$, when $\gamma' = 0$). Fig. 4 shows simulation results of this 2T sensing element at different corners. The minimum R^2 correlation of the output voltage is 0.99995, observed at the fast corner. The sensing element output voltage is also greatly reduced by removing the threshold voltage term. Additionally, devices are sized with similar gate lengths to avoid threshold voltage discrepancies due to reverse short channel effect. The sensing element consumes 8 pW at room temperature and shows a supply dependency of 1.814%/V from 1.0 V to 1.4 V in simulation.

Fig. 5 compares a conventional 2T structure with the proposed structure. Conventional 2T is sized to match the slope of sensing element in the typical corner. Monte Carlo simulations show that the proposed structure has $5\times$ lower output voltage, enabling a $5\times$ reduction in resistor area for equivalent current. Also, the proposed topology exhibits $2.8\times$ lower output voltage variation (σ/μ) and $2.2\times$ less variation in slope (temperature coefficient, or TC, variation). Output voltage process dependency and TC variation are important factors since they directly impact the temperature characteristics of the generated current.

B. Current Generation

For current generation, we first begin with a conventional structure shown in Fig. 6(a). In this structure, the sensing element drives a conventional voltage to current converter to generate currents. A negative feedback loop consisting of an amplifier, transistor, and resistor duplicates the sensing element's output voltage across the resistor. The amplifier operates in the subthreshold region to achieve power savings. Using a 2-stage topology, the amplifier shows 105 dB open-loop gain and 136 pW of power consumption at room temperature (simulated results). The high gain of the amplifier ensures that V_R tracks V_{sense}. Due to the negligible power consumption of the sensing element and amplifier, temperature sensing core power is dominated by I_R (nA range). Conventionally, a current mirror (M_{1-2}) is required to provide control voltages (V_H and

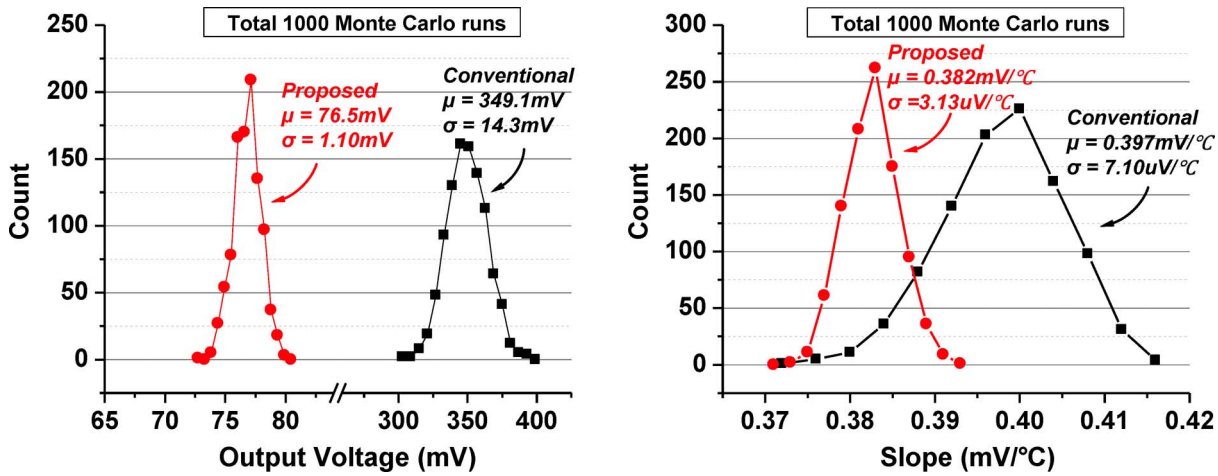


Fig. 5. Simulated output voltage and slope distribution of conventional 2T ($\mathrm{W_{top}/L_{top}} = 50\,\mu\mathrm{m}/4.5\,\mu\mathrm{m}$, $\mathrm{W_{bot}/L_{bot}} = 1\,\mu\mathrm{m}/6\mu\,\mathrm{m}$) and proposed structure ($\mathrm{W_{top}/L_{top}} = 40\,\mu\mathrm{m}/5\,\mu\mathrm{m}$, $\mathrm{W_{bot}/L_{bot}} = 1\,\mu\mathrm{m}/5\,\mu\mathrm{m}$).

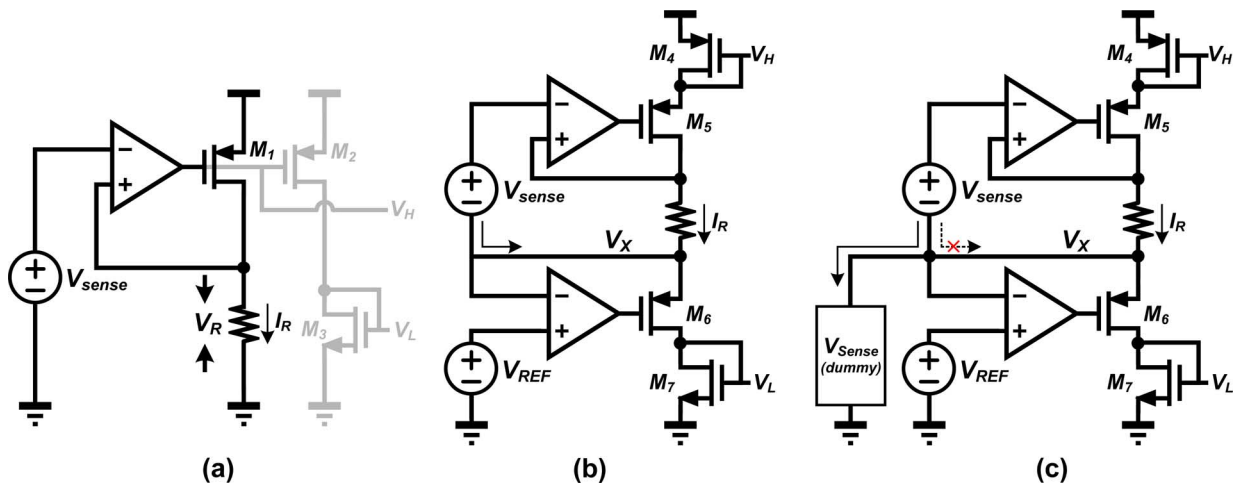


Fig. 6. Circuit diagram for (a) conventional scheme for current generation with a voltage source, (b) modified structure for low-power operation and (c) additional current path added for error reduction.

$\mathrm{V_L}$) for the subsequent ring oscillators; however, 50% power savings can be achieved by avoiding such a current mirror.

Thus, we introduce a second feedback loop along with a reference generator ($\mathrm{V_{REF}}$) to remove the current mirror (Fig. 6(b)). The additional feedback loop allows for the inclusion of a diode-connected transistor $\mathrm{M_7}$ at the bottom of the stack. This structure ensures $\mathrm{M_7}$ is saturated; otherwise, it becomes cutoff due to the sub-100 mV output voltage from the sensing element. As a result, $\mathrm{V_H}$ and $\mathrm{V_L}$ are generated directly from $\mathrm{I_R}$ without an additional mirror. The control voltages are generated from $\mathrm{M_4}$ and $\mathrm{M_7}$ rather than from $\mathrm{M_5}$ and $\mathrm{M_6}$ to avoid large loading on the op-amp outputs. This enhances bandwidth and phase margin of the op-amps, and also relaxes the output swing by biasing the output away from the supply rails. The reference generator is made with diode-connected PMOS transistors. It draws 240 pA and outputs an intermediate voltage between supply and ground. This structure also helps to obtain an effective common-mode voltage of the amplifier by boosting the sensing element's output voltage by $\mathrm{V_{DD}}/2$. Meanwhile, the voltage dropped across the resistor is maintained, helping to protect $\mathrm{I_R}$ against supply variation regardless of the reference generator, which has poor supply regulation. Simulated line sensitivity shows that current changes by 0.974%/V in the 1.0–1.4 V range.

However, by connecting the sensing element's ground to $\mathrm{V_x}$, the current flowing through the sensing element moves along the path and is added to $\mathrm{I_R}$. This causes a discrepancy between top and bottom current of the diode-connected devices, which creates error in subsequent stages. To eliminate this problem, a duplicate sensing element that serves as a dummy structure is connected between $\mathrm{V_x}$ and ground (Fig. 6(c)). Since each element operates over the same voltage range ($\mathrm{V_{DD}}/2$), current flowing through the main sensing element is identical to current through the dummy sensing element. As a result, the dummy sensing element functions as a leakage path for the main sensing element, suppressing unwanted current in the main current generation path.

Fig. 7 shows the detailed schematic of the temperature sensing core. A temperature insensitive reference current ($\mathrm{I_{REF}}$) and temperature sensitive PTAT current ($\mathrm{I_{PTAT}}$) are generated from two sets of the previously described structure. Each current is generated using different types of resistors along with different sensing elements. Proper resistor choice for these

currents is performed by first characterizing $V_{\rm sense}$ and resistance (R) against temperature. Due to the linear temperature characteristic of the sensing element, only its first-order temperature dependency has been considered, while both first- and second- order dependencies have been considered in modeling resistance. Thus, $V_{\rm sense}$ and R can be expressed as follows:

$$V_{\rm sense} = V_o(1 + \alpha_{V1}T). \quad (6)$$

$$R = R_o(1 + \alpha_{R1}T + \alpha_{R2}T^2). \quad (7)$$

As a result, the generated current I_R can be modeled by (8)–(10).

$$I_R = \frac{V_{\rm sense}}{R} = \frac{V_o(1+\alpha_{V1}T)}{R_o(1+\alpha_{R1}T+\alpha_{R2}T^2)} = \frac{V_o}{R_o}(1+\alpha_{I1}T+\alpha_{I2}T^2) = I_0(1+\alpha_{I1}T+\alpha_{I2}T^2). \quad (8)$$

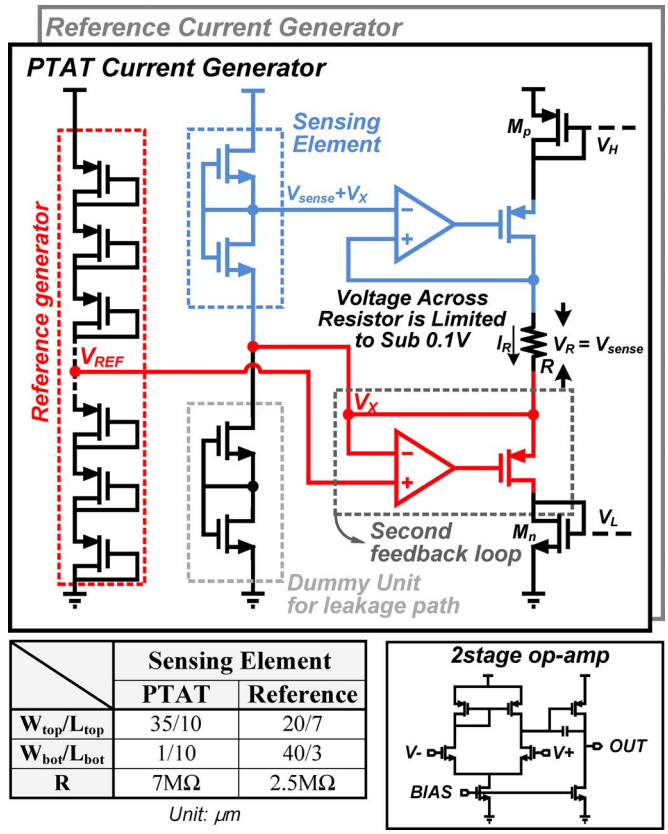
$$\alpha_{I1} = \alpha_{V1} - \alpha_{R1}. \quad (9)$$

$$\alpha_{I2} = \alpha_{R1}^2 - \alpha_{R1}\alpha_{V1} - \alpha_{R2}. \quad (10)$$

Since the sensing element itself has a positive first order temperature coefficient (α_{V1}), a PTAT resistance that has a positive first order temperature coefficient (α_{R1}) is required to generate the I_{REF}. With proper sizing of the sensing element, α_{V1} can be matched to α_{R1} to set α_{I1} to zero. On the other hand, a resistor with a CTAT characteristic is desired for the temperature sensitive I_{PTAT} in order to increase the temperature dependency. Increased temperature dependency translates into a wider range of digital codes and hence finer resolution. In the chosen process, diffusion resistors and poly resistors meet the above requirements for I_{REF} and I_{PTAT}, respectively. Among diffusion resistors, n+ type is chosen to minimize the second order temperature coefficient α_{I2} due to its $1.8\times$ lower α_{R2} compared to p+ type. Resulting design parameters for the I_{REF} are $\alpha_{I2} = 6.26\times 10^{-7}/°C^2$ and $\alpha_{I1} = -7.61 \times 10^{-5}/°C$. Among poly resistors, p^+ type results in a $1.1\times$ better α_{I2} compared to p^- type. However, p^- type is chosen due to its area efficiency ($3.1\times$ less area for iso-resistance) and $1.2\times$ higher α_{I1}. Resulting design parameters for the I_{PTAT} are $\alpha_{I2} = 4.00 \times 10^{-6}/°C^2$ and $\alpha_{I1} = 6.58 \times 10^{-3}/°C$.

In very low power applications, a diffusion resistor must be considered carefully due to its leakage. Fig. 8 shows the structure of an n^+ diffusion resistor. A reverse-biased junction diode is formed between n^+ diffusion and p-substrate. As temperature increases, leakage current through this diode increases exponentially and cannot be neglected. When the lower end of the diffusion resistor is biased at 600 mV, simulated results show that the linearity of the resistance is degraded when the amount of current flowing across a resistor decreases sufficiently towards the leakage current value. In this work, lower bound on reference current is set as 3 nA in order to maintain low temperature sensitivity in the targeted temperature range of 0°C to 100°C.

Although the sensing element is carefully sized to match its first order temperature coefficient with the resistor, temperature dependency of the amplifier gain will cause a discrepancy between $V_{\rm sense}$ and V_R. To remove this problem, amplifier gain is designed to exceed 98 dB across the targeted temperature range, which leads to TC variation below 0.01%. Another source of error comes from non-idealities due to process variation and mismatch. Process variation causes α_{R1} to vary while offset of the amplifier makes α_{V1} to deviate from a designed value. Also, mismatch between the main and dummy sensing element can result in an error in the generated currents. Among these factors, op-amp offset is the dominant source of error as it directly affects reference current stability ($\alpha_{I1} \neq 0$). PTAT current α_{I1} also deviates from its designed value but can be tolerated using 2-point calibration as its linearity is preserved. In contrast, error due to spread of α_{R1} is not critical as their values are nearly constant with process variation in simulation (<0.25% over 3σ corners). Sensing element mismatch is also negligible due to 1) large device sizes and 2) small current level compared to I_{PTAT} and I_{REF} (<0.33%). To minimize these errors, large devices and wide resistor widths are used at the expense of area. Fig. 9 shows the effects of process variation and mismatch on I_{PTAT} and I_{REF} from 1000 Monte Carlo simulations. The calculated resulting average error due to non-linearity is 0.3°C with 11% area overhead due to device and resistor sizing.



	Sensing Element	
	PTAT	Reference
W_{top}/L_{top}	35/10	20/7
W_{bot}/L_{bot}	1/10	40/3
R	7MΩ	2.5MΩ

Unit: μm

Fig. 7. Detailed schematic of temperature sensing core.

C. Ring Oscillators

The voltage-controlled ring oscillator shown in Fig. 10 is used to translate current into frequency. A single stage of an oscillator consists of an inverter followed by a transmission gate (TG). To reduce idle state power consumption, the first stage employs a NAND gate to prevent unnecessary oscillation. Oscillator frequencies are controlled by adjusting the resistance of transmission gates (R_{TG}) with voltages (V_H and V_L) from the previous

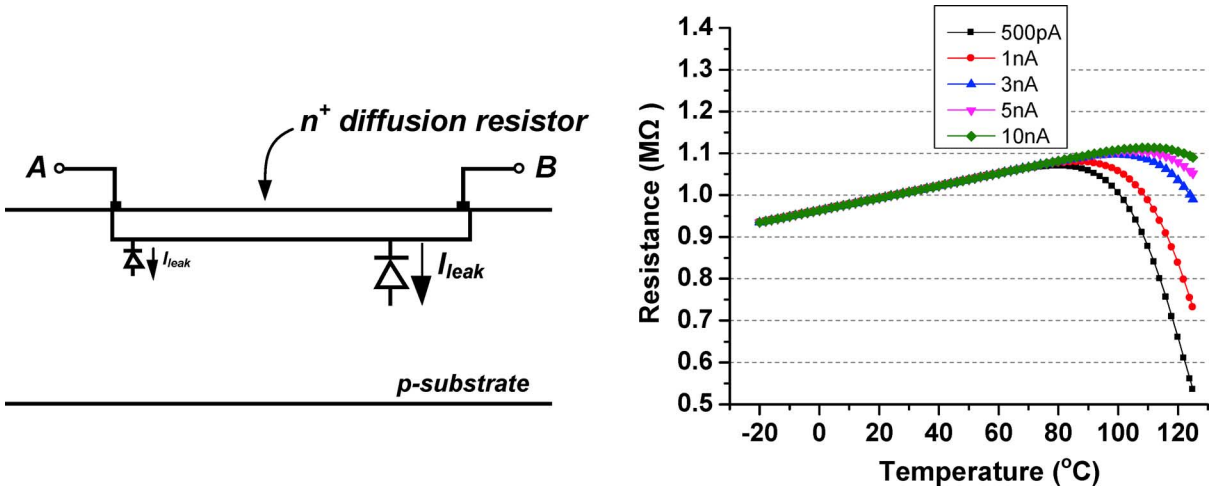


Fig. 8. Structure of an n^+ diffusion resistor (W = 840 nm, L = 15.2 mm) and simulated resistance across different amounts of bias current.

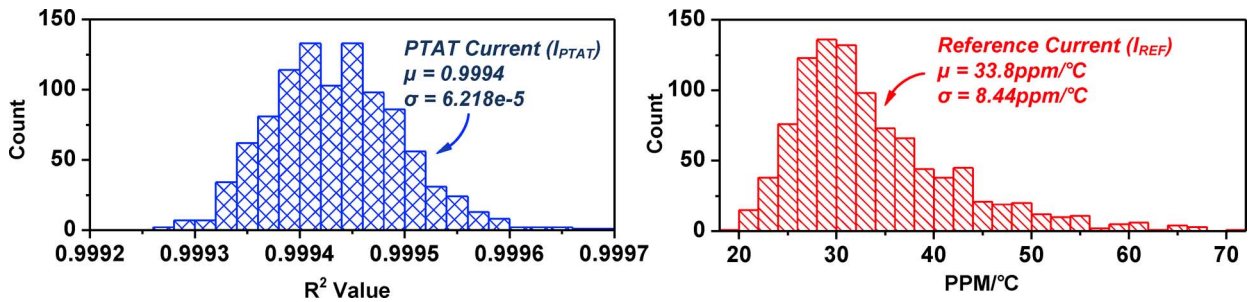


Fig. 9. Effect of process variation and mismatch on PTAT linearity (left) and reference temperature coefficient (right).

stage. Using a simple RC model, the delay of each stage t_d can be expressed as [18],

$$t_d = \frac{C_G(1 + g_M R_{\mathrm{TG}})}{g_M} \tag{11}$$

where g_M is the transconductance of a single inverter and C_G is the total gate capacitance of a stage (including both NMOS and PMOS). It can be seen that for $g_M R_{\mathrm{TG}} \gg 1$, each stage delay will be determined by R_{TG}, rendering inverter delay temperature dependence negligible.

Effective resistance of R_{TG} is an average value of $V_{\mathrm{TG}}/I_{\mathrm{TG}}$ during transition, where V_{TG} and I_{TG} are voltage and current across a transmission gate, respectively. Given a step response of a rising input and $V_{\mathrm{DD}}/2$ as a switching point, I_{TG} will remain same during transition as $V_{\mathrm{ds}}(= V_{\mathrm{DD}}/2)$ is kept above $3V_{\mathrm{T}}$. In this case, effective resistance for a falling transition can be approximated as follows [19]:

$$R_{\mathrm{TG,effective}} = \frac{ln2}{V_{\mathrm{DD}}/2} \int_{V_{\mathrm{DD}}/2}^{V_{\mathrm{DD}}} \frac{V}{I_{\mathrm{TG}}} dV \approx \frac{V_{\mathrm{DD}}}{2I_{\mathrm{TG}}}. \tag{12}$$

Similar discussion also holds for a rising transition. From (11) and (12), the oscillation frequency f_{osc} of an N-stage oscillator can be expressed as:

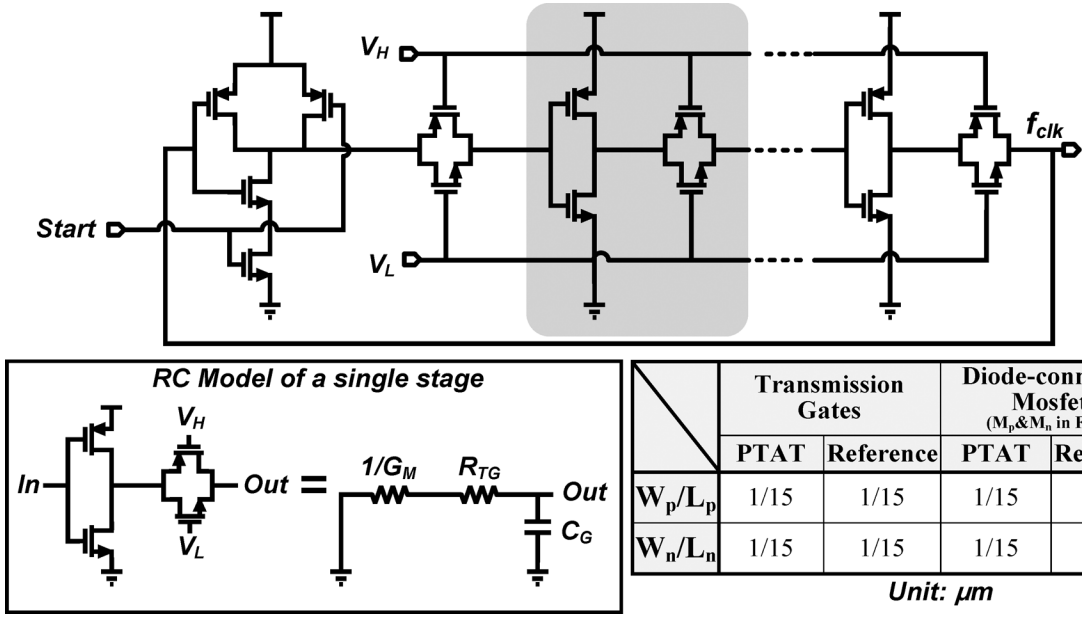
$$f_{\mathrm{osc}} = \frac{1}{2Nt_d} = \frac{g_M}{2NC_G(1 + g_M R_{\mathrm{TG}})} \approx \frac{I_{\mathrm{TG}}}{NC_G V_{\mathrm{DD}}}, (g_M R_{\mathrm{TG}} \gg 1). \tag{13}$$

Since I_{TG} tracks the current generated from the sensing core through V_{H} and V_{L}, frequency will be determined by I_{REF} and I_{PTAT}. As a result, the two ring oscillators generate a PTAT frequency $(\mathrm{clk_{PTAT}})$ and reference frequency $(\mathrm{clk_{REF}})$.

For the $g_M R_{\mathrm{TG}} \gg 1$ condition, inverters are designed with large width devices for fast transitions while I/O devices are used to minimize short-circuit current. This also increases capacitance seen by the previous transmission gate and enhances the delay difference between inverter and transmission gate in each stage at the expense of power consumption. The inverter delay is set to be less than 5% of the total stage delay.

Although the temperature dependency of the frequency is controlled by the current from the sensing core, the frequency is sensitive to supply variation as shown in (13). Supply dependence of R_{TG} causes its value to increase as supply voltage increases, decreasing frequency. Since both $\mathrm{clk_{PTAT}}$ and $\mathrm{clk_{REF}}$ show the same behavior due to their identical structure, this effect is partially suppressed, however different bias condition leave some residual error. The simulated supply sensitivity is $+1.7°\mathrm{C}/-2.8°\mathrm{C}$ across 1 to 1.4 V range.

Process variation and mismatch make it difficult to accurately match the small current flowing through a resistor to a current flowing through transmission gates, degrading the temperature characteristics of the oscillator. Such degradation is especially critical for the reference frequency. While PTAT frequency maintains linearity despite slope changes, the temperature insensitivity of the reference frequency is not preserved with large mismatch and process variation. Digital



	Transmission Gates		Diode-connected Mosfets (M_p&M_n in Fig. 7)	
	PTAT	Reference	PTAT	Reference
W_p/L_p	1/15	1/15	1/15	1/15
W_n/L_n	1/15	1/15	1/15	1/15

Unit: μm

Fig. 10. Circuit diagram of a voltage controlled ring oscillator.

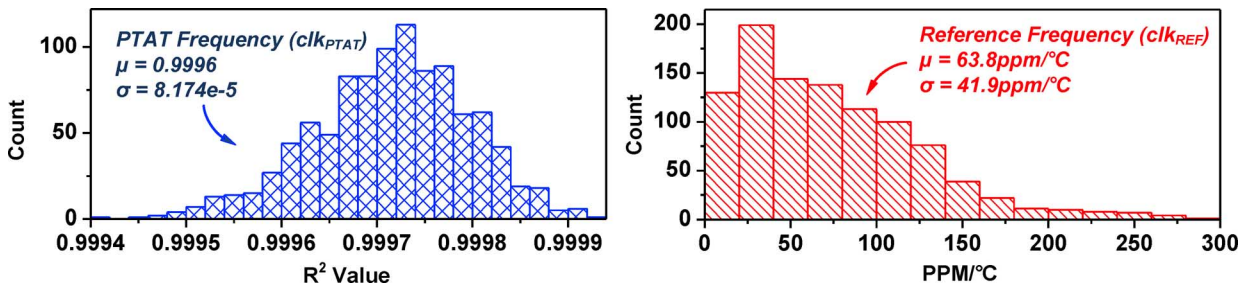


Fig. 11. Monte Carlo simulation results of PTAT and reference frequency.

output linearity is directly affected by this temperature dependency. Thus, careful layout of large devices is used to improve matching. Devices are sized with long lengths and small width to minimize kickback noise and V_{ds} mismatch due to DIBL. Fig. 11 shows 1000 Monte Carlo simulations of the ring oscillators with the temperature sensing core. When compared with Monte Carlo current simulations, PTAT frequency linearity is preserved while the mean temperature sensitivity for the reference frequency worsens by $1.9\times$. Therefore, most error arises from reference current to frequency conversion while op-amp offset (mentioned in Section II-B) becomes the next largest component.

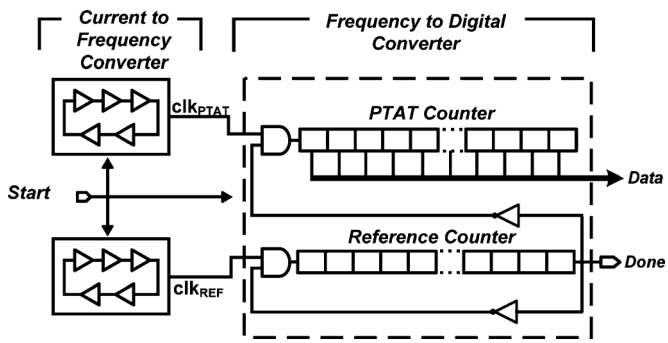


Fig. 12. Block diagram of a frequency to digital converter.

D. Counters

Generated frequencies are converted into a digital output through asynchronous counters. Fig. 12 shows the block diagram; PTAT and reference frequency are connected to the first stage of PTAT and reference counters, respectively. The reference counter consists of 9 bits whereas PTAT counter has 15 bits. The PTAT counter size is chosen such that it will not overflow, especially at high temperature where PTAT frequency is at its maximum. Adding more bits to the PTAT counter increases static power linearly with little impact on dynamic power since MSB switching activity is very low. Flip-flops use I/O devices to minimize leakage and short circuit current during transitions. As a result, the leakage current of a single flip-flop is measured to be 112 fA at room temperature.

When *Start* signal is triggered, the oscillators start running and both counters begin counting upward. Both counters stop when the reference counter saturates and the *Done* signal is set. At the same time, the digital code is read from the PTAT counter. The counter is reset by the *Start* signal. Conversion time is tunable by selecting the size of the reference counter (6 to 9 bits).

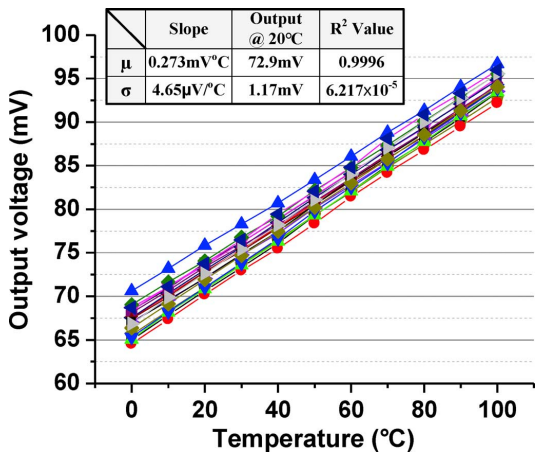


Fig. 13. Measured output voltage of sensing element.

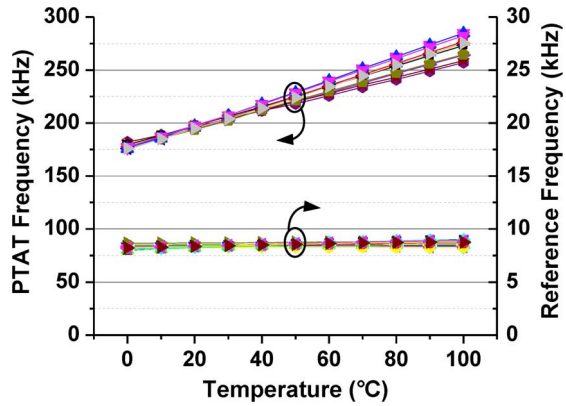


Fig. 14. Measured PTAT and Reference Frequency.

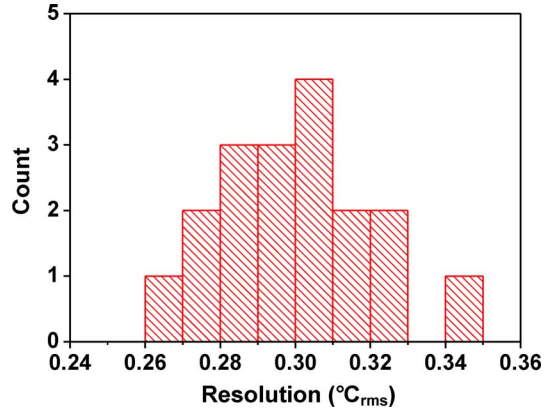


Fig. 15. Measured resolution of temperature sensor.

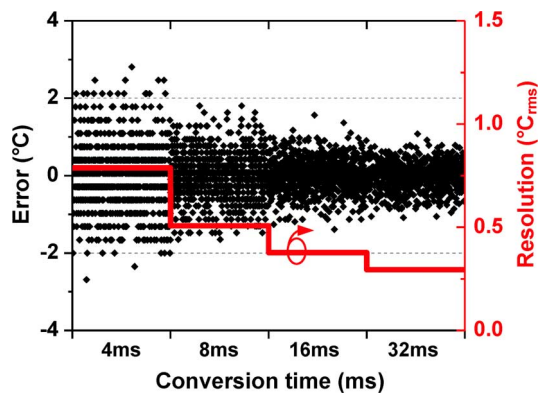


Fig. 16. Measured temperature uncertainty depending on conversion time.

E. Noise Analysis

Noise simulation of the sensor shows 0.26° C_{rms} of error at room temperature and the dominant noise source ($\sim 80\%$) is thermal noise of the op-amps in the temperature sensing core due to their low current consumption. Therefore, to further improve noise performance, op-amp tail current should be increased. Once op-amp thermal noise is decreased (at the expense of power), thermal noise in the sensing element and reference generator becomes the next dominant source of noise. This noise can be decreased by adding capacitors, slowing response time. The next dominant source of noise is flicker noise in the op-amps. Such low frequency noise can be reduced by implementing auto-zeroing or chopping. However, care must be taken with these techniques due to the extremely small current flowing through the sensing element. The addition of MOSFET switches introduces subthreshold and body leakage which degrade the temperature characteristics of the sensing element. Also, clock feedthrough and charge injection will require additional stabilization time for the sensing element.

III. Measurement Results

The proposed temperature sensor is fabricated in 0.18 μm CMOS in 0.09 mm^2. Measurements were made on 18 dies, taken from four different wafers in two different lots to observe the effect of process variation. Measured sensing element output voltage is given in Fig. 13. The proposed circuit generates a process-independent slope and output value while maintaining good linearity. Average sensing element power consumption is measured to be only 10 pW. Measured average PTAT frequency ranges from 176 kHz to 275 kHz, leading to a resolution of 0.04 °C/LSB with the 8-bit reference counter running at 8.4 kHz (Fig. 14). However, the effective resolution of the sensor is thermal noise-limited. Fig. 15 shows measured rms resolution across different chips at a conversion rate of 32.8 samples/sec; average resolution is measured as 0.3 °C_{rms}. Resolution can be improved by using a longer conversion time at the expense of energy. Fig. 16 shows measured temperature uncertainty with different conversion times. It can be seen that rms error decreases as conversion time increases since high frequency noise is averaged out.

Supply sensitivity of the sensor is measured to be $+2.5/-3.15\,^\circ$C from 1.0–1.4 V supply variations (Fig. 17). The complete sensor consumes 54 nA at room temperature with supply voltage of 1.2 V (59 nA average across the 18 dies). Fig. 18 provides the overall power breakdown and shows that the ring oscillator is the largest component. Fig. 19 gives the measured temperature sensor inaccuracy over 18 different test chips. After 1-point calibration at 50°C, the measured error is $+3.7^\circ$ C/-4.5°C across 0 to 100°C. However, the measured

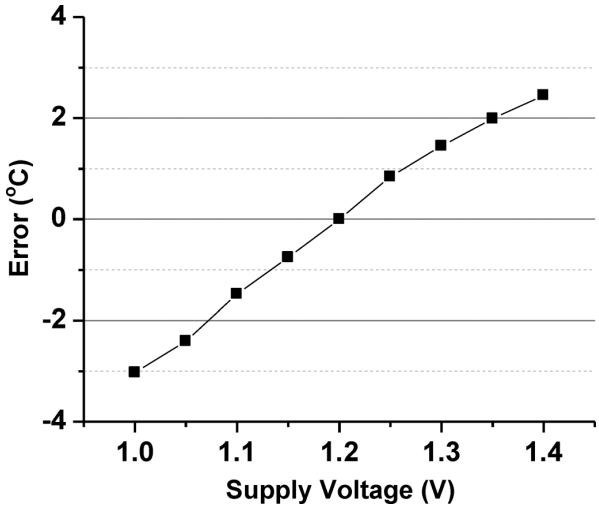


Fig. 17. Measured supply sensitivity of the sensor at 25° C.

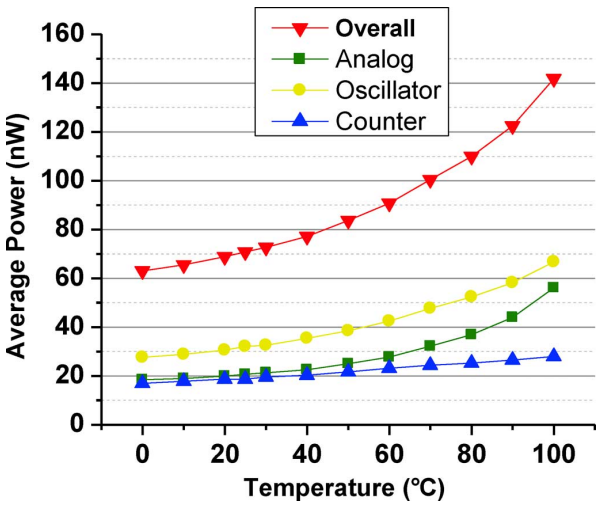


Fig. 18. Measured average power of the temperature sensor and corresponding breakdown by component.

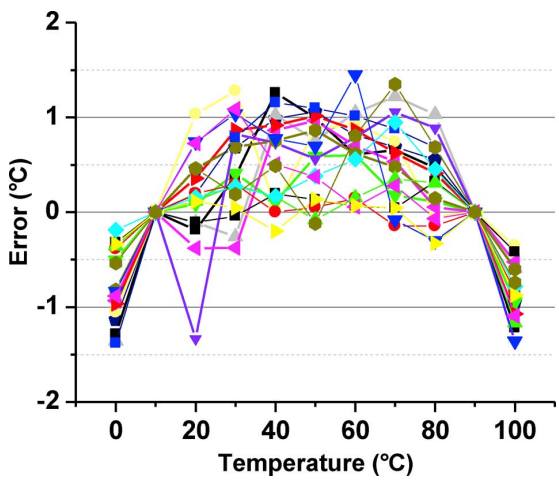


Fig. 19. Measured temperature error over 18 samples.

error is reduced to $+1.5°$ C/$-1.4°$C after 2-point calibration at 10°C and 90°C.

The test chip die photo is shown in Fig. 20. The two resistors occupy 42% of the total area. Table I compares the design with other low-power temperature sensors. The sensors that consumes less than 10 μw and 100 nJ/conversion are highlighted for its possible usage in sensor nodes. The proposed design shows significantly better energy per conversion and relative inaccuracy compared to our previous fully-integrated tem-

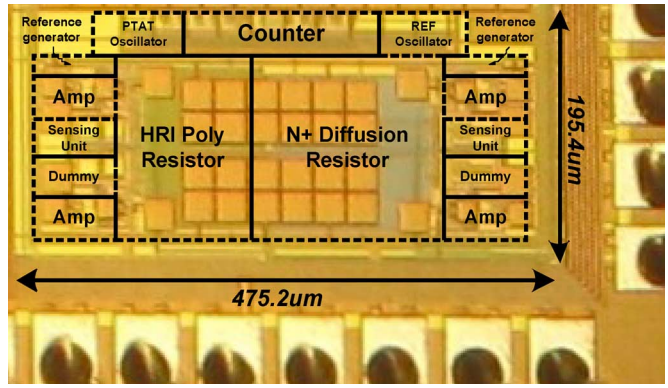
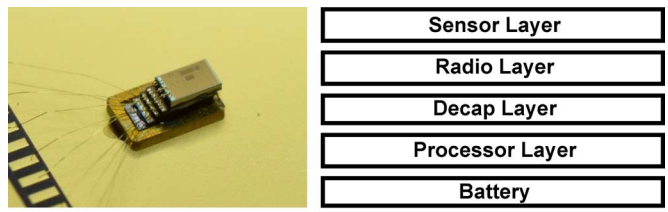


Fig. 20. Die photo of the proposed sensor in 0.18 μm CMOS.



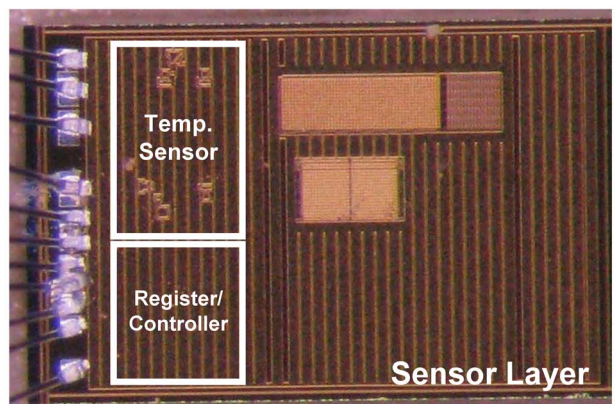


Fig. 21. Photo of a stacked system with proposed temperature sensor in a sensor layer (top left). Bottom shows a die photo in 0.18 μm CMOS of the sensor layer.

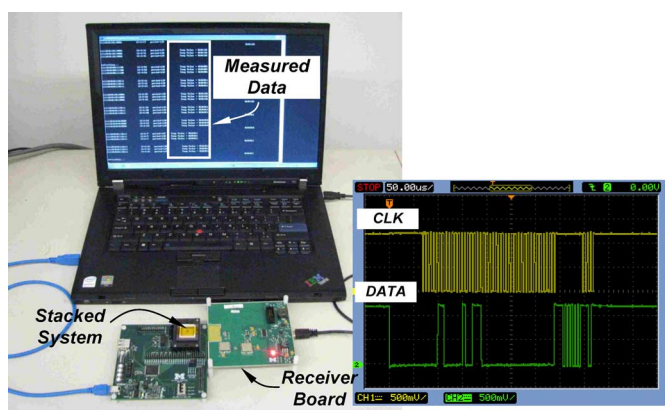


Fig. 22. Testing setup for the stacked system (Fig. 21, top left) and measured waveform.

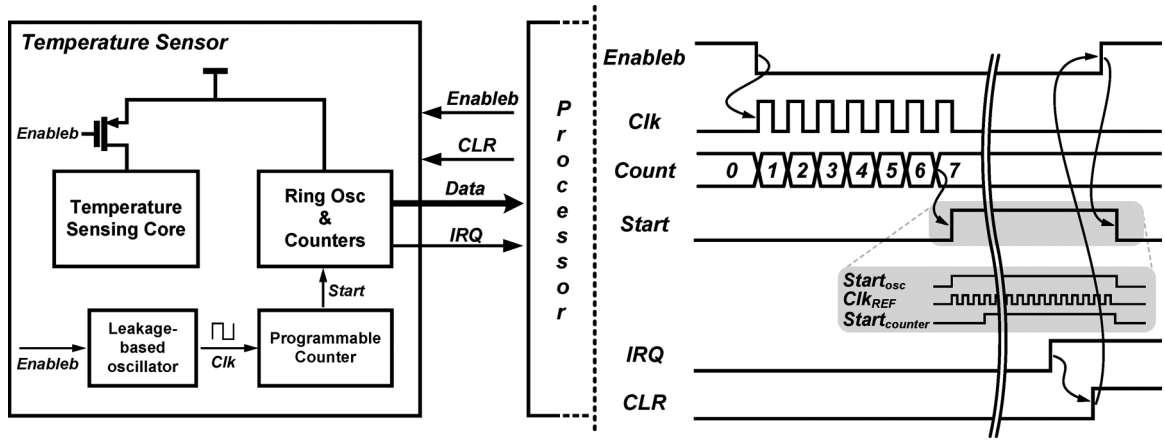


Fig. 23. Block diagram of a temperature sensor in the system and its timing diagram.

perature sensor [14]. The sensor consumes the lowest power even when compared to other MOSFET-based designs that use high accuracy external clocks while achieving comparable resolution and relative inaccuracy.

IV. System Integration

The proposed temperature sensor was fabricated into a separate chip for integration into an ultra-low power wireless sensor node [3]. Fig. 21 shows a die photo of the stacked system and corresponding IC layers. The newly designed sensor layer contains the proposed temperature sensor. The other layers are similar to those reported in [3]. After initial programing, the stacked system switches between sleep and active modes to periodically take temperature measurements. Measured data has been successfully retrieved by the processor layer and checked with an external debugger. Also, measured data is transmitted and received by using a near-field radio [2] (Fig. 22).

Fig. 23 shows a block diagram of the temperature sensor interface with the full system. The temperature sensing core consumes 20 nW at room temperature and is power-gated to minimize standby power consumption. However, ring oscillators and counters are not power-gated since they consume negligible power ($\sim$7 pW) during standby mode. When power gating is released, a certain amount of startup time is required for the temperature sensing core to stabilize. Stabilization requires 100 ms at room temperature with an energy consumption of 1.6 nJ (simulated). Since there is no benefit to having the processor running during this time, the processor initially goes to sleep after a temperature measurement request. The start-up delay is generated internally using a leakage-based oscillator [20] and programmable counter. When a temperature measurement is requested, power gating is released and the leakage-based oscillator starts. Frequency of the leakage-based oscillator has comparable temperature dependency to the required stabilization time of the sensing core. After counting up to a pre-configured number of cycles, *Start* signal is released and oscillation begins. To allow the frequencies to stabilize, conversion starts after a fixed number of cycles of the reference oscillator. When conversion is finished, interrupt is asserted to wake-up the processor for data acquisition. Finally, the *CLR* signal is set from the processor to reset the temperature sensor and power gating is reasserted.

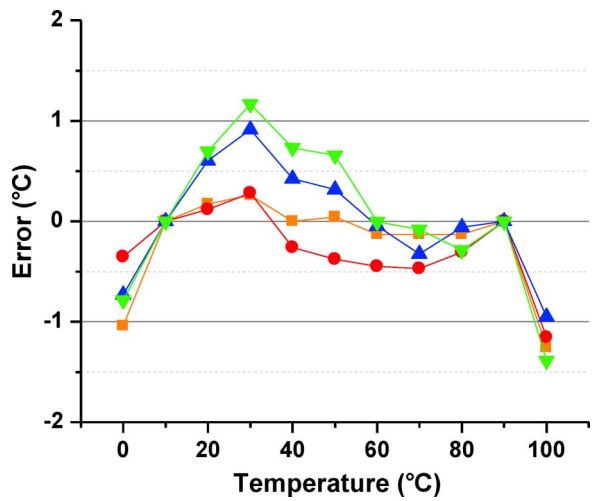


Fig. 24. Measured temperature error of the stacked system over 4 samples.

Fig. 24 shows measured error of 4 stacked sensor nodes after 2-point calibration at 10°C and 90°C ($+1.2°\mathrm{C}/-1.4°\mathrm{C}$). Compared to measurement results shown in Section III, the accuracy of the sensor is maintained. On the other hand, average resolution is measured to be 0.8°C (rms, 30 ms/conversion). The resolution degrades by $\times 2.6$ compared to standalone testing, mainly due to supply voltage ripple when generated by the power management unit (PMU) based on switch capacitor network. However, the resolution is improved to 0.37°C by increasing conversion time $(\times 4)$, at the expense of energy.

V. Conclusion

This work demonstrated a novel temperature sensor that can be integrated into a battery-driven ultra-low power system. The sensor achieves ultra-low power by introducing a new sensing element that benefits from low output voltage and process invariant temperature characteristics. Moreover, a second feedback loop is introduced into a conventional voltage-to-current converter to eliminate power consumed in a current mirror.

TABLE I
PERFORMANCE SUMMARY AND ITS COMPARISON WITH RECENTLY PUBLISHED LOW POWER TEMPERATURE SENSORS

Parameters	This Work	[14]	[13]	[11]	[12]	[15]	[21]	[22]	[23]	[24]	[25]	[9]
Technology	**0.18μm**	0.18μm	0.35μm	0.18μm	0.18μm	0.16μm	0.35μm	0.35μm	0.18μm	0.18μm	65nm	0.16μm
Type	**MOSFET**	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET	BJT
Area	**0.09mm^2**	0.05mm^2	0.084mm^2	0.042mm^2	0.032m^2	0.085mm^2	0.175mm^2	0.4mm^2	0.0413mm^2	0.18mm^2	0.008mm^2	0.08mm^2
Supply Voltage	**1.2V**	1V	1.4V, 2.1V	0.5V, 1V	1.2V	0.85-1.2V	3.3V	3V	1.1V	1.2V	1V	1.5V
Temperature Range	**0-100℃**	0-100℃	35-45℃	-10-30℃	0-100℃	-40-125℃	0-100℃	0-75℃	35-105℃	0-100℃	0-110℃	-55-125℃
Resolution	**0.3℃[1]**	0.1℃[1]	0.035℃/LSB	0.2℃/LSB	0.3℃/LSB	0.063℃[1]	0.16℃/LSB	0.5℃/LSB	1.94℃/LSB	0.25℃/LSB	0.94℃[1]	0.02℃[1]
Conversion Time	**30ms**	100ms	100ms	30ms	1ms	6ms	500ms	50ms	0.128ms	0.0125ms	0.00213ms	5.3ms
Calibration	**2-point**	2-point	2-point	2-point	2-point	1-point	2-point	2-point	1-point	1-point	1-point	1-point
Inaccuracy	**+1.5℃/-1.4℃[2a]**	+3℃/-1.6℃[2a]	+0.1/-0.1℃[2a]	+1℃/-0.8℃[2a]	+1℃/-0.8℃[2a]	±0.4℃[2b]	+0.9℃/-0.7℃[2a]	+1/-1℃[2a]	+2.7℃/-1.4℃[2a]	+0.5℃/-0.5℃[2a]	+1.5℃/-1.4℃[2a]	±0.15℃[2b]
Relative Inaccuracy[3]	**2.9**	4.6	2	4.5	1.8	0.48	1.6	2	4.6	1	2.7	0.2
Fully Integrated[4]	**Yes**	Yes	No	No	No	No	Yes	Yes	No	No	Yes	No
Power	**71nW**	220nW	110nW[5]	120nW[5]	405nW[5]	600nW[5]	10μW	9μW	23.1μW[5]	24μW[5]	500uW	5.1μW[5]
Energy/ Conversion	**2.2nJ**	22nJ	11nJ[5]	3.6nJ[5]	0.41nJ[5]	3.6nJ[5]	5000nJ	450nJ	3nJ[5]	0.3nJ[5]	1.1nJ	27nJ[5]
FOM[6]	**0.19**	0.22	0.013[5]	0.14[5]	0.037[5]	0.014[5]	32	110	11	0.019[5]	0.94	0.011[5]

1. Degree RMS.
2a. Maximum error value, 2b. 3σ value.
3. Relative Inaccuracy (%) = Max error/Temperature range ×100 [26] .
4. The sensor does not require any external references for their operation.
5. Power or Energy for generating external references not include.
6. FOM[nJ/K^2] = Energy/conversion × (Resolution)^2 [26].

As a result, the sensor consumes only 71 nW at room temperature. Without any external components, the sensor achieves $+1.5°C/-1.4°C$ of inaccuracy from 0°C to 100°C and consumes 2.2 nJ/conversion. An example use scenario for the proposed sensor is demonstrated in a battery-operated wireless sensor node.

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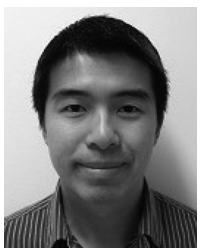

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Dr. Sylvester received an NSF CAREER award, the Beatrice Winner Award at ISSCC, an IBM Faculty Award, an SRC Inventor Recognition Award, and eight best paper awards and nominations. He is the recipient of the ACM SIGDA Outstanding New Faculty Award and the University of Michigan Henry Russel Award for distinguished scholarship. He serves on the technical program committee of the IEEE International Solid-State Circuits Conference and previously served on the executive committee of the ACM/IEEE Design Automation Conference. He has served as Associate Editor for IEEE TRANSACTIONS ON CAD and IEEE TRANSACTIONS ON VLSI SYSTEMS and Guest Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II.