A CMOS Smart Temperature Sensor With a 3σ Inaccuracy of ± 0.1°C From -55 °C to 125 °C

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***Abstract*—A smart temperature sensor in 0.7 μm CMOS is accurate to within ± 0.1 °C (3σ) over the full military temperature range of -55 °C to 125 °C. The sensor uses substrate PNP transistors to measure temperature. Errors resulting from nonidealities in the readout circuitry are reduced to the 0.01 °C level. This is achieved by using dynamic element matching, a chopped current-gain independent PTAT bias circuit, and a low-offset second-order sigma-delta ADC that combines chopping and correlated double sampling. Spread of the base-emitter voltage characteristics of the substrate PNP transistors is compensated by trimming, based on a calibration at one temperature. A high trimming resolution is obtained by using a sigma-delta current DAC to fine-tune the bias current of the bipolar transistors.**

***Index Terms*—Dynamic element matching, offset cancellation, sigma-delta conversion, smart sensors, temperature sensors.**

I. Introduction

TEMPERATURE sensors are widely applied in measurement, instrumentation, and control systems. In many applications, it would be attractive to use temperature sensors that produce a readily interpretable temperature reading in a digital format. Such "smart" temperature sensors combine a sensor and interface electronics on a single chip, and are preferably manufactured in a low-cost standard CMOS process [1]–[5].

Nevertheless, most temperature sensors applied today are conventional sensors, such as thermistors or platinum resistors, which require separate readout circuitry. In part, the limited use of smart sensors can be attributed to their restricted operating range (typically limited to the military range from -55 °C to 125 °C). More importantly, they are relatively inaccurate compared to conventional sensors. A typical inaccuracy in the mentioned temperature range is ± 2 °C, while the inaccuracy that can be obtained with, for instance, a class-A platinum resistor in that range is ± 0.5 °C [6]. Higher accuracy can be obtained by calibration at multiple temperatures, but this would undo much of the cost advantage of CMOS smart temperature sensors.

Most CMOS smart temperature sensors are based on the temperature characteristics of parasitic bipolar transistors [1], [2]. Previous designs employed dynamic offset cancellation techniques, such as nested-chopping [1], [5], [7] and autozeroing [4], [8], to reduce temperature errors due to the offset of the CMOS amplifiers used in the readout circuitry. Since the characteristics of the bipolar transistors used are not entirely linear, curvature correction techniques have been used to improve the linearity [5], [7], [9]. The lowest reported inaccuracy achieved using these techniques is ± 0.5 °C (3σ) [5].

In this paper, a CMOS smart temperature sensor is presented that achieves an inaccuracy of only ± 0.1 °C (3σ) over the military range [10]. All errors caused by the readout circuitry are reduced to the 0.01 °C level. In addition to offset cancellation and curvature correction, precision biasing techniques are used, and dynamic element matching is used to reduce mismatch-related errors. As a result, the spread of the characteristics of the bipolar transistors is the only significant error source in the sensor. A calibration at a single temperature is then sufficient to determine this error and correct it by means of trimming. Since the spread essentially has only one degree of freedom, this correction is effective over the full operating range.

This paper is organized as follows. Section II describes the measurement principle used. Sections III, IV, and V discuss details of the circuit implementation. Experimental results are presented in Section VI. The paper ends with conclusions.

II. Measurement Principle

In order to produce a digital temperature reading, a *ratiometric* measurement has to be performed: a temperature-dependent signal has to be compared to a reference signal. While virtually every device has temperature-dependent characteristics, bipolar transistors are particularly suitable for generating this combination of signals [11]. They can be used to generate both a voltage that is accurately proportional to absolute temperature (PTAT), and a temperature-independent bandgap reference voltage. In CMOS, substrate bipolar transistors can be used for this purpose [2].

A. Ratiometric Temperature Measurement

Fig. 1 illustrates the operating principle of the sensor. Two diode-connected substrate PNP transistors are used to generate two voltages $V_{\rm BE}$ and $\Delta V_{\rm BE}$. These voltages are combined to produce the PTAT and reference voltages mentioned above, which are converted to a digital temperature reading $D_{\rm out}$ using an analog-to-digital converter (ADC).

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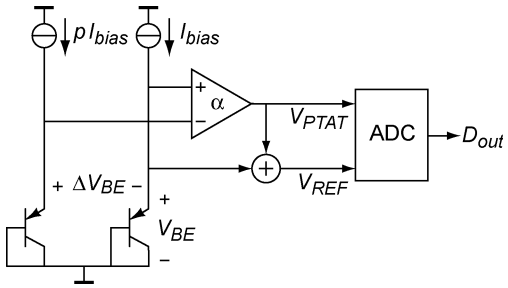

Fig. 1. Operating principle of the temperature sensor.

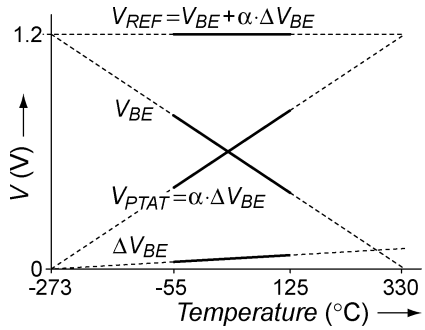

Fig. 2. Temperature dependency of the key voltages in the sensor.

The base-emitter voltage $V_{\rm BE}$ of a bipolar transistor in its forward-active region can be described by the following well-known logarithmic equation:

$$V_{\rm BE}(T) = \frac{kT}{q} \ln\left(\frac{I_{\rm bias}(T)}{I_S(T)}\right) \tag{1}$$

where k is Boltzmann's constant, q is the electron charge, T is the absolute temperature, I_S the transistor's saturation current, and $I_{\rm bias}$ is its collector current, determined by a bias circuit [11]. In the case of a substrate PNP transistor, which is biased via its emitter, the resulting collector current is affected by the transistor's current gain. This effect will be ignored for now, and discussed in Section IV-D.

As a result of the strong temperature dependency of the saturation current I_S, the base-emitter voltage has a negative temperature coefficient of about -2 mV/°C (Fig. 2). The exact value depends on the absolute value of I_S and $I_{\rm bias}$. The extrapolated value of $V_{\rm BE}$ to 0 K is roughly 1.2 V and is often denoted as V_{g0}, as it is related to the silicon bandgap energy. This voltage is independent of the absolute values of I_S and $I_{\rm bias}$ [11].

Using (1), it can be easily shown that the difference in base-emitter voltage $\Delta V_{\rm BE}$ between two bipolar transistors operated at a $p:1$ collector-current ratio is PTAT:

$$\Delta V_{\rm BE}(T) = \frac{kT}{q} \ln(p). \tag{2}$$

This difference only depends on the ratio p, making $\Delta V_{\rm BE}$ an accurate measure of temperature [2]. A larger ratio results in a larger $\Delta V_{\rm BE}$, but care has to be taken to ensure that the two transistors remain in the same operating region. In our design, a current ratio of $p = 5$ is used, resulting in a temperature coefficient of 0.14 mV/°C.

A bandgap reference can be used as the reference voltage of an ADC designed to digitize $\Delta V_{\rm BE}$. As illustrated in Fig. 2, this reference is generated by adding an amplified version of $\Delta V_{\rm BE}$ to $V_{\rm BE}$ so as to obtain a temperature-independent voltage $V_{\rm REF}$:

$$V_{\rm REF} = V_{\rm BE} + \alpha \cdot \Delta V_{\rm BE}. \tag{3}$$

For the mentioned temperature coefficients, a gain of about $\alpha = 16$ is required.

An ADC that converts the ratio of $\alpha \cdot \Delta V_{\rm BE}$ and $V_{\rm REF}$ can be used to obtain a digital temperature reading $D_{\rm out}$

$$D_{\rm out} = A \cdot \frac{\alpha \cdot \Delta V_{\rm BE}}{V_{\rm REF}} - B \tag{4}$$

where the coefficients $A \simeq 600$ and $B \simeq 273$ are chosen so as to obtain a digital output in degrees Celsius [5].

B. Correction for Process Spread

While $\Delta V_{\rm BE}$ is insensitive to process spread, $V_{\rm BE}$ depends on the absolute values of both the saturation current and the bias current, and will therefore spread with variations in the IC process. Assuming that the spread of these currents does not significantly change their temperature dependency, the resulting spread of $V_{\rm BE}$ can be written as

$$\begin{aligned} V_{\rm BE}(T) &= \frac{kT}{q} \ln\left(\frac{I_{\rm bias}(T)\,(1+\varepsilon_{I_{\rm bias}})}{I_S(T)\,(1+\varepsilon_{I_S})}\right) \\ &= \frac{kT}{q} \ln\left(\frac{I_{\rm bias}(T)}{I_S(T)}\right) + \frac{kT}{q} \ln\left(\frac{1+\varepsilon_{I_{\rm bias}}}{1+\varepsilon_{I_S}}\right) \end{aligned} \tag{5}$$

where $\varepsilon_{I_{\rm bias}}$ and ε_{I_S} are the relative errors in the collector and saturation current, respectively. This shows that the error in $V_{\rm BE}$ with respect to its nominal value is PTAT.

Provided all other errors in the sensor are negligible, this PTAT error in $V_{\rm BE}$ can be determined from a calibration at one temperature. The error can then be corrected by means of trimming. This should be done in such a way that the resulting correction is PTAT, and will thus null the PTAT error over the complete operating temperature range [2].

A PTAT correction of $V_{\rm BE}$ can be established by trimming the transistor's emitter area, its bias current, or by adding a programmable PTAT voltage to it [5]. We choose to trim the bias current using a sigma-delta digital-to-analog converter (DAC) (see Section IV-B) to obtain a high trimming resolution [12].

C. Accuracy Requirements

To make the mentioned trimming scheme work, all error sources other than PTAT spread of $V_{\rm BE}$ have to be made negligible by design. Systematic errors, which result in nonlinearity, can be corrected for by introducing a compensating nonlinearity in the readout circuitry, as will be shown below. Random errors need to be reduced by design to the 0.01 °C level to obtain an overall inaccuracy of ± 0.1 °C.

To find what random errors in $V_{\rm BE}$ can be tolerated, the sensitivity of the sensor's output $D_{\rm out}$ to changes in $V_{\rm BE}$ has to be

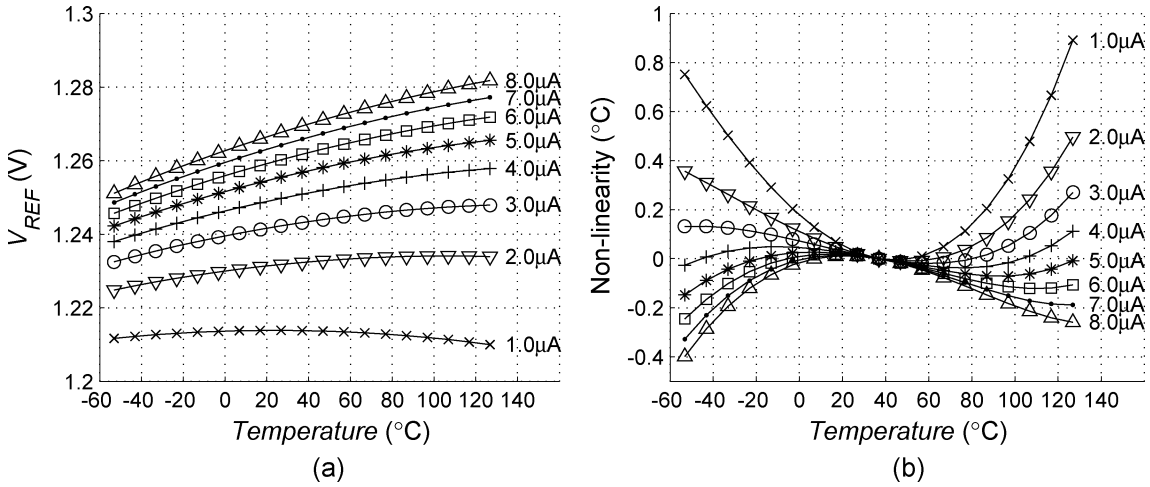

Fig. 3. (a) Simulated temperature dependency of the reference voltage $V_{\rm REF}$ as a function of the bias current at room temperature. (b) Associated nonlinearity of the sensor's output $D_{\rm out}$ (i.e., error with respect to a linear fit).

calculated. This sensitivity is largest at the lower end of the temperature range, where it is approximately (1/3)°C/mV. A maximum temperature error 0.01 °C therefore implies a maximum random voltage error in $V_{\rm BE}$ of 30 μV. Similarly, the maximum random voltage error in $\Delta V_{\rm BE}$ can be found to be about 2 μV. This means that all circuit errors, such as the input-referred offset of the readout electronics, have to be reduced to these levels.

D. Curvature Correction

So far, it has been assumed that $V_{\rm BE}$ is a linear function of temperature. In practice, however, $V_{\rm BE}$ is slightly nonlinear. The magnitude of this nonlinearity, which will be referred to as curvature, depends on the temperature dependency of the saturation current, and on that of the collector current. For a PTAT collector current, it can be written as [11]

$$V_{\rm curv}(T) = \frac{k}{q}(\eta - 1)\left(T - T_r - T\ln\left(\frac{T}{T_r}\right)\right) \qquad (6)$$

where η is the temperature exponent in the analytical expression for the saturation current (a parameter called XTI in SPICE), and T_r is a reference temperature. For our process $\eta \simeq 4$. As will be discussed in Section IV-C, we use a bias current derived from a PTAT voltage using a poly resistor. If the temperature dependency of this resistor is also taken into account, a predominantly quadratic curvature of about 4 mV is found over the military range.

As this curvature is present in the reference voltage $V_{\rm REF}$, it results in an inverse quadratic nonlinearity at the output of the sensor. This is illustrated in Fig. 3, which shows the temperature dependency of $V_{\rm REF}$ and the resulting nonlinearity of the output given by (4), both with the bias current at room temperature as a parameter. For a bias current of 1 μA, $V_{\rm REF}$ is a conventional bandgap reference voltage, with a zero temperature coefficient at room temperature and a small quadratic curvature. The curvature then leads to a quadratic nonlinearity of almost 1 °C at the output.

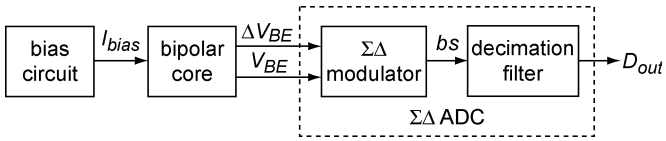

Fig. 4. Block diagram of the temperature sensor.

If the bias current is increased, $V_{\rm REF}$ becomes an "overcompensated" bandgap reference voltage, with a positive temperature coefficient. Fig. 3 shows that the associated nonlinearity at the output then decreases. A minimum nonlinearity of about 0.1 °C is reached for a bias current between 4 and 5 μA.

This can be explained as follows. The linear temperature dependency of $V_{\rm REF}$ gives rise to a nonlinearity at the output, since it appears in the denominator in (4). With a proper choice of the temperature coefficient of the reference, this nonlinearity will compensate for the nonlinearity due to the curvature of $V_{\rm BE}$. Thus, the curvature can largely be eliminated by using a reference voltage with a small positive temperature coefficient [7], [9].

E. Block Diagram

Fig. 4 shows a block diagram of the sensor. A bipolar core generates the voltages $\Delta V_{\rm BE}$ and $V_{\rm BE}$. These are input to a sigma-delta $(\Sigma\Delta)$ modulator, which produces a bitstream bs, of which the average value is equal to the ratio of $\alpha \cdot \Delta V_{\rm BE}$ and $V_{\rm REF}$. The charge-balancing conversion applied in this switched-capacitor modulator is the topic of Section III, while details of the modulator will be discussed in Section V.

A decimation filter is used to filter the quantization noise from the bitstream and perform the required scaling to obtain the output $D_{\rm out}$ as given by (4). As will be explained in Section V-E, this filter also introduces a small nonlinearity to compensate for the above-mentioned residual nonlinearity of about 0.1 °C.

A special bias circuit is used to provide accurate bias currents to the bipolar core. This will be discussed in Section IV.

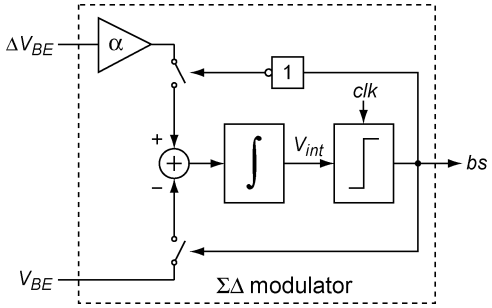

Fig. 5. Block diagram of the $\Sigma\Delta$ modulator.

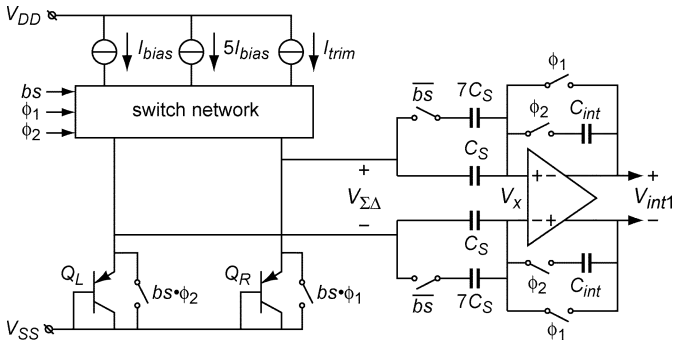

Fig. 6. Simplified circuit diagram of the front-end of the $\Sigma\Delta$ modulator.

III. Charge-Balancing Conversion

A. Charge-Balancing Principle

Fig. 5 shows a block diagram of the $\Sigma\Delta$ modulator. The modulator consists of a loop filter and a clocked comparator. For simplicity, only a first-order loop filter is shown. In the actual modulator, a second-order filter is used (see Section V). Every clock cycle, the comparator produces a bit of the bitstream bs based on the polarity of the output $V_{\rm int}$ of the loop filter. The feedback is arranged so as to drive the output of the integrator to zero.

If the bitstream in a given clock cycle is zero, $\alpha \cdot \Delta V_{\rm BE}$ is integrated, while $-V_{\rm BE}$ is integrated if the bitstream is one. As a result of the feedback in the modulator, the average input to the integrator is zero. In other words, the charge added by $\alpha \cdot \Delta V_{\rm BE}$ is balanced by the charge removed by $-V_{\rm BE}$. If the average value of the bitstream is denoted as μ, this charge balancing can be expressed as

$$(1-\mu)\cdot\alpha\cdot\Delta V_{\rm BE} = \mu \cdot V_{\rm BE}. \tag{7}$$

Solving for μ gives

$$\mu = \frac{\alpha\cdot\Delta V_{\rm BE}}{V_{\rm BE}+\alpha\cdot\Delta V_{\rm BE}} = \frac{\alpha\cdot\Delta V_{\rm BE}}{V_{\rm REF}}. \tag{8}$$

Thus, with a simple charge-balancing scheme, a digital representation of the ratio in (4) is obtained [1].

B. Switched-Capacitor Implementation

In [1] and [5], continuous-time implementations of the above-mentioned charge-balancing scheme were presented. In this work, we choose for a switched-capacitor implementation, because this facilitates the implementation of the various offset cancellation and dynamic element matching techniques required to meet the $\pm 0.1\,^{\circ}$C inaccuracy target.

A simplified circuit diagram of the front-end of the $\Sigma\Delta$ modulator is shown in Fig. 6. The integrator uses correlated double-sampling to eliminate the operational amplifier's offset and $1/$f noise [13] and is similar to the design presented in [8].

The integrator operates in two phases. Suppose, for now, that $bs = 1$, and hence the $7C_S$ capacitors are not used. During phase ϕ_1, when the opamp is switched in unity-gain, the voltage $V_{\Sigma\Delta}(\phi_1)$ is sampled on capacitors C_S with respect to the opamp's virtual ground $V_x(\phi_1)$. In the second phase ϕ_2, the integrator capacitor $C_{\rm int}$ is switched in the feedback path, and the input voltage changes to $V_{\Sigma\Delta}(\phi_2)$. As a result, the output of the integrator changes by

$$\Delta V_{\rm int} = \frac{C_S}{C_{\rm int}}\left\{V_{\Sigma\Delta}(\phi_1) - V_{\Sigma\Delta}(\phi_2) - (V_x(\phi_1) - V_x(\phi_2))\right\}. \tag{9}$$

This shows that slowly varying signals at the opamp's virtual ground, such as its offset and $1/$f noise, are eliminated. The change in $V_{\rm int}$ is proportional to the change in $V_{\Sigma\Delta}$.

The modulator's input $V_{\Sigma\Delta}$ is generated by two substrate bipolar transistors Q_L and Q_R. The bias currents of these transistors are determined by a switch network based on the integrator phase and the value of the bitstream bs.

If $bs = 0$, $\Delta V_{\rm BE}$ has to be integrated. To achieve this, the current $I_{\rm bias}$ is directed to Q_L during phase ϕ_1, while a 5 times larger current is directed to Q_R. As a result, $V_{\Sigma\Delta}(\phi_1) = \Delta V_{\rm BE}$. During phase ϕ_2, the currents are swapped, so that $V_{\Sigma\Delta}(\phi_2) = -\Delta V_{\rm BE}$. Therefore, the change in the integrator's output is proportional to $2\Delta V_{\rm BE}$. Note that mismatch between Q_L and Q_R does not affect the accuracy of this change.

If $bs = 1$, $-V_{\rm BE}$ has to be integrated. During phase ϕ_1, Q_R is shorted to ground, while Q_L is biased by the current $I_{\rm trim}$. As a result, $V_{\Sigma\Delta}(\phi_1) = -V_{\rm BEL}$. During phase ϕ_2, Q_L is shorted and the current $I_{\rm trim}$ is switched to Q_R, so that $V_{\Sigma\Delta}(\phi_2) = V_{\rm BER}$. The change in the integrator's output is then proportional to $-(V_{\rm BEL}+V_{\rm BER})$, so that effectively the average base-emitter voltage of the two transistors is used.

The gain α can be implemented in two ways in this integrator. One way is to use a larger sampling capacitance when integrating $\Delta V_{\rm BE}$ ($bs = 0$). Alternatively, $\Delta V_{\rm BE}$ can also be integrated multiple times every time $bs = 0$. We use a combination of these techniques: an 8 times larger sampling capacitance is used for $\Delta V_{\rm BE}$; moreover, $\Delta V_{\rm BE}$ is integrated twice if $bs = 0$, while $V_{\rm BE}$ is integrated only once if $bs = 1$. Thus, a gain α of $2 \cdot 8 = 16$ is realized.

IV. Biasing Circuitry

A. Dynamically Matched Current Ratio

Mismatch will limit the accuracy of the 1:5 current ratio in Fig. 6, and hence that of $\Delta V_{\rm BE}$. It can be shown that the current ratio has to be accurate to $\pm 0.011\%$ to limit the temperature error resulting from mismatch to $\pm 0.01\,^{\circ}$C. Such accurate

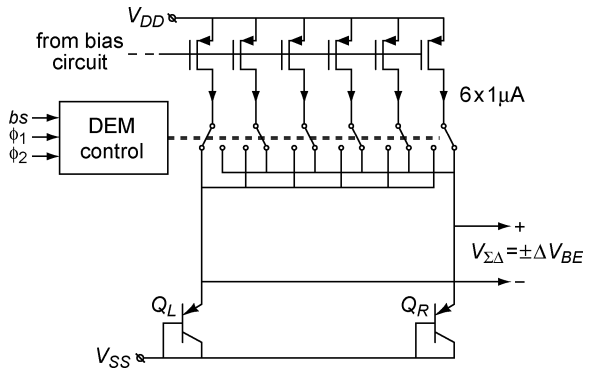

Fig. 7. Current-source configuration used to obtain a dynamically matched 1:5 bias current ratio for generating $\Delta V_{\rm BE}$.

matching cannot be expected from precise layout alone. Therefore, dynamic element matching is used to average out mismatches.

Fig. 7 shows how this has been implemented [2]. Six PMOS current sources provide copies of the current generated in the bias circuit. These current sources are nominally 1 μA each. Using a set of switches, each current can either be directed to Q_L or to Q_R. One of them is switched to one transistor, providing the unit current in the 1:5 ratio, while the remaining currents are switched to the other transistor. The error in the resulting current ratio depends on the mismatch between the unit current source and the average of the other current sources. By alternating the unit current source in successive cycles of the $\Sigma\Delta$ modulator, mismatch errors are averaged out. The required averaging is performed by the integrator of $\Sigma\Delta$ modulator [14].

B. Current Trimming

As discussed in Section II-B, the bias current $I_{\rm trim}$ used for generating $V_{\rm BE}$ has to be trimmed in order to compensate for the spread ε_{I_S} in the nominal value of the transistor's saturation current and the spread $\varepsilon_{I_{\rm bias}}$ of the bias current itself. While the equivalent trimming resolution at the sensor's output has to be in the order of 0.01 °C, the temperature error due to spread can be several degrees. This implies a trimming range of about 10 bits.

Conventional trimming techniques include adjustment of the emitter area or the bias current using switchable binary-scaled transistors or bias current sources [2]. Given the large required range, such techniques would become complex and require a large chip area.

Instead, we use a compact sigma-delta DAC to trim the bias current [12]. Fig. 8 shows how this has been implemented. The same six PMOS current sources used for generating the 1:5 current ratio are used to generate $I_{\rm trim}$. This is possible because $\Delta V_{\rm BE}$ and $V_{\rm BE}$ are never needed at the same time. Five of these sources are used for coarse trimming, and are switched on or off based on the digital input C. The sixth source is used for fine trimming, and is modulated by the bitstream $trim\_bs$ of a digital $\Sigma\Delta$ modulator. The resulting total current $I_{\rm trim}$ is thus switching back and forth between C and $C+1$ times the unit current of 1 μA. The input F of the digital modulator can be

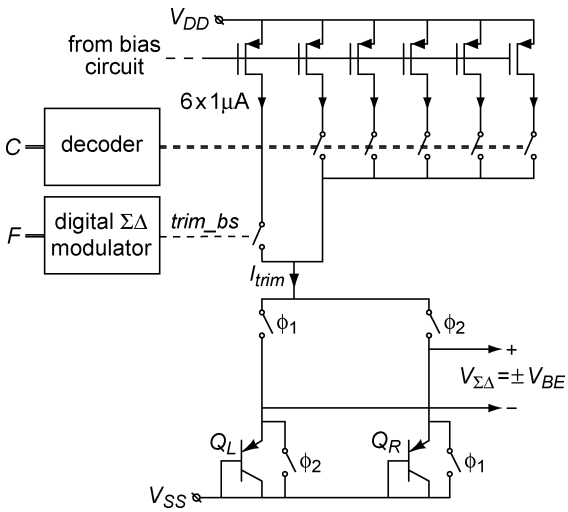

Fig. 8. Current-source configuration used to obtain a trimmable bias current $I_{\rm trim}$ for generating $V_{\rm BE}$.

used to program the average value of the current. The required averaging takes place in the integrator of the analog $\Sigma\Delta$ modulator.

An 8-bit first-order digital $\Sigma\Delta$ modulator is used to obtain a trimming resolution of 4 nA, which corresponds to 0.01 °C at the output of the sensor. A compact implementation of such a modulator is an 8-bit accumulator of which the carry bit is used to generate the bitstream [15]. The total trimming range of 0–6 μA is sufficient to compensate for practical spread of I_S and $I_{\rm bias}$.

In the implementation, current sources whose outputs are not used are connected to an extra diode-connected transistor (not shown in Fig. 8), so as to limit the switching transients at their outputs.

C. Choice of Bias Current Type

While spread in the absolute value of the bias current can be tolerated, as it can be trimmed out, other errors in the bias current, such as variation with the supply voltage and spread of its temperature dependency, should be minimized.

A bias current is generally derived from a bias voltage using a resistor. A difference in base-emitter voltage is a good candidate for the bias voltage, because, as discussed before, it only depends on a current ratio. An additional advantage of using such a PTAT bias voltage is that the resulting temperature dependency of the bias current reduces the curvature of $V_{\rm BE}$ compared to, for instance, a constant bias voltage [11].

As bias resistor we use a high-resistivity polysilicon resistor. The temperature dependency of this resistor affects the curvature of $V_{\rm BE}$, and has been taken into account in the design of the curvature correction (see Section II-D). Spread of this temperature dependency results in a non-PTAT spread of $V_{\rm BE}$, which cannot be trimmed out. It is therefore important to choose a bias resistor with a reproducible temperature dependency. Since data on this reproducibility were not available for the resistors of our process, we chose to use a high-resistivity polysilicon resistor,

which is available as a process option for analog applications, and was therefore expected to be reasonably well controlled.

D. Current-Gain Independent Bias Circuit

As a substrate PNP transistor has to be biased via its emitter, the transistor's forward current-gain β_F affects its collector current, and hence the generated base-emitter voltage:

$$V_{\rm BE} = \frac{kT}{q}\ln\left(\frac{I_C}{I_S}\right) = \frac{kT}{q}\ln\left(\frac{I_{\rm bias}}{I_S}\frac{\beta_F}{\beta_F+1}\right). \quad (10)$$

It can be shown that spread of β_F does not result in a purely PTAT spread of $V_{\rm BE}$, as a result of the strong temperature-dependency of β_F. The resulting temperature errors therefore cannot be completely trimmed out. For a nominal current-gain β_{F0} of 22, as found in our 0.7 μm CMOS process, the resulting error after trimming is about 0.05 °C at the extremes of the operating temperature range for a $\pm 10\%$ spread of β_{F0}. This error will be larger for more modern CMOS processes in which smaller values of β_{F0} are found.

Fig. 9 shows a PTAT bias circuit that can be used to eliminate the current-gain dependency of $V_{\rm BE}$. Two PNP transistors Q_{B1} and Q_{B2} are biased at a 1:m current ratio. As a result, the difference between their base-emitter voltages is

$$\Delta V_{\rm BE,bias} = \frac{kT}{q}\ln(m) \quad (11)$$

The feedback loop ensures that the input voltage of the opamp is zero, so that we can write

$$R_{\rm bias}\cdot I_{\rm bias} - \frac{R_{\rm bias}}{m}\frac{m\cdot I_{\rm bias}}{\beta_F+1} = \Delta V_{\rm BE,bias}. \quad (12)$$

Solving for $I_{\rm bias}$ gives

$$I_{\rm bias} = \frac{\beta_F+1}{\beta_F}\frac{\Delta V_{\rm BE,bias}}{R_{\rm bias}} \quad (13)$$

that is, the generated bias current depends on β_F. Substituting this current in (10) shows that the β_F-dependent terms cancel (assuming ideal matching), so that the generated base-emitter voltage $V_{\rm BE}$ is independent of the current gain.

The presented bias circuit has an inherently high power-supply rejection, as all PMOS transistors connected to $V_{\rm DD}$ have matched drain-source voltages, including the output transistor that provides bias current to the bipolar core. In the implemented circuit, cascoding has been used to further improve the power supply rejection.

E. Offset Cancellation

Offsets in the bias circuit of Fig. 9 introduce spread in $V_{\rm BE}$ that cannot be completely trimmed out. This applies to both the offset of the opamp and that due to mismatch between Q_{B1} and Q_{B2}. These offsets must be small compared to $\Delta V_{\rm BE,bias}$. It can be shown that for a current-ratio $m = 10$, the combined offset

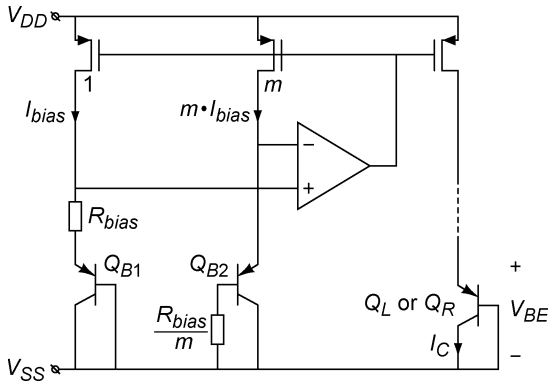

Fig. 9. PTAT bias circuit that makes $V_{\rm BE}$ independent of the forward current-gain.

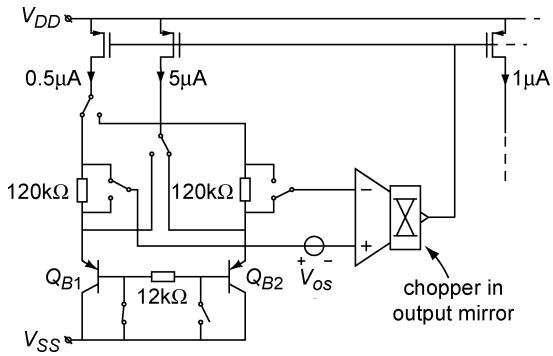

Fig. 10. Implementation of the bias circuit that uses chopping to cancel the offset V_{os}.

V_{os} has to be smaller than ± 70 μV to result in a temperature error smaller than ± 0.01 °C. This implies that some form of offset cancellation is required.

Fig. 10 shows the implementation of the bias circuit, in which chopping is used to cancel the offset V_{os}. A current ratio $m = 10$ and a bias resistor $R_{\rm bias} = 120$ kΩ are used to obtain nominal currents of 0.5 and 5 μA. The nominal bias current provided to the bipolar core is 1 μA.

The bias circuit is chopped synchronously with the integrator of the $\Sigma\Delta$ modulator (Fig. 6). The position of the switches shown in Fig. 10 corresponds to phase ϕ_1 of the integrator. The circuit configuration is then the same as in Fig. 9, and the offset V_{os} adds to $\Delta V_{\rm BE,bias}$, resulting in a bias current which is a bit too large. Via the trimming circuit of Fig. 8, this current is applied to transistor Q_L. With the switches in the other position (which corresponds to phase ϕ_2), the polarity of the offset is effectively reversed, resulting in a bias current which is a bit too small. This current is applied to transistor Q_R. Since the integrator effectively integrates the sum of the base-emitter voltages of Q_L and Q_R, the error due to the offset is largely eliminated. Due to the logarithmic characteristic of transistors, the cancellation is not perfect, but the residual quadratic error is negligible.

The chopping scheme requires an extra bias resistor of 120 kΩ compared to the unchopped circuit. It can be shown that there is no severe matching requirement between the bias

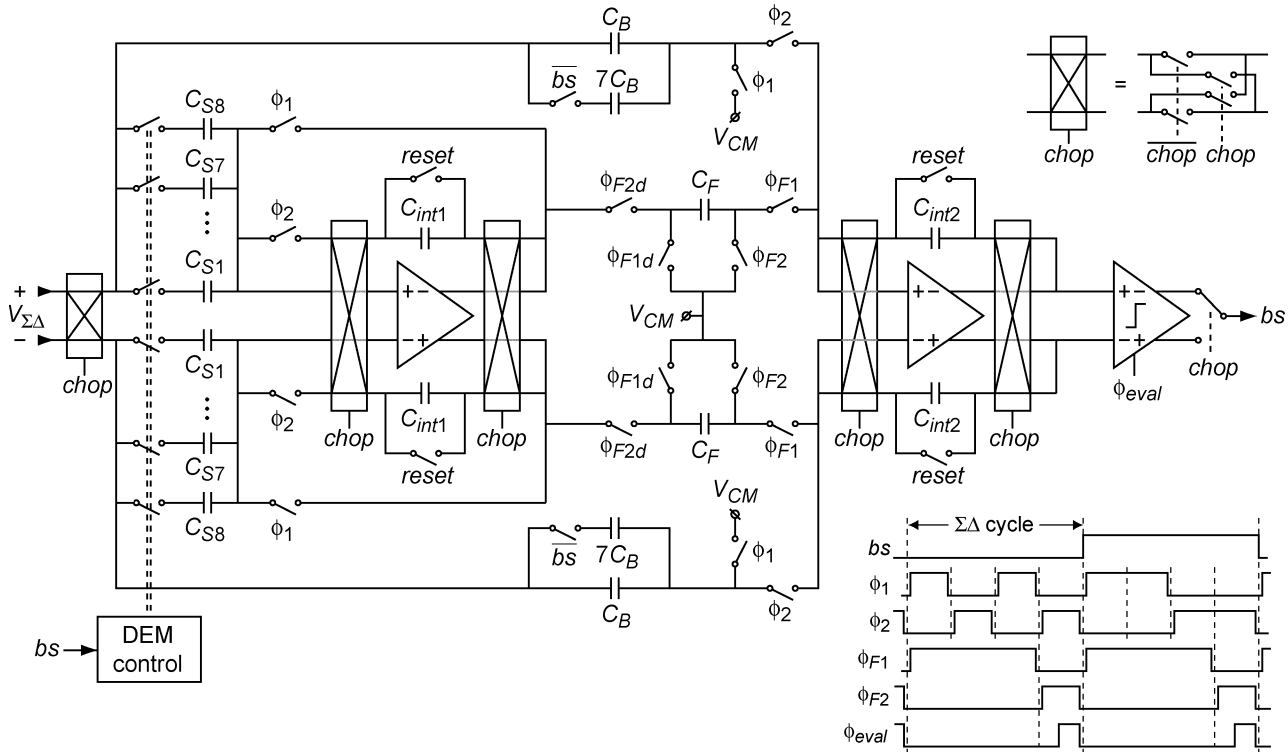

Fig. 11. Circuit diagram of the second-order $\Sigma\Delta$ modulator.

resistors. The opamp is a simple folded-cascode design. Its output current mirror is chopped to maintain negative feedback.

V. Sigma-Delta ADC

A. Modulator Topology

The $\Sigma\Delta$ ADC, consisting of a $\Sigma\Delta$ modulator and a decimation filter, converts $V_{\rm BE}$ and $\Delta V_{\rm BE}$ to a digital temperature reading $D_{\rm out}$. A quantization error in the order of 0.01 °C is desired, which corresponds to about 16 bits (since the full scale is equivalent to about 600 K; see Fig. 2). The desired conversion time is 100 ms.

The $\Sigma\Delta$ ADC is operated differently than conventional $\Sigma\Delta$ ADC's used for audio or communication applications. In such applications, the $\Sigma\Delta$ is running continuously, producing a bitstream which is filtered and decimated to Nyquist-rate output data by a decimation filter. The sensor, in contrast, requires a "one-shot" type of operation. After power-up, the modulator and the decimation filter are reset in order to bring them in a well-defined state. The modulator then produces a given number of bits, which are turned into a single temperature reading by the decimation filter. Finally, the sensor is powered down again to save power. Such operation is also referred to as "incremental" operation, and implies that a relatively simple decimation filter of the same order as the modulator can be used [16].

When using a first-order $\Sigma\Delta$ modulator, a simple counter can be used as decimation filter [1], [7]. However, 2^{16} cycles are required to achieve a resolution of 16 bits. To obtain a conversion time of 100 ms, a clock frequency of about 650 kHz would be required, which would result in an undesirably high power consumption.

To reduce the required clock frequency, a second-order modulator is used. Such a modulator, operated as an incremental ADC, can obtain a resolution of 16 bits in only a few hundred clock cycles (depending on the exact implementation) [16]. Thus, the clock frequency can be reduced to a few kilohertz . A single-loop second-order topology is used that is similar to that presented in [5]. A fully differential switched-capacitor implementation is used, rather than the single-ended mixed continuous-time switched-capacitor implementation described there.

B. Switched-Capacitor Implementation

Fig. 11 shows a circuit diagram of the $\Sigma\Delta$ modulator. Ignoring the chopper switches for now, the first integrator works as described in Section III-B: in a $\Sigma\Delta$ cycle in which the bitstream $bs = 0$, $\Delta V_{\rm BE}$ is integrated in two integration cycles; if $bs = 1$, $V_{\rm BE}$ is integrated in one integration cycle (see the timing diagram in Fig. 11). The sampling capacitor of the first integrator is split in eight unit capacitors of 5 pF each. All of them are used when integrating $\Delta V_{\rm BE}$, while only one is used when integrating $V_{\rm BE}$. Thus, a gain $\alpha = 16$ is realized.

Mismatch between the unit capacitors limits the accuracy of α. It can be shown that α has to be accurate to $\pm 0.0067\%$ to limit the temperature error resulting from mismatch to ± 0.01 °C. As such accurate matching cannot be expected from precise layout alone, dynamic element matching is used. By alternating the unit capacitor used in successive cycles of the $\Sigma\Delta$ modulator in which $bs = 1$, mismatch errors are averaged out [14].

The first integrator essentially determines the accuracy of the modulator. To guarantee negligible errors in this integrator due to finite gain, a gain-boosted folded-cascode implementation with a DC gain of 100 dB was used [17].

At the end of a $\Sigma\Delta$ cycle, the output of the first integrator is sampled on capacitors C_F (of 2 pF), which are discharged into the second integrator at the beginning of the next $\Sigma\Delta$ cycle. To ensure stability of the modulator, a feedforward branch from the input to the second integrator is used. The sampling capacitors C_B (of 1 pF) and $7{\cdot}C_B$ of this branch are switched with the same timing as the input sampling capacitors. Since errors introduced by the second integrator are attenuated by the gain of the first integrator, no offset cancellation, dynamic element matching, or gain boosting is needed here. A simple folded-cascode opamp is used.

The polarity of output of the second integrator is evaluated at the end of every $\Sigma\Delta$ cycle by a clocked comparator. The result determines the value of the bitstream for the next cycle. The comparator is implemented as a dynamic latch preceded by a preamp, which prevents kickback to the output of the second integrator.

The modulator uses nonoverlapping clocks. Switching in the front-end circuitry and updating of the bitstream output take place in the time gap between the clock phases ϕ_1 and ϕ_2, so that any resulting charge injection does not result in errors. Clocks with delayed falling edges (e.g., ϕ_{F1d}) are used to prevent signal-dependent charge injection [18].

C. System-Level Chopping

While offset and $1/\mathrm{f}$ noise of the first integrator are reduced by the applied correlated double-sampling, charge-injection mismatch in the switches driven by ϕ_1 and ϕ_2 results in residual offset. Minimum-size NMOS switches are used to minimize this offset. Nevertheless, an offset of a few tens of μV remains. This is too large, given that the error in ΔV_{BE} has to be in the order of 2 μV.

To further reduce the offset, the modulator is chopped at system-level. A chopper switch at the input and a switch at the output periodically reverse the polarity of the input signal and the bitstream. To avoid disturbing the operation of the modulator when chopping, its state is also inverted by swapping the integration capacitors of both integrators. The chopping is done at a slow speed to make errors due to charge-injection in the chopper switches negligible. Two chopping periods per conversion are used, so as to modulate the offset to the first zero of the decimation filter (see Fig. 12).

D. Timing of a Temperature Conversion

The timing of a complete temperature conversion is illustrated in Fig. 12. After the chip has powered up, the integrators of the modulator are reset. The modulator then runs for 400 cycles, producing a bitstream which is fed into the decimation filter. The resulting conversion result has a resolution of 0.01 °C.

An arbitrary fragment of the bitstream is shown in Fig. 12 to illustrate the timing of the dynamic element matching of the 1:5 current ratio and the 1:8 sampling capacitor ratio, and the timing of the $\Sigma\Delta$-modulated trimming of the bias current.

The current source used for generating the unit current in the 1:5 ratio is selected by a cyclic counter that counts from 1 to 6. This counter is enabled only if the bitstream is 0. Similarly, the unit capacitor used for sampling V_{BE} is selected by a cyclic 1 to 8 counter, which is enabled only if the bitstream is 1 [14].

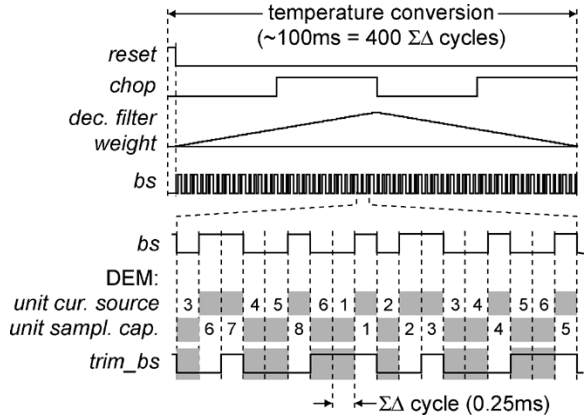

Fig. 12. Timing diagram of a complete temperature conversion.

The digital $\Sigma\Delta$ modulator that produces the fine-trimming bitstream $trim\_bs$ (Fig. 8), is only clocked at the end of $\Sigma\Delta$ cycles in which $bs = 1$. If $bs = 0$ (indicated by the shaded areas in Fig. 12), the modulator is frozen. Fig. 12 shows how this works out if $trim\_bs$ has a 50% duty cycle: a repetitive 0101 pattern appears in successive $\Sigma\Delta$ cycles in which $bs = 1$.

This "bitstream-controlled" operation of the digital $\Sigma\Delta$ modulator prevents quantization noise from being modulated into the signal band due to intermodulation between the two bitstreams [12]. Such intermodulation can occur, because the two bitstreams are effectively multiplied; this is a result of the fact that V_{BE}, which is modulated by $trim\_bs$, is only integrated when $bs = 1$.

E. Decimation Filter

The decimation filter produces a temperature reading D_{out} from the 400 bits produced by the modulator. A sinc^2 filter is used, of which the symmetrical triangular impulse response is shown in Fig. 12. A nonsymmetrical triangular impulse response could be used to obtain the required resolution in fewer clock cycles [16]. Such a filter, however, would not properly average out the modulated offset and DEM residuals. Moreover, the use of a filter with a symmetrical impulse response ensures that the conversion result is a representation of the average temperature during a conversion.

As mentioned in Section II-D, the decimation filter is used to introduce a small nonlinearity that corrects for the nonlinearity that remains after curvature correction. This nonlinearity is only in the order of 0.1 °C. In the present implementation, the correction was implemented by an off-chip lookup table. With only a small circuit overhead, it can be implemented on-chip using the techniques described in [19].

VI. Experimental Results

The sensor was realized in a 0.7 μm CMOS process with linear capacitors and high-resistivity poly resistors. A chip microphotograph is shown in Fig. 13. The chip area is 4.5 mm^2,

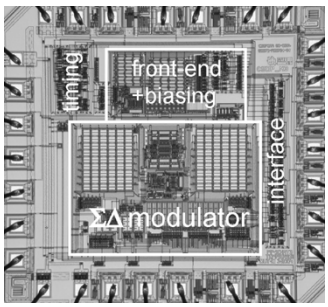

Fig. 13. Chip microphotograph of the temperature sensor.

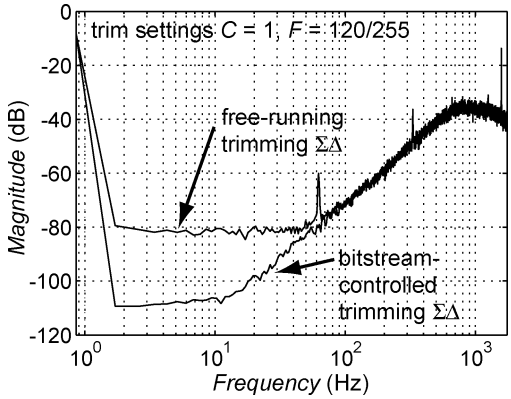

Fig. 14. Measured power spectrum of the bitstream, with the digital trimming $\Sigma\Delta$ modulator operated in free-running and in bitstream-controlled mode (4096 bits, 16× averaged, Hanning windowed).

which includes bondpads and some test circuitry. The decimation filter and digital control circuitry were implemented off-chip for testing flexibility.

Fig. 14 shows measured power spectra of the bitstream of the second-order $\Sigma\Delta$ modulator. The second-order noise shaping is clearly visible. The figure shows the effectiveness of the bitstream-controlled operation of the digital trimming modulator. With a free-running trimming modulator, the noise floor increases by about 30 dB as a result of intermodulated quantization noise that ends up in the signal band.

To determine the temperature error of the sensor, 24 samples from one batch were mounted in ceramic packages, placed in an oven, and compared with a platinum thermometer. This thermometer was calibrated to 20 mK at the Dutch Metrology Institute. The temperature error of the 24 samples before trimming is shown in Fig. 15. The 3σ spread over the range of $-55\,^{\circ}$C to $125\,^{\circ}$C is $\pm 0.5\,^{\circ}$C. The fact that the spread increases toward the high end of the temperature range is consistent with the assumption that it is mainly due to the PTAT spread of V_{BE} [7].

Fig. 16 shows the measured temperature error of the same samples after trimming. The trimming consisted of adjusting the coarse and fine trimming parameters C and F (see Fig. 8) so as to null the temperature error at $30\,^{\circ}$C. This reduces the 3σ spread at the trimming temperature to $\pm 0.03\,^{\circ}$C, while the spread over the full operating temperature range is reduced to $\pm 0.1^{\circ}$C. This performance meets the original target, and shows the effectiveness of the applied readout techniques.

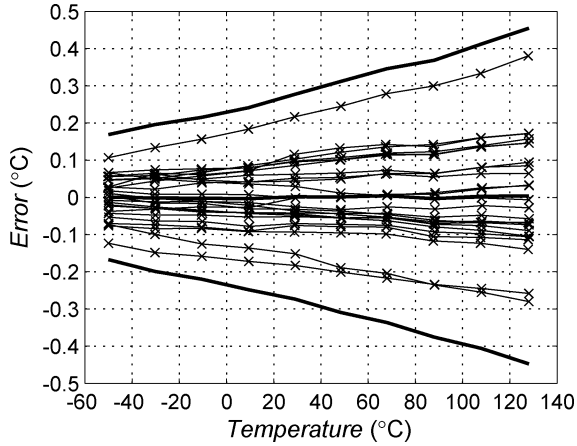

Fig. 15. Measured temperature error of 24 devices before trimming; bold lines indicate the average error and $\pm 3\sigma$ values.

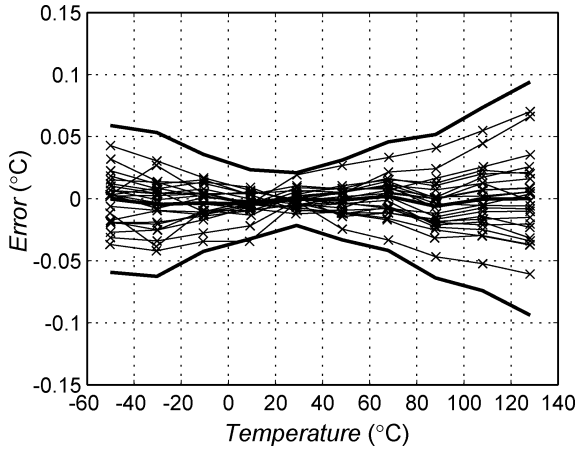

Fig. 16. Measured temperature error of 24 devices after trimming; bold lines indicate the average error and $\pm 3\sigma$ values.

TABLE I
PERFORMANCE SUMMARY

Technology	0.7μm 2M-1P analog CMOS
Chip size	$4.5\mathrm{mm}^2$
Supply voltage	2.5V – 5.5V
Temperature range	-55°C – 125°C
Resolution	0.01°C at 10 conversions/s 0.002°C at 1 conversion/s
Supply current	75μA when operated continuously
Power-supply sensitivity	0.03°C/V from 2.5V to 5.5V
Inaccuracy (3σ)	$\pm 0.03^{\circ}$C at 30°C $\pm 0.1^{\circ}$C from -55°C to 125°C

The above-mentioned measurements were performed at a supply voltage of 3.3 V. The sensor is functional for supply voltages from 2.5 to 5.5 V. Over this range, the power-supply

TABLE II
COMPARISON OF INACCURACY WITH PREVIOUS WORK

Reference	Inaccuracy	Range	Conditions	Calibration
Bakker, 1996 [3]	$\pm 1.0^\circ$C	-40°C to 120°C	min/max of 3 samples	after packaging, 2 points
Tuthill, 1998 [4]	$\pm 1.5^\circ$C	-50°C to 125°C	min/max of 6 samples	wafer-level, 1 point
Pertijs, 2005 [5]	$\pm 0.3^\circ$C	at 25°C	$\pm 3\sigma$ of 32 samples	after packaging, 1 point
	$\pm 0.5^\circ$C	-50°C to 125°C	$\pm 3\sigma$ of 32 samples	after packaging, 1 point
LM92 [20]	$\pm 0.33^\circ$C	at 30°C	min/max	unknown
	$\pm 1.5^\circ$C	-25°C to 150°C	min/max	unknown
DS1626 [21]	$\pm 0.5^\circ$C	0°C to 70°C	min/max	unknown
	$\pm 2.0^\circ$C	-55°C to 125°C	min/max	unknown
SMT160-30 [22]	$\pm 0.7^\circ$C	-30°C to 100°C	min/max	wafer-level, 1 point
	$\pm 1.2^\circ$C	-45°C to 130°C	min/max	wafer-level, 1 point
ADT7301 [23]	$\pm 1.0^\circ$C	0°C to 70°C	min/max	unknown
	$\pm 3.0^\circ$C	-40°C to 125°C	min/max	unknown
This work [10]	$\pm 0.03^\circ$C	at 30°C	$\pm 3\sigma$ of 24 samples	after packaging, 1 point
	$\pm 0.1^\circ$C	-50°C to 125°C	$\pm 3\sigma$ of 24 samples	after packaging, 1 point

sensitivity is 0.03 °C/V, which is a tenfold improvement over previous work [5]. This can be attributed to the supply-insensitive bias circuit and the fully differential circuitry. A performance summary is given in Table I.

Table II compares the achieved performance with previous work [3]–[5]. Since most work in the field of smart temperature sensors is done in industry, the specifications of four leading commercial sensors have also been included [20]–[23]. Our measured inaccuracy in the range −55 °C to 125 °C is a fivefold improvement over the highest performance published to date.

VII. CONCLUSION

A CMOS smart temperature sensor with integrated second-order $\Sigma\Delta$ ADC has been presented. The sensor was designed to achieve an overall inaccuracy of ± 0.1 °C.

The design philosophy was to reduce all temperature errors resulting from circuit nonidealities to the ± 0.01 °C level. Errors due to offset were reduced by a combination of correlated double-sampling and system-level chopping in the $\Sigma\Delta$ modulator, and chopping in the bias circuit. A special bias circuit was used to make the sensor insensitive to variations in the current gain of the substrate bipolar transistor used, and to variations in the supply voltage. Mismatch-related errors were eliminated by means of dynamic element matching. Curvature, finally, was corrected for by using a temperature-dependent reference and a slightly nonlinear decimation filter. Spread of the base-emitter voltage of the bipolar transistors is then the only remaining significant error source. This error is trimmed out based on a calibration at one temperature, by means of a high-resolution trimming circuit based on a $\Sigma\Delta$ current DAC.

The realization in 0.7 μm CMOS meets the target of ± 0.1 °C over the full temperature range of −55 °C to 125 °C. This is, to date, the highest reported accuracy for this class of temperature sensors.

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