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Website: www.blueeyesintelligence.org

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2.	Authors:	Mallesha B. Y	
	Paper Title:	Design and FPGA Implementation of LDPC Decoder using High Level Modeling for WSNs	
	Abstract: Low density parity check (LDPC) codes are error-correcting codes that offer huge advantages in terms of coding gain, throughput and power dissipation in digital communication systems. Error correction algorithms are often implemented in hardware for fast processing to meet the real-time needs of communication systems. However, traditional hardware implementation of LDPC decoders require large amount of resources, rendering them unsuitable for use in energy constrained sensor nodes of wireless sensor networks (WSN). This paper investigates the use of short-length LDPC codes for error correction in WSN. It presents the LDPC decoder designs, implementation, resource requirement and power consumption to judge their suitability for use in the sensor nodes of WSN. Due to the complex interconnections among the variable and check nodes of LDPC decoders, it is very time consuming to use traditional hardware description language (HDL) based approach to design these decoders. This paper presents an efficient automated high-level approach to designing LDPC decoders using a collection of high-level modeling tools. The automated high-level design methodology provides a complete design flow to quickly and automatically generate, test and investigate the optimum (length) LDPC codes for wireless sensor networks to satisfy the energy constraints while providing acceptable bit-error-rate performance. Keywords: Error Correction Coding; Wireless Communication; Wireless Sensor Networks; Digital System. References: 1. R. Gallager, "Low-density parity-check codes," IRE Transactions on Information Theory, vol. 8, pp. 21-28, 1962. 2. S. J. Johnson, "Introducing low-density parity-check codes," University of Newcastle, Australia, 2006. 3. M. Eroz, F. W. Sun, and L. N. Lee, "DVB-S2 low density parity check codes with near Shannon limit performance," International Journal of Satellite Communications and Networking, vol. 22, pp. 269-279, 2004. 4. T. Mohsenin and B. M. Baas, "Split-Row: A reduced complexity, high throughput LDPC decoder architecture," in International Conference on Computer Design, ICCD, San Jose, 2007, pp. 320-325. 5. Darabiha, A. C. Carusone, and F. R. Kschischang, "A bit-serial approximate min-sum LDPC decoder and FPGA implementation," in IEEE International Symposium on Circuits and Systems, ISCAS, Island of Kos, 2006. 6. D. Culler, D. Estrin, and M. Srivastava, "Overview of wireless sensor networks," IEEE Computer, Special Issue in Sensor Networks, vol. 37, pp. 41-49, 2004. 7. C. Buratti, A. Conti, D. Dardari, and R. Verdone, "An Overview on Wireless Sensor Networks Technology and Evolution," Sensors, vol. 9, p. 6869, 2009. 8. M. Tubaishat and S. Madria, "Sensor networks: an overview," IEEE potentials, vol. 22, pp. 20-23, 2003. 9. Akyildiz, T. Melodia, and K. Chowdhury, "A survey on wireless multimedia sensor networks," Computer Networks, vol. 51, pp. 921-960, 2007. 10. S. M. Aziz and D. M. Pham, "Energy Efficient Image Transmission in Wireless Multimedia Sensor Networks," IEEE Communications Letters, vol. 17, pp. 1084 -1087, June 2013.		

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