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Analysis and Comparative Study of Different Parameters of Operational Amplifier Using Bipolar Junction Transistor and Complementary Metal Oxide Semiconductor Using Tanner Tools

Ankit Kapil, Arpan Shah, Rekha Agarwal, Sandhya Sharma

Abstract— Operational amplifier (Op-Amp) is used in linear AC operation and is widely used in electronic industry. What follows are two operational amplifier designs using bipolar junction transistor (BJT) technology and metal oxide field effect transistor (CMOS) technology. Presented designs will focus on the characteristics of both BJT and CMOS.BJT invented in 1940's and CMOS came in 1960's and became popular due to low power because it draws current when switching states. In this analysis I will cover various aspects of an op-amp like power consumption, offset voltage for small signal and large signal mode, input bias current, input offset current, gain and frequency response, maximum and minimum voltage swing, slew rate etc. Operational Amplifier are important building blocks for a wide range of electronic circuits. They used in many linear, non-linear and frequency-dependent circuits so they are most widely used electronic device ,being used in a vast array of consumer, Industrial and Scientific devices-MOS amplifiers can be operated with power supplies down to 1.5 to 2.0 volts. This is using now a days in several advanced technologies like cell phones, smart phones ,I-pod and many more because it is many advantageous from electronic industry point of view. In my work I will cover the following points.

1. I will analyze and compare the different parameters of Op-amp using BJT and CMOS using tanner tools.

2. Different waveforms will be finding out by manipulating different parameters in the circuit design and mathematical calculation and comparison will be done.

3. At last all the results of different parameters which is obtained by different simulations using programming on T-Spice window will be summarized in a table then conclusion will be presented.

Keywords– Op-amp, voltage swing, offset voltage, bias current, offset current, slew rate, power dissipation, gain and frequency response.

I. INTRODUCTION

Measuring the appropriate signals directly on the IC itself requires extreme mechanical and electrical measurement precision and is limited to specific types of measurements so Computer programs that simulate the performance of an electronic circuit provide a simple, cost effective means of confirming the intended operation prior to the circuit construction and of verifying new ideas that could lead to improved circuit performance. In this paper first of all I would like to give an brief overview of tanner tools which actually I used for my work for simulation and designing purposes then I will present the different parameter results of BJT and CMOS by Showing different simulation results and the mathematical calculation which I approached here.

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Ankit Kapil, Student, Suresh Gyan Vihar University, Jaipur, India.
Arpan Shah, Student, Suresh Gyan Vihar University, Jaipur, India.
Rekha Agarwal, Asst. Prof. , Suresh Gyan Vihar University, Jaipur, India.
Sandhya Sharma, Asso. Prof., Suresh Gyan Vihar University, Jaipur, India.

II. EDA TOOL

Objectives of the Tool:

1. To develop an understanding of design and simulation of analog and digital logic circuits.
2. To get a basic understanding of layout of electronic circuits.
3. We will use Tanner tools for design and simulation.
4. This presentation introduces us to Tanner tools.
5. Analog and Transient Waveforms can be easily understood.

Introduction to Tanner Tools:-

1. Design is carried out with the help of SPICE.
2. SPICE-Simulation Program with Integrated- Circuit Emphasis.
3. It is basically used to analyze microelectronic circuits.
4. With the help of this we can analyze no of parameters which makes it very useful.
5. It is manufactured by Microsim Corporation for commercial purposes.

III. TYPES OF ANALYSIS THAT CAN BE PERFORMED

Three basic types of analysis are:

1. DC ANALYSIS
2. TRANSIENT ANALYSIS
3. AC ANALYSIS

Some other types of analysis are:

1. SENSITIVITY ANALYSIS
2. TEMPERATURE ANALYSIS
3. NOISE ANALYSIS
4. FOURIER ANALYSIS

IV. CIRCUIT DESCRIPTION AND RESULTS

A detailed analysis of the 741 op-amp circuit:

Here first of all I will take the detailed circuit of 741 Op-amp which is shown below in which two power supplies i.e. +Vcc and –Vee, a coupling capacitor Cc, 11 resistors named R1 to R11, 10 PNP and 15 NPN transistors with their respective parameters are taken.

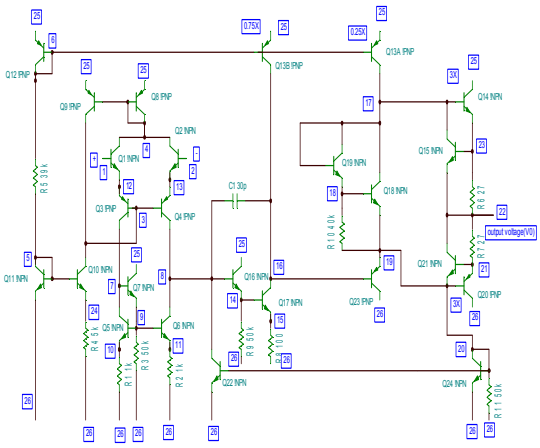

Figure 1.1 741 Op-amp circuit.

A detailed circuit schematic of the 741 op amp which I have used in all my analysis consists five main parts:

1. The bias current
2. The input gain stage
3. The second gain stage
4. The output buffer and
5. The short-circuit protection stage

Now I will present different parameters of Opamp with their respective waveform and mathematical calculations

1. DC Analysis of 741 Op-amp:

A DC operating-point analysis will provide us with some insight into the DC behavior of all the transistors in the Op-amp circuit for grounded inputs, in case such insight is needed. DC sweep so that the input differential voltage is varied between the limits of the two power supplies. after the submission to Spice we refine the sweep range to vary between -400 micro volts to -200 micro volts

2. Transient analysis of 741 Op-amp:

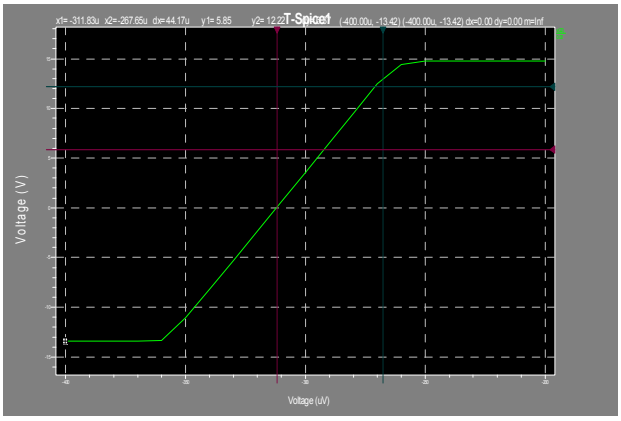

Figure 1.2 Large-signal differential-input transfer characteristic for the 741 Op-amp circuit. The input common-mode voltage level is set to 0.

3. Output voltage swing:

Linear region is from -360 micro volts to -268 micro volts this corresponds to maximum output voltage swing bounded from -13.2 volts to +13.2 volts.

DC gain = output voltage swing / input voltage swing

= 13.2 volts - (-13.2 volts) / -268 micro volts – (-360 micro volts)

= 26.4 volts / 92 mV

= +287 kv/v

4. DC Offset voltage:

Here the transfer characteristics of this amplifier cross the 0v output axis somewhere between -320 micro volts to -310 micro volts. A closer look and careful look using probe indicated that the crossover point occurs at **-314.1** micro volts.

5. Input bias current:

NAME	EV+	EV-
V-SOURCE	1.571E-04	1.571E-04
I-SOURCE	3.440E-08	3.456E-08

So from the above description we know that the current at EV+ source is -34.40nA and at the EV- it is equal to -34.56nA. So the input bias current can be calculated as

$$I_B = ((-34.40nA) + (-34.56nA)) / 2$$

$$I_B = 34.48nA$$

6. Input offset current:

The input offset current can be calculated with the help of difference of two currents.

$$I_{OS} = (-34.40nA) - (-34.56nA)$$

$$I_{OS} = 0.16nA$$

7. Power dissipation:

The total power dissipation can be calculated by **P=V*I**. Here current at Power supply is from +15 volts to -15 volts that is equal to 30 volts and current at Vcc is 1.841E-03 so power can be calculated as:

Power dissipation =(Vcc x current at Vcc) 55.2mW

8. Gain and frequency response of the 741 Op-amp:

The low frequency current drawn by the op-amp was found to be

FREQUENCY	Im (EV+)	Im (EV-)
1.000E-01	2.766E-07	2.732E-07

On the simulation of this Spice deck W-editor give the following response.

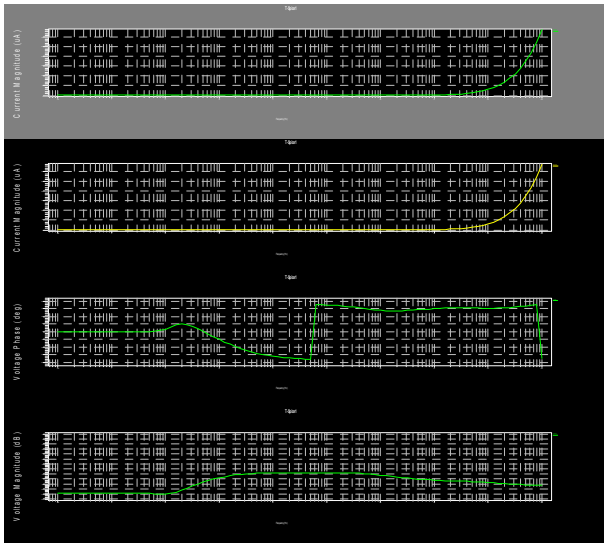

Figure 1.3 Frequency and phase response of the 741 op-amp.

9. Slew rate of the 741 Op-amp:

Slew rate limiting is an important attribute of op-amp behavior and usually limits the high-frequency operation of op-amp circuits. For this we can connect the op-amp in a unity gain configuration and apply a large voltage pulse to its input so as to revel both its positive going and negative going slew rates. The waveform is

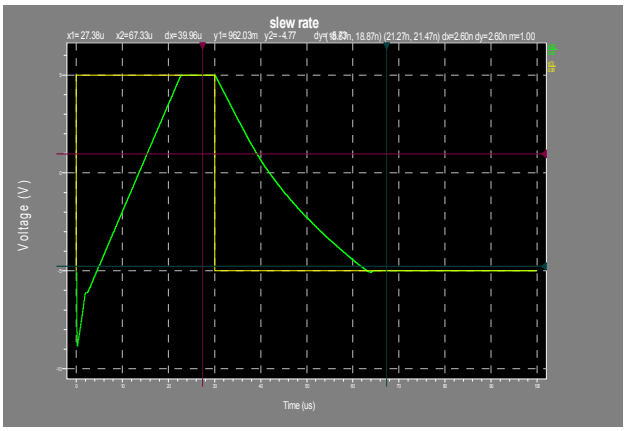

Figure 1.4 Input and Output transient voltage waveforms of the 741 op-amp circuit connected in a unity-gain on figuration. Both the positive-going and negative-going slew rate limits of the op-amp are evident from these results.

Positive going slew rate is 0.55V/Microsecond
Negaive going slew rate is 0.39V/Microsecond

V. CIRCUIT DESCRIPTION AND RESULTS

Detailed analysis of cmos op-amp circuit:

A detailed circuit schematic of the 5µm CMOS op amp which I have used in all my analysis is shown in figure 5.8. Here we show a two stage CMOS op-amp circuit with the transistor geometries shown in the below table:

S.NO	Transistor	W / L Ratio
1.	M1	120 / 8
2.	M2	120 / 8
3.	M3	50 / 8
4.	M4	50 / 10
5.	M5	150 / 10
6.	M6	100 / 10
7.	M7	150 / 10
8.	M8	150 / 1

Table 2.1 Transistor geometries for the CMOS Op-amp circuit.

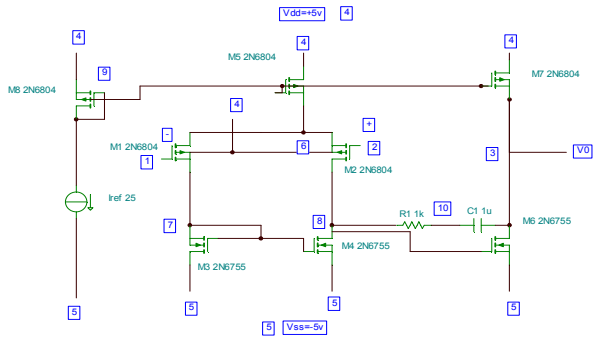

Figure 2.1 Op-amp circuit using 5µm CMOS.

Now we will find out and calculate the same parameters of the CMOS Op-amp and then will compare all the calculated parameters with the parameters that found out for the 741 op-amp. In particular, we consider that each MOSFET is modeled after the transistors found in the 5µm CMOS process at Bell Northern Research (BNR).

DC analysis of CMOS Op-amp:

The first analysis requested is a DC sweep of the input differential voltage Vd between the two power supply limits with the input common-mode level Vcm set to 0 V; it results in the figure 2.1

Transfer character analysis:

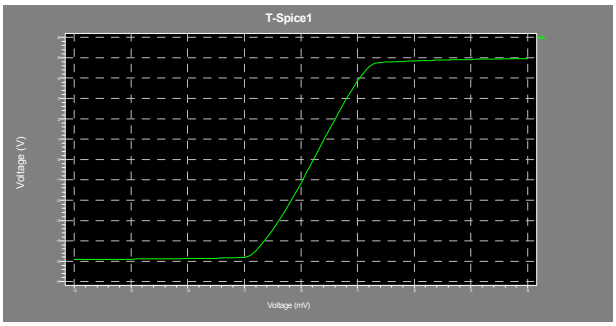

Figure 2.2 Large-signal differential-input transfer characteristic of the CMOS op-amp circuit. The input common-mode voltage level is set to 0v.

3. Output voltage swing:

Linear region is from -0.9 mV to +1.2 mV this corresponds to maximum output voltage swing bounded from -4.40V to +4.54V.

DC gain = output voltage swing / input voltage swing
= 4.54 volts - (-4.40 volts) / 1.2mV – (0.9 mV)
= 8.94 volts / 21.0 mV
= +4.257 kv/v

4. DC Offset voltage:

It is the voltage actually where output voltage tends to zero. Here the transfer characteristics of this amplifier cross the 0v output axis somewhere between -215 micro volts to -225 micro volts. A closer look and careful look using probe indicated that the crossover point occurs at **-220.0** micro volts.

5. Input bias current:

Voltage controlled voltage sources

NAME	EV+	EV-
V-SOURCE	1.100E-04	1.100E-04
I-SOURCE	0.000E-08	0.000E-08

So from the above description we know that the current at EV+ source is 0.000 nA and at the EV- it is equal to 0.000 nA. So the input bias current can be calculated as

$$I_B = 0.000E\text{-}08 \text{ nA}$$

6. Input offset current:

The input offset current can be calculated with the help of difference of two currents. Since here input bias current is 0 nA so input offset current is also 0 nA

$$I_{OS} = 0.000E\text{-}08 \text{nA}$$

7. Power dissipation:

The total power dissipation can be calculated by **P=V*I**. Here current at Power supply is from +5 volts to -5 volts that is equal to 10 volts and current at Vss is 8.061E-05 so power can be calculated as:

Power dissipation = (Vdd x current at Vdd)
= 0.80 mW

8. Gain and frequency response of the 5µm C-MOS Op-amp:

We can carry the small-signal analysis over to the frequency domain and have Spice compute the differential magnitude and phase response of the Op-amp. First the input differential excitation should be changed to include an AC voltage component. 1v amplitude is commonly chosen for the input signal because the output voltage then directly represents the transfer function of the circuit.

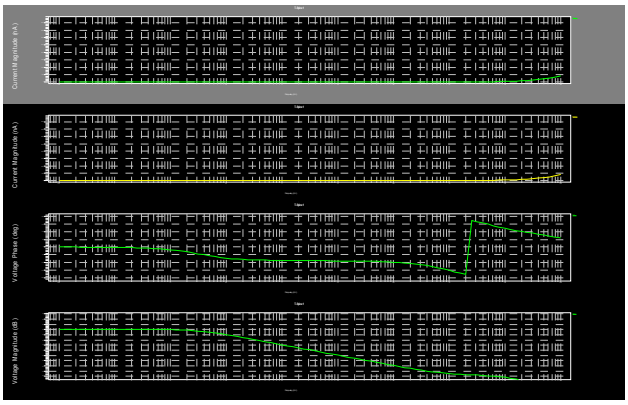

Figure 2.3 Frequency and gain response of 5um CMOS Op-amp.

10. Slew rate of the 5um C-MOS op-amp:

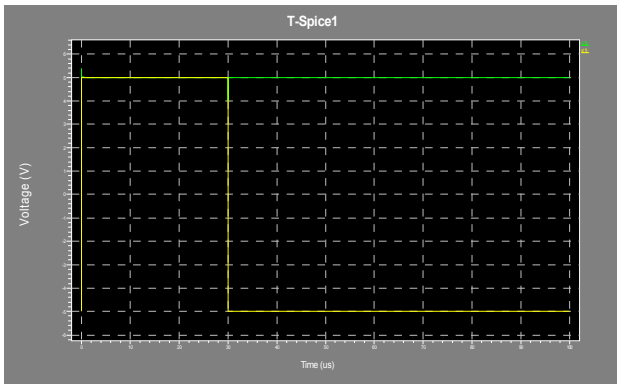

Figure 2.4 Slew rate response of 5um CMOS Op-amp.

5µm CMOS can be split in two separate part for both input and output transient voltage waveform as:

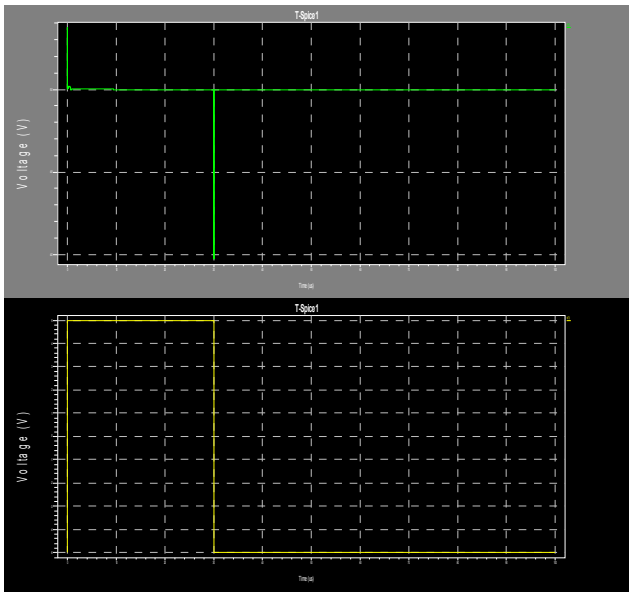

Figure 2.5 Separate responses of input and output waveforms.

VI. RESULTS

The mathematical comparison between 741 op-amp and C-MOS op-amp can be described as follows:

PARAMETERS	741 OP-AMP	C-MOS OP-AMP
1. Linear Region	-360 milli volts to -268 milli volts	-0.9 milli volts to +1.2 milli volts
2. Output Voltage Swing	-13.2 volts to +13.2 volts	-4.40 volts to +4.54volts
3. Dc Gain	+287 kv/v	+4.257 kv/v
4. DC Offset Voltage	-314.1 microvolts	-220.0 microvolts
5.Iinput Bias Current	-34.48 nano ampere	-34.48 nano ampere
6.Iinput Offset Current	0.16 nano ampere	0 nano ampere
7. Power dissipation	55.2 milli watt	0.80 milliwatt
8. Gain and Frequency response	at 1 khz freq. i_m(ev+) = 0.0276 na i_m(ev-) = 0.0232 na	at 1 khz freq. i_m(ev+) = na i_m(ev-) = na
9. slew rate	positive = +0.55 v/microseconds negative = -0.39 v/microseconds	positive = +0.4 v/picoseconds negative = - 0.21 v/pic

Table 2.2 Comparison table of different parameters between 741 BJT and 5um C-MOS Op-Amp.

VII. CONCLUSION

The future implications of the project are very wide since Op-amp is a device which is now a days using in many applications The project I have undertaken can be used as a reference or as a base for realizing the op-amp circuits so it can be further implemented in other projects of greater level such as reduction in power using miller capacitance technique, to reduce input bias current, to increase the slew rate etc. Since in this project I worked on the Op-amp using BJT and C-MOS both I found that somewhere the application of BJT is good due to its some of parameters good responses like current controlling and speed but I also found that somewhere or infact in many applications C-MOS Op-amp is quite good over BJT because of its very less power consumption which is one of the most important feature as far as industries concern and for practical uses and anther major feature is its slew rate which is also very fast than BJT its offsets current is also very much reduced and gain and frequency response is quite efficient and smooth over BJT. So overall C-MOS OP-amp now a days going to replace most of BJT Op-amps but still due to some good characteristics of BJT's in some applications we need BJT's Op-amp. Therefore due to the importance of both the devices we switched on the new technology which is very

efficient and well known now days that is Bi-cmos technology. So we can further work on lots of researches in this field in which we can try to improve all the parameters further by utilizing the advantage of both the previous research results and can study further to enhance the capacity and efficiency of Operational amplifier. So it can play more important and advantageous role in electronics.

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ANKIT KAPIL, Student of M.Tech Final year in Suresh Gyan Vihar University, Jaipur. I have completed my B.E degree in 2009 from Rajasthan University. I am currently working in the VLSI field.

ARPAN SHAH, Student of M.Tech Final year in Suresh Gyan Vihar University, Jaipur. I have completed my B.E degree in 2008 from Rajasthan University. I am currently working in the VLSI field.

REKHA AGARWAL, M.TECH degree in VLSI from Banasthali Vidhyapith, Jaipur. She is currently working as Asst. Prof. in Dept. of Electronics and Communication Engg. In Suresh Gyan Vihar University, Jaipur.

SANDHAYA SHARMA, M.TECH degree in Digital and wireless Communication from MBM, Jodhpur. She is currently working as Asso. Prof. in Dept. of Electronics and Communication Engg. In Suresh Gyan Vihar University, Jaipur.