

# EE5390: Analog Integrated Circuit Design

## Introduction

Nagendra Krishnapura

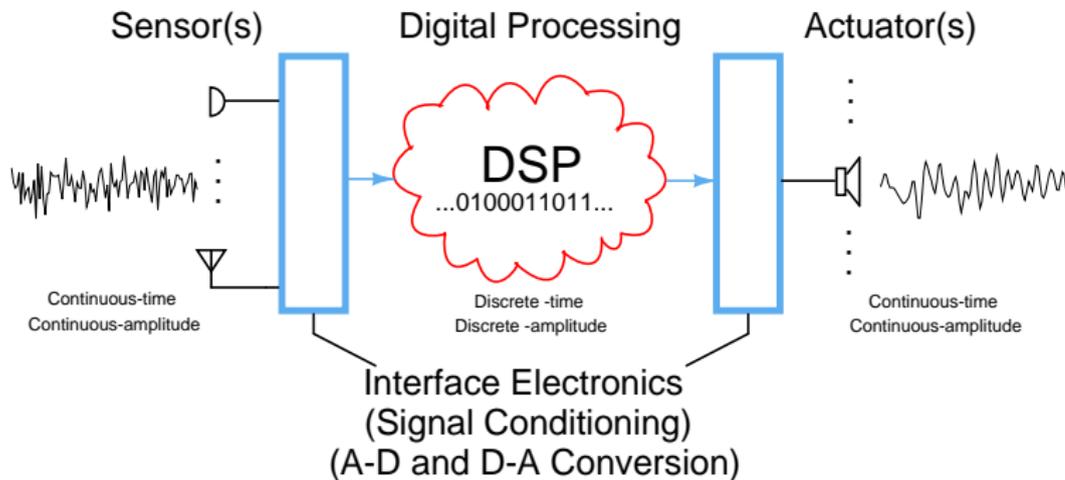
Department of Electrical Engineering  
Indian Institute of Technology, Madras  
Chennai, 600036, India

6 Jan. 2010

- <http://www.ee.iitm.ac.in/~nagendra/EE539/201001/courseinfo.html>
- TAs: P. Rakesh, Kunal Karanjkar
- E Slot (Tue. 1100-1150, Wed. 1000-1050, Thu. 0800-0850, Fri. 1400-1450)

Check it regularly for recorded lectures, assignments, and references

# Modern signal processing systems

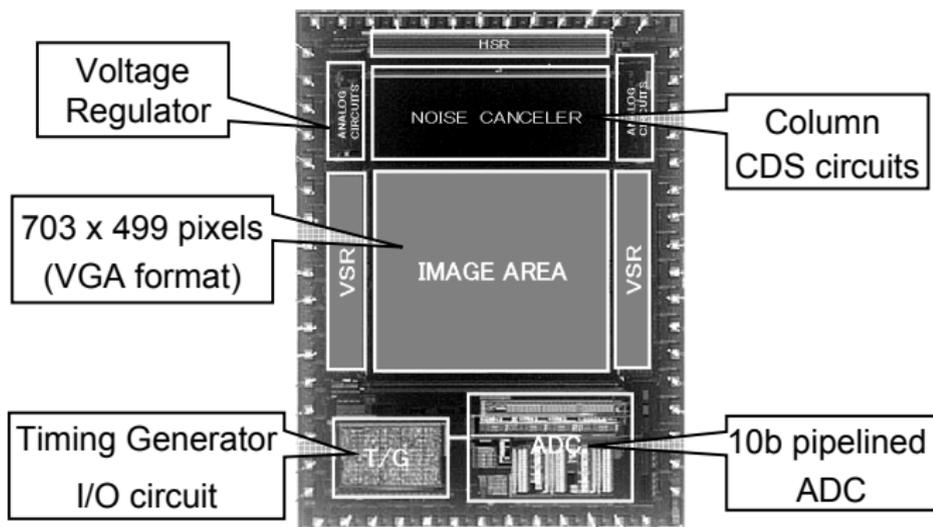


# Analog circuits in modern systems on VLSI chips

- Analog to digital conversion
- Digital to analog conversion
- Amplification
- Signal processing circuits at high frequencies
- **Power management-voltage references, voltage regulators**
- **Oscillators, Phase locked loops**

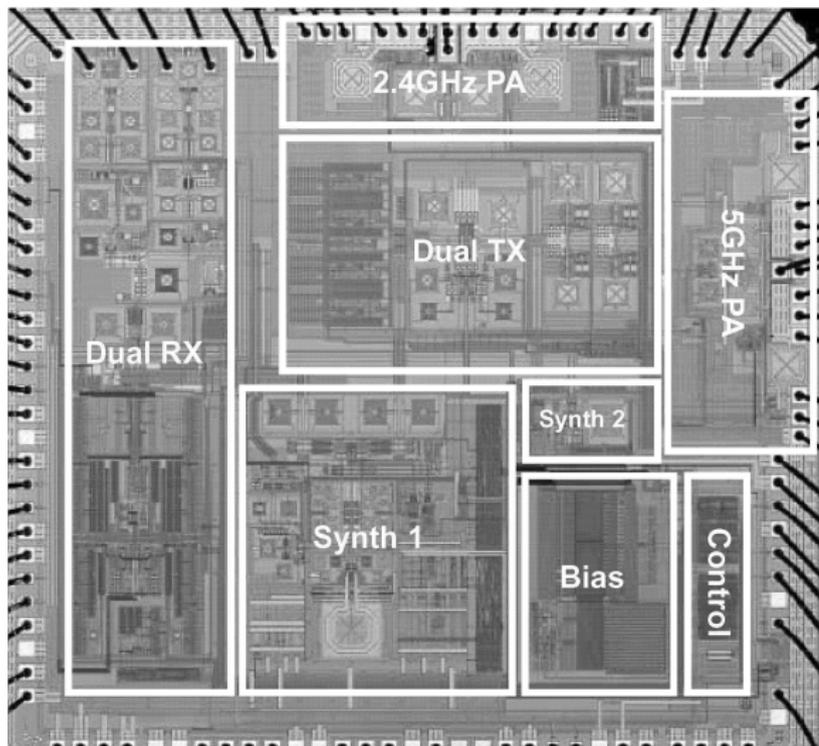
The last two are found even on many “digital” ICs

## Chip Micrograph

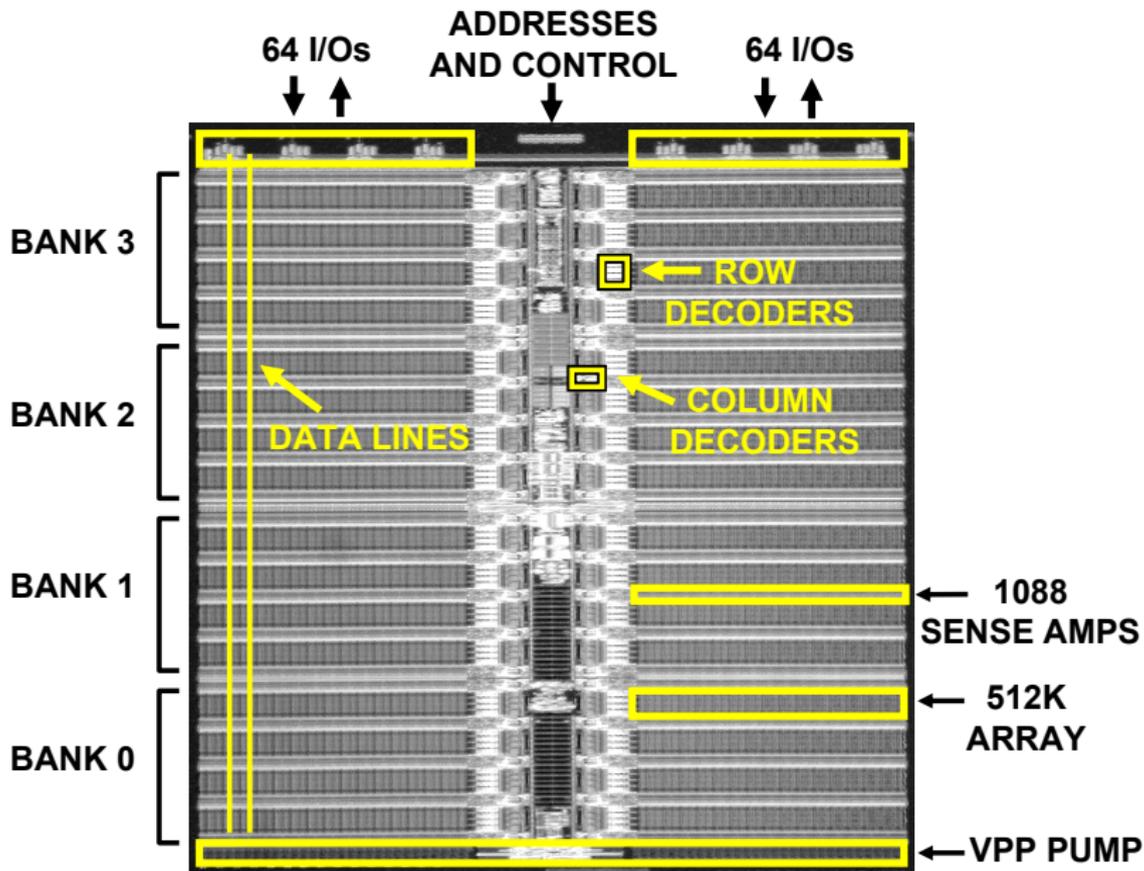


Chip size: 4.74mm x 6.34mm

## Die Micrograph



# DRAM[ISSCC 2004]



# Analog IC design in India

- Many companies starting analog centers
- Multinationals-TI, National, ST, ADI etc.
- Indian start ups-Cosmic, Manthan, Karmic, Sankalp etc.
- Big demand for skilled designers
- Interesting and profitable activity 😊

Learn to design negative feedback circuits on CMOS ICs

- Negative feedback for controlling the output
- Amplifiers, voltage references, voltage regulators, biasing
- Phase locked loops

# Course prerequisites

- Circuit analysis-small and large signal
- Laplace transforms, frequency response, Bode plots, Differential equations
- Opamp circuits
- Single transistor amplifiers, differential pairs

EE542 (Analog Electronic Circuits)/EC201 (Analog Circuits)

# Course contents-Negative feedback amplifiers

- Amplifiers using negative feedback
- Stability, Frequency compensation
- Negative feedback circuits using opamps
- Opamp macromodel

# Course contents-Opamps on CMOS ICs

- Components available on a CMOS integrated circuit
- Device models-dc small signal, dc large signal, ac small signal, mismatch, noise
- Single stage opamp
- Cascode opamps
- Two stage opamp with miller compensation

# Course contents-Fully differential circuits

- Differential and common mode half circuits, common mode feedback
- Fully differential miller compensated opamp
- Fully differential feedforward compensated opamp

# Course contents-Phase locked loop

- Frequency multiplication using negative feedback
- Type I, type II loops
- Oscillators
- Phase noise basics
- PLL noise transfer functions

# Course contents-Design of opamps

- Single stage opamp
- Folded, telescopic cascode opamps
- Two stage opamp
- Fully differential opamps and common mode feedback
- Applications: Bandgap reference, constant  $g_m$  bias generation

# Course contents-Applications

- Bandgap reference
- Constant current and constant gm bias generators
- Continuous-time filters
- Switched capacitor filters

# Design versus Analysis

- Design: Create something that doesn't yet exist
- Analysis: Analyze something that exists

# To be able to design

- Knowing analysis is necessary, not sufficient
- Multiple ways of looking at building blocks
- Trial and error approaches
- Intuitive thinking/understanding
- Curiosity
- Open mind
- Thoroughness

- Intuitive thinking **is not** sloppy thinking!
- Relate problems to other problems already solved
- Use boundary conditions, dimension checks etc.
- Build your intuition
  - Solve many problems
  - Think about why the answer is what it is
  - Come up with the form of the solution before applying full blown analysis

# Circuit analysis

- Nodal analysis-Kirchoff's Current Law (KCL) at each node
- Solve  $N$  simultaneous equations for an  $N$  node circuit
- Mesh analysis-Kirchoff's Voltage Law (KVL) around each loop
- Solve  $M$  simultaneous equations for a circuit with  $M$  independent loops

# Nodal analysis

$$\begin{aligned}i_{11}(\bar{v}) + i_{12}(\bar{v}) + \dots + i_{1N}(\bar{v}) &= i_1 \\i_{21}(\bar{v}) + i_{22}(\bar{v}) + \dots + i_{2N}(\bar{v}) &= i_2 \\&\vdots \\i_{N1}(\bar{v}) + i_{N2}(\bar{v}) + \dots + i_{NN}(\bar{v}) &= i_N\end{aligned}$$

- $i_{kl}$ : Current in the branch between nodes  $k$  and  $l$
- $i_{kk}$ : Current in the branch between node  $k$  and ground
- $v_k$ : Voltage at node  $k$ ;  $\bar{v} = [v_1 v_2 \dots v_N]^T$
- $i_k$ : Current source into node  $k$

$i_{kl}$  can be a nonlinear function of  $\bar{v}$

# Nodal analysis—Linear circuits

$$\begin{aligned}g_{11}v_1 + g_{12}v_2 + \dots + g_{1N}v_N &= i_1 \\g_{21}v_1 + g_{22}v_2 + \dots + g_{2N}v_N &= i_2 \\&\vdots \\g_{N1}v_1 + g_{N2}v_2 + \dots + g_{NN}v_N &= i_N\end{aligned}$$

- $g_{kl}$ : Conductance between nodes  $k$  and  $l$
- $g_{kk}$ : Conductance between node  $k$  and ground
- $v_k$ : Voltage at node  $k$
- $i_k$ : Current source into node  $k$

# Nodal analysis—Independent voltage source

$$\begin{array}{rcc} & \vdots & \\ \cancel{g_{k1}v_1} + \cancel{g_{k2}v_2} + \dots + \cancel{g_{kN}v_N} & = & i_k \quad \text{node } k \\ & \vdots & \\ v_k & = & V_o \quad \text{node } k \end{array}$$

- Ideal voltage source  $V_o$  connected to node  $k$

# Nodal analysis—Controlled voltage source

$$\begin{array}{rcl} & \vdots & \\ \mathcal{G}_{k1}v_1 + \mathcal{G}_{k2}v_2 + \dots + \mathcal{G}_{kN}v_N & = & i_k \quad \text{node } k \\ & \vdots & \\ v_k - kv_I & = & 0 \quad \text{node } k \end{array}$$

- Voltage controlled voltage source  $v_k = kv_I$  driving node  $k$

# Nodal analysis—Controlled voltage source

$$g_{k1}v_1 + g_{k2}v_2 + \dots + g_{kI}v_I + \dots + g_{kN}v_N = i_k \quad \text{node } k$$

$$g_{k1}v_1 + g_{k2}v_2 + \dots + \frac{v_k}{R_m} + \dots + g_{kN}v_N = i_k \quad \text{node } k$$

$$g_{l1}v_1 + g_{l2}v_2 + \dots + g_{lK}v_K + \dots + g_{lN}v_N = i_l \quad \text{node } l$$

$$g_{l1}v_1 + g_{l2}v_2 + \dots - \frac{v_k}{R_m} + \dots + g_{lN}v_N = i_l \quad \text{node } l$$

- Current controlled voltage source  $v_k = R_m i_{kl}$  driving node  $k$

# Nodal analysis—Controlled current source

$$\begin{aligned}g_{k1}v_1 + g_{k2}v_2 + \dots + g_{kl}v_l + \dots + g_{kN}v_N &= i_k + g_m v_l \\g_{k1}v_1 + g_{k2}v_2 + \dots + g_{kl}v_l - g_m v_l + \dots + g_{kN}v_N &= i_k\end{aligned}$$

- Current controlled voltage source  $i_0 = g_m v_l$  driving node  $k$

# Nodal analysis—Ideal opamp

$$\begin{array}{rcl} & \vdots & \\ \cancel{g_{m1}v_1} + \cancel{g_{m2}v_2} + \dots + \cancel{g_{mN}v_N} & = & i_m \quad \text{node } m \\ & \vdots & \\ v_k - v_l & = & 0 \quad \text{node } m \end{array}$$

- Ideal opamp with input terminals at nodes  $k$ ,  $l$  and output at node  $m$

# Nodal analysis—solution

$$\begin{bmatrix} g_{11} & g_{12} & \cdots & g_{1N} \\ g_{21} & g_{22} & \cdots & g_{2N} \\ \vdots & & & \\ g_{N1} & g_{N2} & \cdots & g_{NN} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_N \end{bmatrix} = \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_N \end{bmatrix}$$
$$G\bar{v} = \bar{i}$$
$$v = G^{-1}\bar{i}$$

- $g_{kl}$ : Conductance between nodes  $k$  and  $l$
- $g_{kk}$ : Conductance between node  $k$  and ground
- $v_k$ : Voltage at node  $k$
- $i_k$ : Current source into node  $k$
- Modified terms for voltage sources or controlled sources
- Matrix inversion yields the solution

# Nodal analysis—solution

$$V_k = \frac{\begin{vmatrix} g_{11}g_{12} \dots i_1 \dots g_{1N} \\ g_{21}g_{22} \dots i_2 \dots g_{2N} \\ \vdots \\ g_{N1}g_{N2} \dots i_N \dots g_{NN} \end{vmatrix}}{\begin{vmatrix} g_{11}g_{12} \dots g_{1k} \dots g_{1N} \\ g_{21}g_{22} \dots g_{2k} \dots g_{2N} \\ \vdots \\ g_{N1}g_{N2} \dots g_{Nk} \dots g_{NN} \end{vmatrix}}$$

- Cramer's rule can be used for matrix inversion

# Circuits with capacitors and inductors

$$\begin{bmatrix} Y_{11}(s) & Y_{12}(s) & \dots & Y_{1N}(s) \\ Y_{21}(s) & Y_{22}(s) & \dots & Y_{2N}(s) \\ & & \vdots & \\ Y_{N1}(s) & Y_{N2}(s) & \dots & Y_{NN}(s) \end{bmatrix} \begin{bmatrix} V_1(s) \\ V_2(s) \\ \vdots \\ V_N(s) \end{bmatrix} = \begin{bmatrix} I_1(s) \\ I_2(s) \\ \vdots \\ I_N(s) \end{bmatrix}$$
$$\mathbb{Y}(s)\bar{V}(s) = \bar{I}(s)$$
$$\bar{V}(s) = \mathbb{Y}^{-1}\bar{I}(s)$$

- Conductances  $g_{kl}$  replaced by admittances  $Y_{kl}(s)$
- Roots of the determinant of  $\mathbb{Y}(s)$  are system poles

# Laplace transform analysis for linear systems

Input      Output

$$X(s) \quad H(s)X(s)$$

$$e^{st} \quad H(s)e^{st}$$

$$X(j\omega) \quad H(j\omega)X(j\omega)$$

$$e^{j\omega t} \quad H(j\omega)e^{j\omega t}$$

$$\cos(\omega t) \quad |H(j\omega)| \cos(\omega t + \angle H(j\omega)) \quad (\text{Steady state solution})$$

- Linear time invariant system described by its transfer function  $H(s)$
- $H(s)$  is the laplace transform of the impulse response
- $s = j\omega$  represents a sinusoidal frequency  $\omega$

# Laplace transform analysis for linear systems

Transfer function  $H(s)$  (no poles at the origin)

$$\begin{aligned} H(s) &= A_{dc} \frac{1 + b_1 s + b_2 s^2 + \dots + b_M s^M}{1 + b_1 s + b_2 s^2 + \dots + b_N s^N} \\ &= A_{dc} \frac{\prod_{k=1}^M 1 + s/z_k}{\prod_{k=1}^N 1 + s/p_k} \end{aligned}$$

Single pole at the origin

$$H(s) = \frac{\omega_u}{s} \frac{\prod_{k=1}^M 1 + s/z_k}{\prod_{k=2}^N 1 + s/p_k}$$

- All poles  $p_k$  must be in the left half plane for stability

# Frequency and time domain analyses

## Frequency domain

- Algebraic equations-easier solutions
- Only for linear systems

## Time domain

- Differential equations-more difficult to solve
- Can be used for nonlinear systems as well
- Piecewise linear systems occur quite frequently (e.g. saturation)

# Bode plots

- Sinusoidal steady state response characterized by  $|H(j\omega)|$ ,  $\angle H(j\omega)$
- Bode plot: Plot of  $20 \log |H(j\omega)|$ ,  $\angle H(j\omega)$  versus  $\log \omega$  approximated by straight line segments
- Good approximation for real poles and zeros

Very powerful tools, indispensable for complex calculations, but GIGO!

- Matlab: System level analysis (Frequency response, pole-zero, transfer functions)
- Spice: Circuit analysis
- Maxima: Symbolic analysis

# References: Recorded lectures

- EC201: Analog Circuits
- EE539: Past years' lectures

URL: <http://www.ee.iitm.ac.in/~nagendra/videolectures/>

# References

- Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, August 2000.
- Hayt and Kemmerly, *Engineering Circuit Analysis*, McGraw Hill, 6/e.
- B. P. Lathi, *Linear Systems and Signals*, Oxford University Press, 2 edition, 2004.
- Sergio Franco, *Design with operational amplifiers and analog ICs*, Tata McGraw Hill.
- H. Takahashi et al., "A 3.9  $\mu\text{m}$  pixel pitch VGA format 10b digital image sensor with 1.5-transistor/pixel," *IEEE International Solid-State Circuits Conference*, vol. XVII, pp. 108 - 109, February 2004.
- M. Zargari et al., "A single-chip dual-band tri-mode CMOS transceiver for IEEE 802.11a/b/g WLAN," *IEEE International Solid-State Circuits Conference*, vol. XVII, pp. 96 - 97, February 2004.
- K. Hardee et al. "A 0.6V 205MHz 19.5ns tRC 16Mb embedded DRAM," *IEEE International Solid-State Circuits Conference*, vol. XVII, pp. 200 - 201, February 2004.