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1.

Authors: Rizawan N. Shaikh,Ramesh Kumar K. R, Ramachandra C. G

Paper Title: Prototype Model of Multi-Load AGV for Material Supply in Manufacturing System

Abstract: Here we aim to build a model of the multi load material supply system which is the hybrid of AGV (Automated guided vehicle) and AS/RS (Automated storage/Retrieval system) system. The AGV base provides movement in the manufacturing facility and AS/RS provides storage of the material. The machine can be designed depending on the AGV load caring capacity and variety of material need to be carried. Depending upon number of variety of products and requirements, compartment can be increased or decreased. One of major advantage of this kind of machine in normal AGV is it has high throughput. Since single machine can carry more products hence number of AGVs needed to handle material is less thereby traffic in the manufacturing environment can be decreased and more efficiency in material handling transportation can be achieved. Due to decrease in AGV numbers in manufacturing environment, cost of handling and maintenance them is reduced hence it saves money and increase efficiency.

Keywords: Multi-load Robots, Multi Load AGVs, Revolutionary AGV Design.

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2.

Authors: Sayyan N. Shaikh, Neelakantha V. Londhe

Paper Title: OCR Based Mapless Navigation Method of Robot

Abstract: This paper reviews a method for a robot can locate and track landmarks using segmentation algorithm within proper distance, It extracts text or sign from the landmark and inputs them into the OCR engine for recognition. Simultaneously, a projection analysis of texts or signs of the landmark is conducted, finally by identifying the semanteme of text or signs the robot can find the routes to the destinations automatically. Experiments on the robot model shows that this method can be used to accomplish maples navigation task perfectly in the indoors or customised environment. Being able to navigate with landmarks in real life directly without generating maps or resetting new navigation sign for robots. Specially, this method can be applied in the field of service robots rapidly, which can enhance their adaptability and viability significantly.

Keywords: Mapless navigation, Landmark recognition, OCR, Kohonen Neural Network.

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Authors: Bibin M. C, Premananda B. S

Paper Title: Implementation of UART with BIST Technique in FPGA

Abstract: Asynchronous serial communication is usually implemented by Universal Asynchronous Receiver Transmitter (UART), mostly used for short distance, low speed, low cost data exchange between processor and peripherals. UART allows full duplex serial communication link, and is used in data communication and control

3.	system. There is a need for realizing the UART function in a single or a very few chips. Further, design systems without full testability are open to the increased possibility of product failures and missed market opportunities. Also, there is a need to ensure the data transfer is error proof. This paper targets the introduction of Built-in self test (BIST) and Status register to UART, to overcome the above two constraints of testability and data integrity. The 8-bit UART with status register and BIST module is coded in Verilog HDL and synthesized and simulated using Xilinx XST and ISim version 14.4 and realized on FPGA. The results indicate that this model eliminates the need for higher end, expensive testers and thereby it can reduce the development time and cost. **Keywords:** UART, BIST, Error check, Status register, LFSR. **References:** 1. Naresh, Vatsalkumar and Vikaskumar Patel, "VHDL Implementation of UART with Status Register", in the proceedings of International Conference on Communication Systems and Network Technologies, IEEE Computer Society, 11-13th May 2012, DOI: 10.1109/CSNT.2012.164, pp.750-754. 2. Fang Yi-yuan and Chen Xue-jun, "Design and Simulation of UART Serial Communication Module Based on VHDL", in the proceedings of 3rd International Workshop on Intelligent Systems and Applications (ISA), IEEE, May 2011, DOI: 10.1109/ISA.2011.5873448, pp.1-4. 3. Mohd Yamani Idna Idris, Mashkuri Yaacob and Zaidi Razak, "A VHDL Implementation of UART Design with BIST Capability", in the proceedings of Malaysian Journal of Computer Science, June 2006, Vol. 19(1), pp. 73-86. 4. Dr. Garima Bandhawarkar Wakhle, Iti Aggarwal and Shweta Gaba, "Synthesis and Implementation of UART using VHDL Codes", in the proceedings of International Symposium on Computer, Consumer and Control, IEEE June 2012, DOI: 10.1109/IS3C.2012.10. 5. Norhuzaimin J and Maimun H.H, "The design of high speed UART", in the proceedings of Asia-Pacific Conference on Applied Electromagnetics, APACE 05, IEEE, 20-21st Dec. 2005, DOI: 10.1109/APACE.2005.1607831, pp.5-8. 6. Dr. T.V.S.P.Gupta, Y. Kumari and M. Ashok Kumar, "UART realization with BIST architecture using VHDL", in the proceedings of International Journal of Engineering Research and Applications, February 2013, Vol. 3, Issue 1, ISSN: 2248-9622, pp.636-640. 7. Shikha Kakar, Balwinder Singh and Arun Khosla, "Implementation of BIST Capability using LFSR Techniques in UART", in the proceedings of International Journal of Recent Trends in Engineering, May 2009, Vol 1, No. 3. 8. Sybille Hellebrand, Birgit Reeb and Steffen Tarnick, "Pattern Generation for a Deterministic BIST Scheme", in the proceedings of IEEE/ACM International Conference on Computer-Aided Design, ICCAD-95, Digest of Technical Papers, November 1995, DOI: 10.1109/ICCAD.1995.479997, pp. 88-94. 9. Mahat N.F, "Design of a 9-bit UART module based on Verilog HDL", in the proceedings of 10th IEEE International Conference on Semiconductor Electronics (ICSE), 19-21st Sept. 2012, DOI: 10.1109/SMElec.2012.6417210, pp. 570-573.	**13-17**