Quantum-dot Cellular Automata: Introduction and Experimental Overview

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Abstract

An overview is given of the QCA architecture, along with a summary of experimental demonstrations of QCA devices. Quantum-dot cellular automata (QCA) is a transistorless computation paradigm that addresses such challenging issues as device and power density. The basic building blocks of the QCA architecture, such as AND, OR gates and clocked cells have been demonstrated and will be presented here. The quantum dots used in the experiments are metal islands that are coupled by capacitors and tunnel junctions. An improved design of the cell is presented in which all four dots of the cell are coupled by tunnel junctions. A non-invasive electrometer is presented which improves the sensitivity and linearity of dot potential measurements. The operation of this basic cell is confirmed by an externally controlled polarization change of the cell.

1. Introduction

For almost 40 years integrated circuits produced by the semiconductor industry have obeyed Moore's law, which predicts that the number of devices on each chip will double every 18 months. Adherence to this exponential growth curve has been a monumental task requiring rapid improvements in all aspects of integrated circuit (IC) fabrication to permit manufacturers to both shrink the size of devices, and increase chip size, while maintaining acceptable yields. The engine driving this growth has been the field effect transistor (FET). While the use of FETs has been an incredibly successful circuit paradigm, FETs are still used as current switches much like the mechanical relays used by Konrad Zuse in the 1930s. At gate lengths below 0.05 μm FETs will begin to encounter fundamental effects such as tunneling that make further scaling difficult. In addition, power dissipation will limit the growth of integration. A high-performance chip today dissipates more power per unit area than a typical electric range-top unit. One can argue that each major shift in integrated circuits, from BJTs to FETs, from NMOS to CMOS, was driven by the need to reduce power dissipation. Quantum-dot Cellular Automata (QCA) offers the ultra-low power dissipation and scalability to molecular dimensions that will be necessary when another paradigm shift is needed. Here, instead of fighting the effects that come with feature size reduction, these effects are used to advantage. QCA employs arrays of coupled quantum dots to implement the Boolean logic functions and clocked circuits needed for general purpose computing [1, 2]. The advantage of QCA lies in the extremely high packing densities possible due to the small size of the dots, the simplified interconnection, and the extremely low power-delay product.

A basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. Electrons are able to tunnel between the dots, but cannot leave the cell. If two excess electrons are placed in the cell, Coulomb repulsion will force the electrons to dots on opposite corners. There are thus two energetically equivalent ground state polarizations, as shown in Fig. 1(a), which can be labeled logic "0" and "1". If two cells are brought close together, Coulombic interactions between the electrons cause the cells to take on the same polarization. If the polarization of one of the cells is gradually changed from one state to the other, the second cell exhibits a highly bistable switching of its polarization, shown in Fig. 1(b). In explaining the operation of QCA systems we will begin with unclocked systems. While this approach will not be used in large QCA systems, it

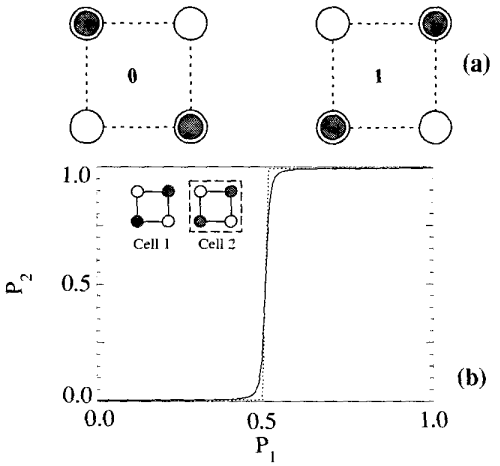


Figure 1. (a) Schematic representation of QCA cells showing the two possible polarizations. (b) Polarization switching in cell 2 as cell 1 is switched.

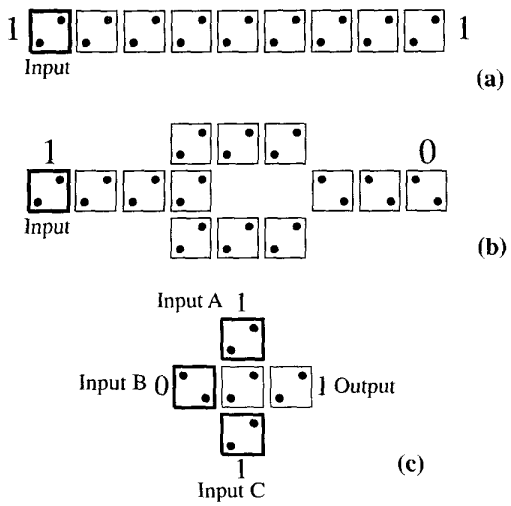


Figure 2. (a) Line of QCA cells. (b) QCA inverter. (c) QCA majority gate.

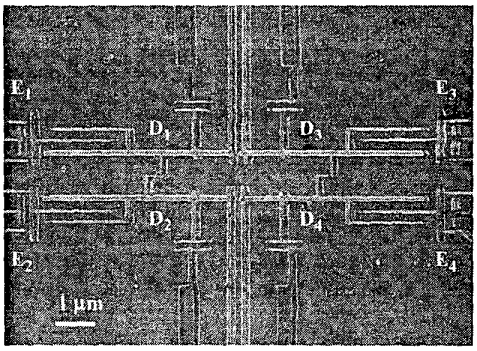
is simple to understand, and was used for the first experimental demonstrations of QCA devices. The simplest QCA array is a line of cells, shown in Fig. 2(a). Since the cells are capacitively coupled to their neighbors, the ground state of the line is for all cells to have the same polarization. In this state, the electrons are as widely separated as possible, giving the lowest possible energy. To use the line, an input is applied at the left end of the line, breaking the degeneracy of the ground state of the first cell and forcing it to one polarization. Since the first and second cell are now of opposite polarization, with two electrons close together, the line is in a higher energy state and all subsequent cells in the line must flip their polarization to reach the new ground state. No metastable state (where only a few cells flip) is possible in a line of cells [3]. A tremendous advantage of QCA devices is the simplified interconnect made possible by this paradigm. Since the cells communicate only with their nearest neighbors, there is no need for long interconnect lines. The inputs are applied to the cells at the edge of the system and the computation proceeds until the output appears at cells at the edge of the QCA array.

Computing in the QCA paradigm can be viewed as computing with the ground state of the system. A computational problem is mapped onto an array of cells by the layout of the cells, where the goal is to make the ground state configuration of electrons represent the solution to the posed problem. In unclocked systems computation becomes a task of applying a set of inputs that put the system into an excited state, and then letting it relax into a new ground state. For each set of inputs a unique system ground state exists that represents the solution for those inputs. The mapping of a combinational logic problem onto a QCA system can be accomplished by finding arrangements of QCA cells that implement the basic logic functions AND, OR, and NOT. An inverter, or NOT, is shown in Fig. 2(b). In this inverter the input is first split into two lines of cells then brought back together at a cell that is displaced by 45° from the two lines, as shown. The 45° placement of the cell produces a polarization that is opposite to that in the two lines, as required in an inverter. AND and OR gates are implemented using the topology shown in Fig. 2(c), called a majority gate. In this gate the three inputs "vote" on the polarization of the central cell, and the majority wins. The polarization of the central cell is then propagated as the output. One of the inputs can be used as a programming input to select the AND or OR function. If the programming input is a logic 1 then the gate is an OR, but if a 0 then the gate is an AND. Thus, with majority gates and inverters it is possible to implement all combinational logic functions.

For practical QCA circuits, clocked control is necessary. In clocked circuits the system is switched smoothly between the ground state corresponding to the old inputs and the state corresponding to the new inputs. Clocking allows cells to be locked in a particular state, performing as a latch. Thus general purpose computing is possible, and in particular, latches make it possible to implement pipelined architectures, as required in all high-performance systems. Clocking of QCA cells is accomplished by switching the cells using a quasi-adiabatic approach [3, 4]. This keeps the system in its instantaneous ground state during switching, which avoids any metastable states and results in very low power dissipation. Quasi-adiabatic switching can be implemented in both semiconductor and metallic QCA systems. In a semiconductor system the barriers between dots are typically controlled by gates, and quasi-adiabatic switching is implemented by applying a clock signal to the gates which modulates the height of the barriers between dots. In metallic QCA systems the barrier between dots is an oxide whose barrier height cannot be modulated. In this case, an additional dot is introduced between the top and bottom dots of a cell. The clock signal is applied to a gate coupled to this central dot to modulate the potential of the dot. Thus the central dot plays the role of the variable barrier between the dots of the cell.

2. Experiment

The experimental work presented is based on a QCA cell using aluminum islands and aluminum-oxide tunnel junctions fabricated on an oxidized silicon wafer. The fabrication uses standard electron beam lithography and dual shadow evaporations to form the islands and



igure 3. SEM micrograph of QCA cell.

tunnel junctions [5]. A completed device is shown in the SEM micrograph of Fig. 4. The area of the tunnel junctions is an important quantity since this dominates island capacitance, determining the charging energy of the island, and hence the operating temperature of the device. For our devices the area is approximately 60 by 60 nm, giving a junction capacitance of 400 aF. These metal islands stretch the definition of a quantum dot, but we will refer to them as such because the electron population of the island is quantized and can be changed only by quantum mechanical tunneling of electrons. The device is mounted on the cold finger of a dilution refrigerator that has a base temperature of 10 mK, and characterized by measuring the conductance through various branches of the circuit using standard ac lock-in techniques. A magnetic field of 1 T is applied to suppress the superconductivity of the aluminum metal. Full details of the experimental measurements are described elsewhere [6-9].

A single, unclocked cell confirms the basic premise of the QCA paradigm: that the switching of a single electron between coupled quantum dots can control the position of a single electron in another set of dots [6, 7]. A simplified schematic diagram of the QCA system is shown in Fig. 4(a). The four-dot QCA cell is formed by two double-dots D1-D2, and D3 - D4, which are coupled by tunnel junctions, and the double-dots are coupled to each other by lithographically defined capacitors C_C. The four individual dots E1-E4 are used as electrometers, and track the electrons moving between D1-D4. The object of the experiment is to show a polarization change in the cell, and this operation is shown in Fig. 4(b) and (c). A differential input voltage V_{IN} (with opposite polarities V_1=–V_2) is applied to the left double-dot, while the gate voltages applied to the right double dot are held constant. Figure 4(b) (solid line) plots the potential of dot D1 as measured by electrometer E1. At V_{IN}=0.5 mV, there is a sharp downward transition corresponding to an electron entering dot D1 from D2.

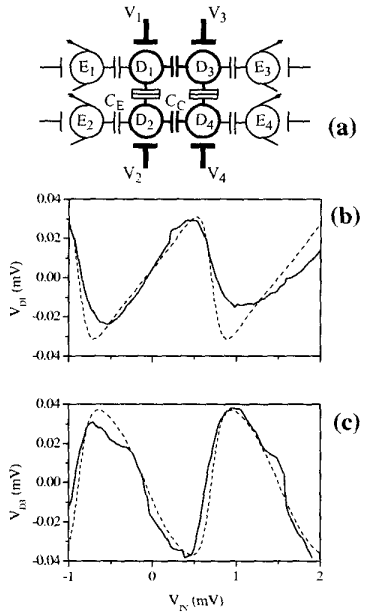


Figure 4. (a) Schematic diagram of QCA cell. (b) Potential on dot D1, experiment: solid line, theory: dashed line. (c) Potential on dot D3.

At the same voltage in Fig. 4(c) there is a sharp upward transition in the potential of D3 (measured by E3), showing that an electron has moved from D3 to D4.

To compare the experimental results with theory we perform calculations of the dot potentials. We calculate the charging energies and the dot voltages for the possible charge configurations using experimentally determined capacitance values. The finite temperature effects are obtained by averaging the dot voltages corresponding to the different charge configurations assuming Boltzmann statistics. Since the device has no DC connection to the dots, the net charge is assumed to be zero. Charge configurations which do not fulfill this requirement are excluded from the thermal averaging. The results of calculations at 70 mK are shown in Fig. 4(a) and (b) and are in good agreement with experimental data.

As discussed earlier, the fundamental QCA logic device is a three-input majority logic gate that can be programmed to act as either an AND gate or OR gate. A conceptual diagram of the gate and its input cells is shown in Fig 5(a). We will implement only the central 4-dot cell, and use gates to mimic the dot potentials produced by the two dots of each input cell, shown by the shaded regions. A simplified schematic of the resulting QCA system is shown in Fig. 5(b). Details of the selection of the magnitude of the gate voltages corresponding to the dot potentials are given in [10].

In the experiment, the logic cell is biased using gates 1 – 4 to an unpolarized state where logic 1 and 0 are equally probable, and the electrometer outputs are set to 0 V for this condition. This procedure also cancels the effect of the substrate background charge. Differential signals A (between gates 1 and 3), B (between gates 1 and 2), and C (between gates 2 and 4) constitute the inputs to the central cell. The negative (positive) bias on a gate, Φ- (Φ+), mimics the presence (absence) of an electron in the input dots as shown by the shaded regions in Fig. 5(a). The amplitudes of Φ- and Φ+ are carefully chosen to mimic the potentials due to the polarization of an input cell. Differential signals A, B, and C are converted into logic levels 1 and 0 based on the convention used in Fig. 5(a). Since dots D1 and D2 are coupled to only one gate electrode each, voltages corresponding to inputs A and B on gate 1, and inputs B and C on gate 2, are added in order to mimic the effect of two input dots. For instance, the input configuration shown in Fig. 5(a) (i.e. ABC = 111) is achieved by setting V1 = 2Φ-, V2 = 2Φ+, V3 = Φ+, and V4 = Φ-.

Figure 5(c) shows the output of the majority gate as inputs A, B, and C are traced as a function of time according to the truth table. The output is the differential potential between dots D4 and D3, Φ_{D4}-Φ_{D3}, as measured using the electrometers E2 and E1. The measured output is shown by the solid line (the transient characteristics at the transitions are determined by the time constant of our electrometer circuitry). The theoretical results, shown by the dashed line, are calculated for the electron temperature in the experiment (70 mK), as determined from the Coulomb blockade peak-width

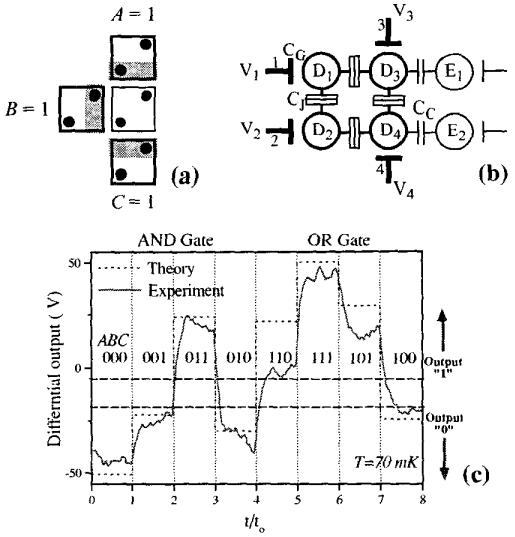


Figure 5. (a) Simplified diagram of QCA majority gate. (b) Schematic diagram. (c) Experimental results (solid line) along with theoretical data (dashed line).

dependence on temperatures. No adjustable parameters are used in the theory, and the agreement between the experimental and theory is excellent.

Output high (V_{OH}) and output low (V_{OL}) are marked by dashed lines in Fig. 5(c) showing a clear separation as required for digital logic. The first and last four input steps are grouped separately, with A as the programming input, to illustrate AND and OR operations. The AND operation is carried out when A = 0, for which we see that the output is high only when both of the remaining two inputs are high. The OR operation is performed when A = 1, for which the output is high when either of the other two inputs is high. Thus, the data shown in Fig. 5(c) confirm majority gate operation.

In an ideal logic gate the gap between V_{OH} and V_{OL} is large, as required for large noise margins. Our majority gate has only a small separation due to thermal smearing of the charge states of the dots, that results in a less than complete polarization of the cell. The performance of the gate can be improved by reducing the capacitance of the cell (by reducing the size of the dots), which will raise the energy of the excited states.

In our recent experiments we have demonstrated clocked control of QCA systems. As mentioned earlier, Toth and Lent [11] suggested a scheme for clocked control of the switching in metallic QCA cells where a central dot acts as a modulated barrier between the two dots forming a QCA half-cell, as shown in Fig. 6(a). This half cell has no DC connection to the external environment, so the overall cell remains electrically neutral throughout the experiment. When its gate sets the central dot's potential high it is energetically unfavorable for an electron to be on the middle dot, so the middle dot takes on a positive net charge. An electron moves to either the top or bottom dot, depending on the input bias applied to the cell as the central dot potential is raised. Once the central dot potential is high, the electron is locked into position. If the polarity of the input signal is reversed, the electron is trapped in a metastable state [11] which does not correspond to the minimal energy configuration. If the lifetime of this state is long compared to the switching speed of the circuit, then the locked cell can be used as a latch. However, the lifetime of this state is limited by cotunneling effects [12]. For this device, the estimated lifetime is on the order of 1 μs, which is several orders of magnitude smaller than the typical time scale of a scan in our experiment. For high-frequency (f > 10 MHz) applications, however, this would be sufficient to provide latching.

An important feature of the clocked QCA architecture is that the polarization of the cell is changed using the clock signal. The small input signal only defines the final cell polarization while the clocking signal drives

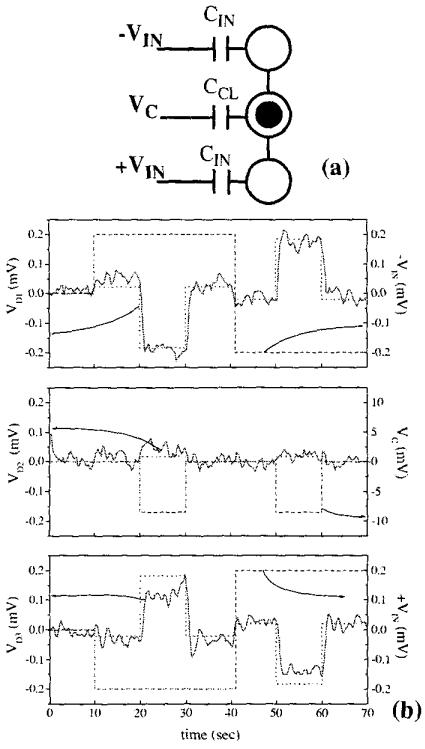


Figure 6. (a) Simplified diagram of clocked QCA half-cell. (b) Schematic diagram. (c) Experimental results. Dot potentials (solid lines), along with theory (dotted lines), and applied voltages (dashed lines).

the electron transfer. To demonstrate this, the following experiment is performed. First (t=0 sec.) in Fig. 6(b), the system is set to a null mode, where the potential of the middle dot is low, and all dots in the cell are neutral, and the cell unpolarized. Here $V_C = 0$, and $V_{IN} = 0$. Then at t=10 sec. the input differential signal $V_{IN} = -0.2$ mV is applied to the input gates. This creates some asymmetry in the potential of the top and bottom dots, but the system remains in the null mode, and as seen in Fig. 6(b), the dot potentials remain very close to zero. Then at t=20 sec. the clock signal changes from $V_C = 0$ to $V_C = -8.5$ mV raising the potential of the middle dot. This drives the system from the null mode with charge configuration (0,0,0), excess electron population of the (top, middle, bottom) dot, through the transition (the active mode) where an electron moves to D1 leaving a hole on D2, and into the locked mode (charge configuration (1,-1,0)). At t=30 sec., the clock signal is set to 0, and the cell again is driven to the null mode. At t=40 sec., the polarity of the input voltage is reversed, and at t=50 sec. the clock signal is again applied, so the half-cell acquires the opposite polarization (0,-1, 1).

To demonstrate a working QCA latch, we fabricated another device where the tunnel junction between the three dots is replaced by a multi-tunnel junction (MJT) consisting of three tunnel junctions. These extra tunnel junctions suppress the rate of co-tunnelling, increasing the lifetime of the metastable state to a few seconds, sufficient for our low speed measurements. A schematic of the latching half-cell is shown in Fig. 7(a). Only one electrometer is necessary to determine the polarization of the cell.

Operation of the latching cell is shown in Fig. 7(b). The top panel shows the input voltage applied to the top dot, the clock signal in the middle panel, and the top-dot potential (output) in the bottom panel. When a small negative voltage input is applied, the cell responds with only a small change in the potential of the top dot. Next the clock is applied (negative voltage) and the input data is latched into the cell. Note that a single half-cell inverts the input. When the input is removed at t=0.3 sec. the output of the latch remains in the high state until the clock is released at 1.5 sec., whereupon the cell returns to its null state. At the times 1.5 to 3 sec. a bit of

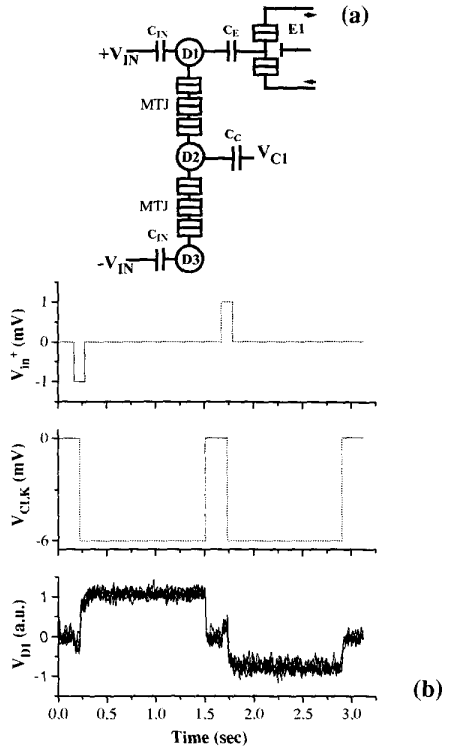


Figure 7. (a) Schematic of a latching QCA half-cell, showing the multi-tunnel junctions. (b) Experimental results. Top panel: input voltage; middle: clock; bottom: output.

the opposite polarity is clocked into the latch. This demonstrates the operation of a latching cell.

3. Conclusions

Quantum-dot cellular automata is a dramatic departure from usual digital logic devices in that information is encoded by the position of single electrons, not by the operating state of an FET current switch. We have experimentally demonstrated many of the functional elements of the QCA paradigm including individual cells, lines, logic gates, and clocking. In this paper we have given a short introduction to QCA and a brief overview of some experiments.

While our experiments demonstrate the feasibility of the QCA paradigm, significant challenges must be overcome before practical applications are possible. The greatest challenge, operating temperature, is also an opportunity. An important advantage of QCA is that since its basis of operation exploits quantum mechanics, scaling is possible to the molecular level. In fact, the smaller the device, the better it works. Our current devices operate only at temperatures below 200 mK because of the large area of the device and high capacitance of the tunnel junctions. As the device is scaled down in size the operating temperature increases, and molecular sized devices will operate at room temperature. Molecular implementations of QCA are being investigated, and should offer power densities unattainable in conventional digital logic.

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