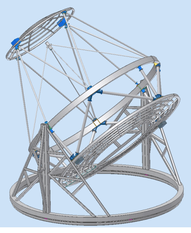

The Advanced Gamma-ray Imaging System (AGIS)
— Camera Electronics Designs —

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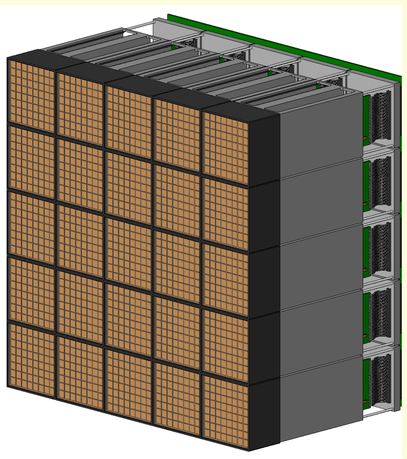
Report of the Camera Electronics Working Group, AGIS collaboration

Abstract

AGIS, a next-generation atmospheric Cherenkov telescope array, aims to achieve a sensitivity level of about one milliCrab for gamma-ray observations in the energy band of 40 GeV to 200 TeV. Achieving this level of performance will require on the order of 50 telescopes with perhaps as many as 1M total electronics channels. Producing this affordably will require individual components with lower cost and higher reliability than are used in the current generation of telescopes. We are exploring several design concepts to reduce the cost of camera electronics while improving their performance. These design concepts include systems based on multi-channel waveform sampling ASIC optimized for AGIS, a system based on IIT (image intensifier tube) for large channel (order of 1 million channels) readout as well as a multiplexed FADC system based on the current VERITAS readout design.
Here we present comparison of these design concepts..

Introduction:

Given scientific requirements of the AGIS, we envision an instrument consisting of 50–100 telescopes with 5,000–10,000 pixel cameras. This corresponds to an increase of more than two orders of magnitude in the number of channels compared with the current generation experiments. With a target cost for the camera of less than $20 per pixel, the AGIS project will require a dramatic change in the electronics approach compared with previous instruments, where the camera cost ranged from $1k to $2k per channel. In addition to the cost reduction, reliability of camera components is also a critical feature due to the number of pixels involved. Fig. 1 shows proposed modular camera design consisting of photodetector, front-end electronics, HV system and DAQ interface. Modular design makes it easier to assemble and maintain a large number of cameras.



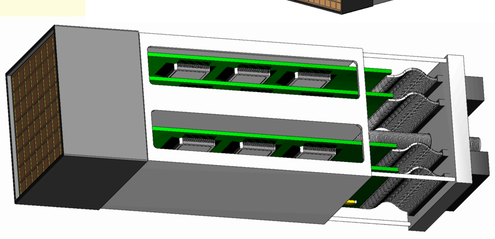


Fig. 1 Modular camera design

From scientific requirements and budget constraints, specifications of camera electronics can be summarized as

- ADC sampling time: > 1Gsps,
- Readout time: < 30 μs,
- Trigger latency tolerance: > 2 μs,
- Dynamic range: > 8 bits
- Target cost: $15 per pixel.

In order to meet above requirements, we are exploring several design concepts to reduce the cost of camera electronics while improving their performance. These design concepts include

- systems based on multi-channel waveform sampling ASICs,
- a system based on IIT (image intensifier tube) for large channel readout,
- a multiplexed FADC system based on the current VERITAS readout design.

Here we present comparison of these design concepts.

Multiplexed FADC system:

This option is an extension from the current VERITAS camera readout system and consists of preamplifier, delay line, analog multiplexer and Gsps flash ADC. Low-threshold comparators and pattern trigger boards are used to switch the region of interest (a subfield of the full camera) into a bank of FADCs (see Fig. 2). Since the angular extent of shower images is typically less than 1°, a large data reduction is possible if one can quickly select a readout region around the triggering pixels. New ADCs which dissipate less than 1 watt per channel, with two Gsps devices in a single package are commercially available and have been tested in the lab at Washington University. A detailed cost estimate gives $250 for each FADC channel, and $25 per pixel with >10:1 multiplexing.

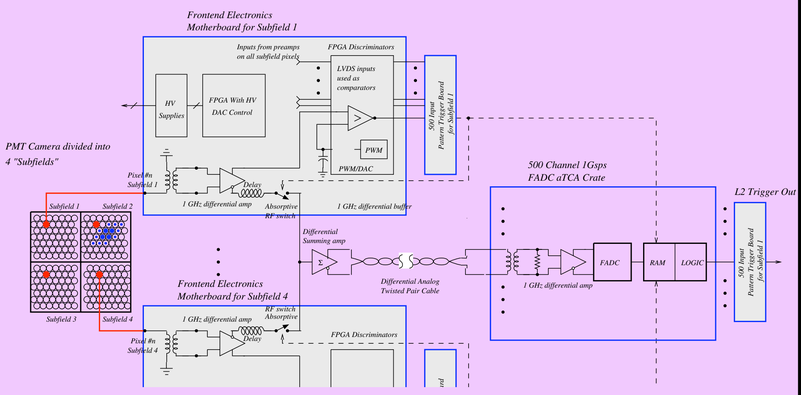


Fig. 2 Diagram of multiplxed FADC system

Image Intensifier Tube + CMOS sensor system:

This option is based on a combination of preamplifier, delay line, fiber driver, optical fibers and image intensifiers (IIT), along with hybrid CMOS Si sensors as shown in Fig. 3. In this approach, large numbers of optical fibers are bundled together and fed to the IIT+CMOS sensor readout system, significantly reducing the number of readout systems, which results in lower cost and easier maintenance. Recent advances in technologies made this approach feasible. New hybrid CMOS technology that provides off-the-shelf very fast readout (>160 MHz/pixel, using >16 channels at 10 MHz/pixel) and provides the ability to address/read arbitrary groups of pixels in the 1024x1024 array of pixels, thus further increasing speed in select windows (a picture of such a sensor is shown in Fig. 3) [1,2]. Image intensifiers can be gated with ~2 ns resolution. Fibers can be driven with laser drivers that have ~2 ns response, and the fibers are regularly made such that they suffer <1% losses over >700 m distances. The total per channel cost is expected to be $~10 per pixel, which is dominated by front-end (cost of the fiber, IIT and CMOS sensor is insignificant). One major drawback of this approach is loss of waveform recording capability present in the other options.

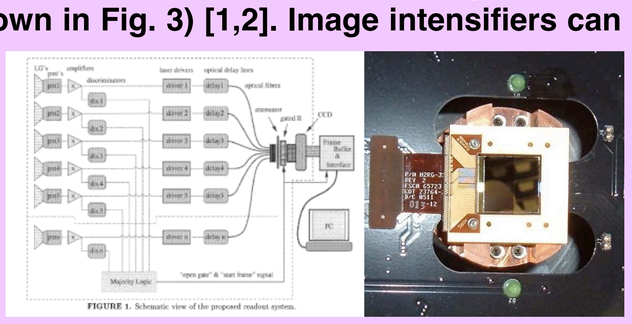
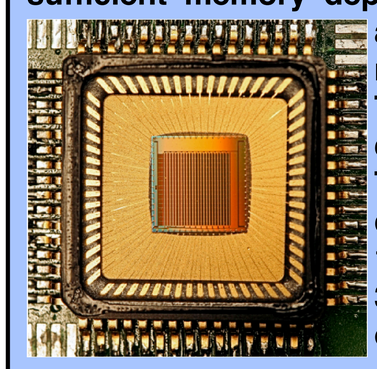


FIGURE 1. Schematic view of the proposed readout system.

Fig. 3 Left: Diagram of IIS+CMOS sensor system. Right: Picture of a CMOS sensor with random access.

Multi-channel Waveform Sampling ASICs:

This option makes use of mixed-signal Application Specific Integrated Circuit (ASICs) based on the SCA (Switched Capacitor Array) architecture to reduce the cost and power consumption of the camera readout system. The basic theory of operation is shown in diagrams below. Signals from a photodetector are continuously stored into an array of capacitors that act as analog memory. With sufficient memory depth, an array trigger can stop acquisition, allowing the analog memory to be addressed, the pulse localized in memory and the stored analog samples to be digitized.



The Domino Ring Sampler ASIC [3] shown in Fig.4 is developed at the Paul Scherrer Institute in Switzerland. The DRS3 chip is the third version of this design and contains 12288 sampling cells, which can be arranged as 1, 2, 3, 4, 6, or 12 channels then with 12288, 6144, 4096, 3072, 2048 or 1024 cells, respectively. This allows us to operate it in a 6-channel mode with 2048 samplings to achieve 2 μs look-back time at 1 Gsps sampling rate. DRS3 ASIC features a special readout mode which selects only a certain region-of-interest (ROI) for output and brings down the readout time to 3 µs for 100-cell readout at 33 Msps. The DRS3 chip consumes 50 mW of power at 2 Gsps. The expected cost is $~16 per pixel. This ASIC meets the AGIS specifications and is commercially available, making this an attractive option.

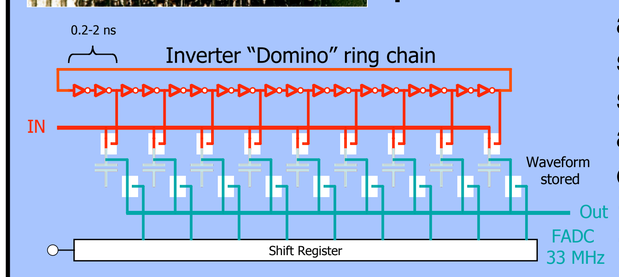


Fig. 4 Top: Picture of Domino Ring Sampler (DRS3) ASIC. Bottom: Diagram of DRS3.

We are also developing an ASIC customized for the AGIS specifications based on LABRADOR family of ASICs [4] originally developed for the ANITA experiment (picture of LABRADOR is shown in Fig. 5). These ASICs are unique since they include highly parallel fast ADCs on chip, and are capable of 1 Gsps digitization with a 10-bit resolution. The customized ASIC is designed to incorporate 16 channels each with 4096 samplings (corresponding look-back time of 4 μs at 1 Gsps sampling rate). Total conversion and readout time is 16 µs for 16 channels when reading out 32 samples per channel (this is programmable). The expected cost is $~10 per pixel due to elimination of external flash ADCs. The design layout has been submitted to a foundry for fabrication with expected delivery in May 2008.

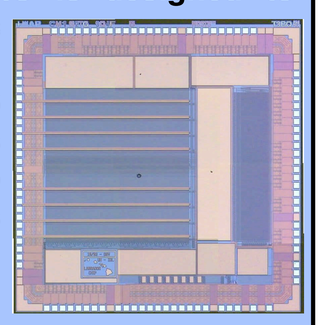


Fig. 5 Picture of LABRADOR ASIC

References:

1. A. D. Falcone, et al., "Hybrid CMOS X-ray Detectors: The Next Generation for Focused X-ray Telescopes," Proc. SPIE, Vol. 6686, 02-1 (2007).
2. Y. Bai, M. C. Farris, A. Joshi, J. R. Hosack, J. Bajaj, J. T. Montroy, "Recent progress of hybrid CMOS visible focal plane array technology," Proc. SPIE, 5902, 94 (2005).
3. S. Ritt., "The DRS chip: Cheap waveform digitizing in the GHz range", Nucl. Instum. Meth., A518, 470 (2004).
4. G. S. Varner, et al., "The large analog bandwidth recorder and digitizer with ordered readout (LABRADOR) ASIC," Nucl. Instum. Meth., A583, 447 (2007).