Speed Regulation of DC Drive Using Mobile Communication

Shakti Bajaj, Ravinder Kumar Bhataia, J. Sandeep Soni

Abstract- The importance of the speed control of DC motors in manufacturing industries like plastic, textile, chemical and pharmaceutical hardly needs any emphasis as it ensures efficient and consistent production. In this paper, the authors present implementation of a hardware circuit which is designed for remote speed control of a DC motor by using Dual Tone Multi Frequency (DTMF) tone of mobile phone. The hardware circuit includes the use of DTMF decoder IC MT8870 and Relay driver IC ULN2003. The mobile keypad keys have been mapped to the speeds of 'High Speed', 'Medium Speed', 'Low Speed' and 'Stop' to regulate the speed of DC motor.

Keywords- DC motor, DTMF, IC MT8870, IC ULN2003

Fig.1: Block diagram of remote speed control of a DC motor by Mobile

I. INTRODUCTION

A DC motor generates torque directly from DC power supplied to the motor by using internal commutation, stationary permanent magnets and by rotating electrical magnets. It works on the principle of Lorentz force according to which any current carrying conductor placed within an external magnetic field experiences a torque or force known as Lorentz force. The latest development in DC drives are the brushless DC drives, advantages of a brushed DC motor include low initial cost, higher reliability and simple control of motor speed. DC motors can be used as DC drives in various applications requiring adjustable speed as well as good speed regulation and frequent starting-braking-reversing. Some important industrial applications of DC drives are rolling mills (paper, steel), mine winders, hoists, machine tools, traction, printing presses, textile mills, excavators and cranes [1]. There are great number of methods which can be used to control the speed of DC motors [2,3]. If a DC motor operates with the remote control by the mobile phone it is obviously advantageous for the industry. In this project, speed control of a DC motor is ensured by using Dual Tone Multi Frequency (DTMF) tone of mobile phone. The DTMF is a method of representing digits with tone frequencies in order to transmit them over an analog communication network [4].

The tone received by mobile headphone is processed by DTMF decoder IC MT8870 which decodes into equivalent binary. This binary signal is further sent to relay driver IC ULN2003 to ON/OFF the relays according to the key pressed by the user which is responsible for controlling the speed of DC motor.

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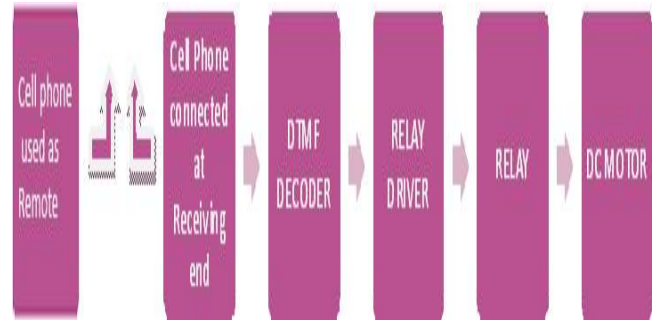**J.Sandeep Soni,** Faculty, Department of EE, BKBIET, Pilani, Rajasthan, India

II. CIRCUIT ILLUSTRATION

A. Circuit Introduction

This process works when a mobile phone initiates a call for the other mobile phone on any network which is connected with the receiver end in auto answer mode. During this outgoing call if a key is pressed the associated key generates dual tone multiple frequency (DTMF) at the other end. The received tone is processed by DTMF decoder IC MT8870. A specific frequency consisting of two separate tones is assigned by the DTMF decoder. It produces two different frequencies from lower band and upper band frequencies. For example, if the user presses a key'2' it will send a tone comprising of 697 Hz and 1336 Hz to the other end of the system. Then the decoder produces an equivalent binary digit after decoding the DTMF tone [5]. This binary number goes to relay driver IC ULN2003, which drives the relays and produces the output for DC motor. Crucial components used in this project are DTMF decoder (MT8870), Relay driver (ULN2003) and Voltage regulator (7805). When mobile headphone output is connected to pin 2 (IN-) in a single- ended input configuration it is recognised to be effective, a correct 4-bit decoded signal corresponding to the DTMF tone is transferred to pin 11 (Q1) - pin 14 (Q4) outputs. Q1-Q4 pins of the DTMF decoder are connected to input pins (1 B - 4 B) of relay driver IC ULN2003 respectively. Pin 1 (IN+) and pin 4 (V_{ref}) of DTMF decoder IC MT8870 are shorted. Binary output from MT8870 is not sufficient for operating the relays directly since the magnitude of output current is very low. Thus, the authors have used ULN2003 for current amplification purposes. A 3.597 MHz crystal oscillator is used for providing clock input to MT8870. The output from Voltage regulator (7805) i.e. 5 V is given to MT8870 . The Circuit layout on which the hardware has been implemented is shown in Figure 2.
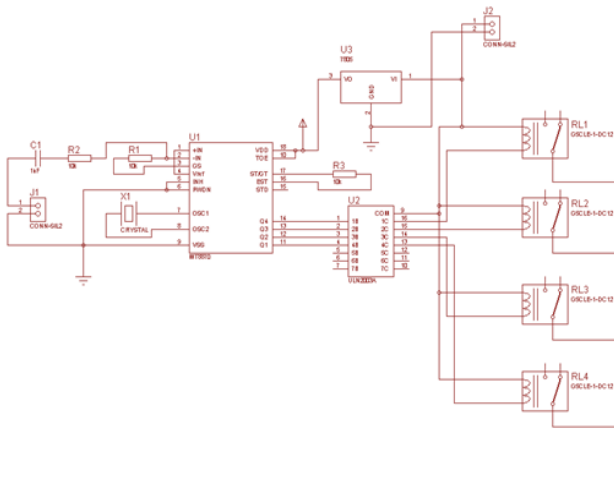
Fig.2: Circuit layout

B.   DTMF decoder MT8870

MT8870 is a complete DTMF receiver. It integrates the band split filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters. The decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. This DTMF receiver minimizes external component count by providing an on-chip differential input amplifier, clock generator and a latched three-state interface bus [6]. The MT8870 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a band split filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus. The DTMF technique presents distinct representation of 16 common alphanumeric (0-9, A-D, *, #) on the mobile phone. The lowest frequency used is 697 Hz and the highest frequency used is 1633 Hz. The DTMF keypad is arranged in such a way that each row will have its own unique tone frequency and also each column will have its own unique tone frequency. The frequency assignments in a DTMF system are shown in Table 1.

Frequency	1209 Hz	1336 Hz	1477 Hz	1633 Hz
697 Hz	1	2	3	A
770 Hz	4	5	6	B
852 Hz	7	8	9	C
941 Hz	*	0	#	D

Table1: Frequency assignments in a DTMF system

Among the keys specified in Table 3, only 4 different keys have been used to serve the purpose of controlling the speed. The Table 2 shows the action performed corresponding to the keys pressed.

KEY PRESSED BY THE USER	ACTION PERFORMED
1	High Speed
2	Medium Speed
4	Low Speed
8	Stop

Table2: Function assigned for the key

Low	High	Digit	Binary Output

Group Freq.(Hz)	Group Freq.(Hz)		Q4 (MSB)	Q3	Q2	Q1 (LSB)
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

Table3: DTMF data output

For DTMF decoding in the project, the circuit used is Single Ended Input configuration as shown in Figure 3. Pin Description of IC MT8870 is illustrated in Table 4. The functional block diagram of MT8870 is shown in Figure 4.
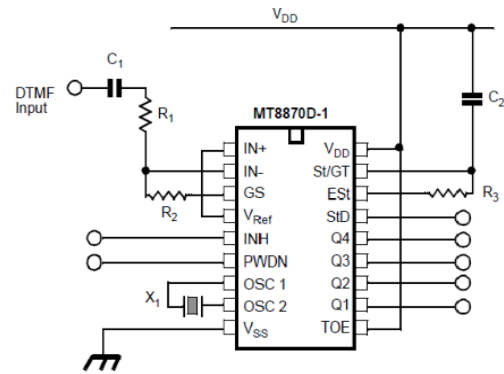

Fig.3: Single Ended Input Configuration of MT8870

PIN DESCRIPTION

Pin 18	Pin 20	Name	Description
1	1	IN+	**Non-Inverting Op-Amp(Input)**
2	2	IN-	**Inverting Op-Amp(Input)**
3	3	GS	**Gain Select.** Gives access to output of front end differential amplifier for connection of feedback resistor.
4	4	V_{ref}	**Reference Voltage (Output).** Nominally $V_{DD}/2$ is used to bias inputs at midrail.
5	5	INH	**Inhibit(Input).** Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
6	6	PWDN	**Power Down (Input).** Active high powers down the device and inhibits the oscillator. This pin input is internally pulled down.
7	8	OSC1	**Clock (Input).**
8	9	OSC2	**Clock (Output).** A 3.579545 MHz crystal oscillator connected between Pins OSC1 and OSC2 completes the internal oscillator circuit.
9	10	V_{ss}	**Ground (Input).** 0V typical.

10	11	TCE	**Three State Output Enable (Input).** Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	12-15	Q1-Q4	**Three State Data (Output).** When enabled by TOE, provide the code corresponding to the last valid tone-pair received. When TOE is logic low, the data outputs are high impedence.
15	17	StD	**Delayed Steering (Output).** Presents a logic high when a received tone-pair has been registered and the output latch updated, returns to logic low when the voltage on St/Gt falls below V_{TSt}.
16	18	ESt	**Early Steering (Output).** Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return a logic low.
17	19	St/GT	**Steering Input/Guard time (Output) Bidirectional.** A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant its state is a function of ESt and the voltage on St.
18	20	V_{DD}	**Positive power supply (Input)** +5V typical
	7,16	NC	No Connection

Table4: Pin Description of MT8870

current of 600mA. The inputs and outputs are provided opposite to each other in the pin layout. Each driver also contains a suppression diode to dissipate voltage spikes while driving inductive loads. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED gas discharge), line drivers, and logic buffers. The ULN2003 has a 2.7kW series base resistor for each Darlington pair for operation directly with TTL or 5V CMOS devices. These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal print heads and high power buffers [7]. The schematic for each driver is shown in Figure 5.

Fig.5: Schematic for each driver

The logic diagram of ULN2003 is shown in Figure 6 and the Pin Description of ULN2003 is illustrated in Table 5.
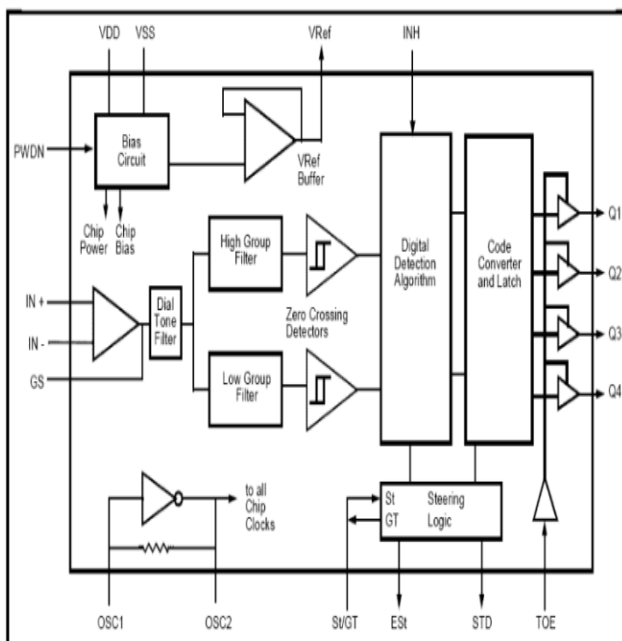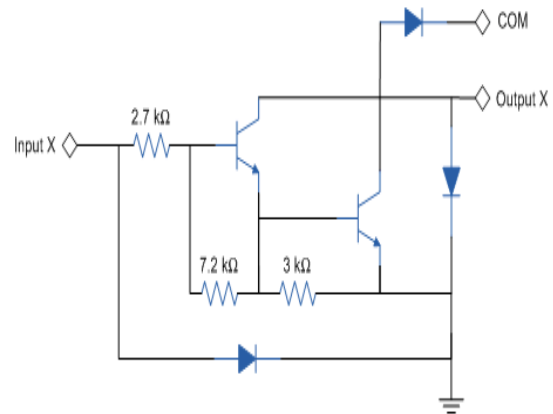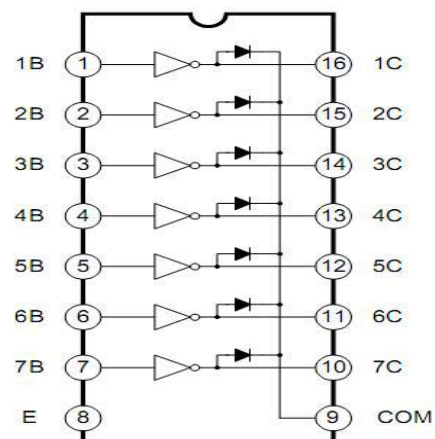

Fig.4: Functional block diagram of MT8870

C. Relay driver ULN2003

ULN2003 is a high voltage and high current Darlington array IC. It contains seven open collector Darlington pairs with common emitters. A Darlington pair is an arrangement of two bipolar transistors. ULN2003 belongs to the family of ULN200X series of ICs. Different versions of this family interface to different logic families. ULN2003 is for 5V TTL, CMOS logic devices. Each channel or Darlington pair in ULN2003 is rated at 500mA and can withstand peak

Fig.6: Logic Diagram of ULN2003

PIN DESCRIPTION

Pin No	Function	Name
1	Input for 1st channel	Input 1
2	Input for 2nd channel	Input 2
3	Input for 3rd channel	Input 3
4	Input for 4th channel	Input 4
5	Input for 5th channel	Input 5
6	Input for 6th channel	Input 6
7	Input for 7th channel	Input 7

8	Ground (0V)	Ground
9	**Common freewheeling diodes**	**Common**
10	Output for 7th channel	Output 7
11	Output for 6th channel	Output 6
12	Output for 5th channel	Output 5
13	Output for 4th channel	Output 4
14	Output for 3rd channel	Output 3
15	Output for 2nd channel	Output 2
16	Output for 1st channel	Output 1

Table5: Pin Description of ULN2003

III. HARDWARE DESIGN

The circuit layout of remote speed control of a DC motor by mobile shown in Figure 2 has been implemented in hardware as illustrated in the Figure 7.

Fig.7: Hardware design for remote speed control of a DC motor by mobile

IV. CONCLUSION

We have discussed and successfully demonstrated the purpose, use and implementation of mobile communication system to control speed of DC motor from remote area using mobile. To achieve this, we have used the concept of relay operation using decoding of DUAL TONE MULTI-FREQUENCY SIGNALING (DTMF) produced by mobile. We have designed a hardware module connected with a prototype load as DC motor and have performed precise control and speed tests as well as braking. Its efficiency is relatively high as compared to the other similar methods.

V. ACKNOWLEDGEMENTS

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