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A Novel Dedicated Low Power 64 Bit Digital Comparator Using Cmos Logic

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Abstract In this paper we have designed a novel dedicated low power 64 bit digital comparator. Magnitude comparison is one of the basic functions used for sorting in microprocessor, digital signal processing, so a high performance, effective magnitude comparator is required. The main objective of this paper is to provide new low power, area solution for Very Large Scale Integration (VLSI) designers. A Low Power 64-bit CMOS binary comparator is proposed in this brief. Comparison is most basic arithmetic operation that determines if one number is greater than, equal to, or less than the other number. Comparator is most fundamental component that performs comparison operation. This brief presents comparison of modified and existing 64-bit binary comparator designs concentrating on power delay product. Modifications are done in existing 64-bit binary comparator design to improve the PDP of the circuit. Simulation of the proposed design is performed at 180 nm technology in Tanner EDA Tool.

Keywords: *Binary comparator, digital arithmetic, Power delay product (pdp), CMOS logic*

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1. Introduction

Binary comparators are found in a wide variety of circuits, such as microprocessors, communications systems, encryption devices, image processing, 3D graphics and many others. A faster, more power efficient, or more compact comparator would be an advantage in any of these circuits. use of comparators in high-performance systems places a great importance on the extensive performance and power consumption optimizations. A comparator basically involves comparison of two n-bit bit numbers is a critical operation for almost all digital systems. A comparator compares two n-bit values to determine which is greater, or if they are equal. In general it is used to compare two inputs. Comparators are broadly classified into Analog and Digital comparators. However in this brief what is concerned is about the digital comparator. The digital comparator is further classified into Total (Full) comparators and Equality comparators. In full comparators, given two n-bit binary numbers A and B, they are able to separately recognize the three possible conditions i.e. A > B, A < B and A = B. In equality comparators, as the name suggests, they only indicate equality when both the inputs are equal. Comparators find their applications in many Digital Signal Processors. It has been an important logic block in an ALU and have extensive applications such as decoding of x86 instructions [1]. It also finds applications in MIMO (Multiple Input Multiple Output) decoding algorithms require extensive iterations of binary number comparison. In recent year, high speed & low power device designs have emerged as principal theme in electronic industry due to increasing demand of portable devices. This tremendous demand is due to popularity of battery operated portable equipments such as personal computing devices, wireless communication, medical applications etc. Demand & popularity of portable electronic devices are driving the designers to strive for higher speed, smaller power consumption and smaller area. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. Circuit size depends on the number of transistors and their sizes and on the wiring complexity. The wiring complexity is determined by the number of connections and their lengths. All these characteristics may vary considerably from one logic style to another and thus proper choice of logic style is very important for circuit performance. in this paper a hierarchical approach has been adopted to design the CMOS comparator. Simulations are carried out for delay and power consumption with varying supply voltage at 180 nm technology in Tanner EDA Tool [2].

1.1. Conventional Comparators vs Hierarchical Comparators

Conventional comparators are generally used for small magnitude comparison and becomes tedious for the case

of large magnitude comparisons. To meet this requirement hierarchical comparators are used. Hierarchical design is suitable for wide comparators, faster designs are possible by combining several smaller comparators in a hierarchical fashion. By combining one or both of the designs with different widths in different stages, it is possible to take advantage of the best characteristics of both designs and create hierarchical comparators to meet a wide variety of speed, power, and area requirements [3].

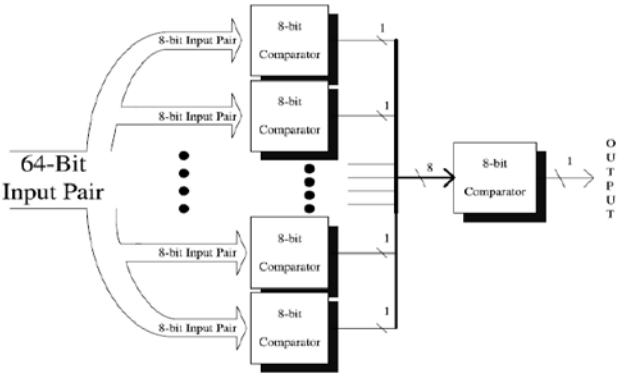

Figure 1. Schematic of hierarchical design

1.2. CMOS Based 64 Bit Digital Comparator

64-bit binary comparator compares two numbers each having 64 bits (A63 to A0 & B63 to B0. This comparator is designed by combining seven numbers of 8 bit comparators and a final decision maker single 4 bit comparator arranged in hierarchical fashion [4].

1.3. Circuit Diagram of Cmos Based 8 Bit Comparator

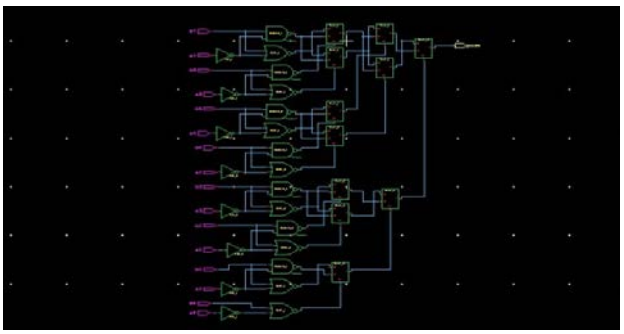

Figure 2. Circuit diagram of 8 bit comparator

1.4. Circuit Description of 8 Bit Comparator

In this, the magnitude of two binary numbers is compared by identifying the locations of the first 1 from the MSB. The one that has the first 1 in most significant position is the largest. In case that the locations of the first 1 are the same in both numbers, the decision is postponed to the lower bit where only one input has 1 in that bit position if X >*Y*, Output comp = 1 and if X ≤Y, Output comp =0.

The results less than or equal to are conveyed by the same output Comp. This circuit uses basic logic gates such as NAND gates, NOR gates, inverters and a 2:1 Mux [5].

In general the sum of Mux gates in n-bit comparator is given by

$$\sum_{k=1}(2^k - 1), where\ M = \log_2 N$$

The total number of gate count in n-bit comparator is

$$INV \times N + AND2 \times N + OR2 \times (N-1) + Mux2to1_{stage-1} \times (n-1) +$$

$$Mux2to1_{Higher-stage} \times \{[\sum_{k=1}^{M}(2^k - 1)] - (N-1)\},$$

$$where\ \ M = \log_2 N.$$

1.5. CMOS Implementation of 8 Bit Comparator

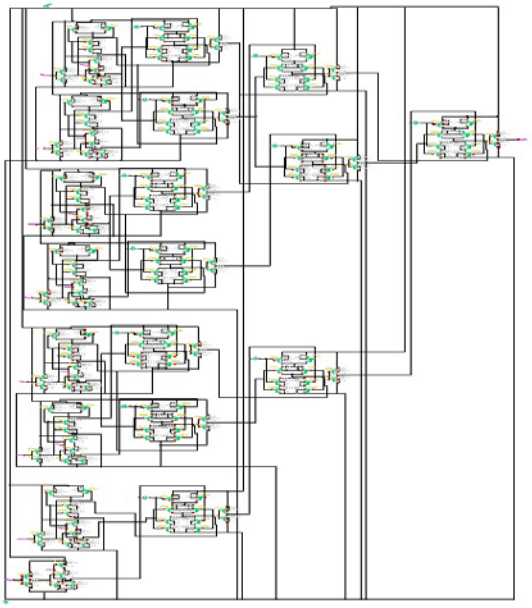

Figure 3. CMOS implementation of 8 bit comparator

1.6. Design of 64 Bit Comparator Using Eight 8 Bit Versions and One 4 Bit Version

The proposed design strategy uses a hierarchical design of a full cmos 64-bit comparator is shown in Figure 3.4, which is composed of eight 8-bit comparators and one final 4 bit comparator. The 64 bits are divided into eight bytes which are evaluated at the same time, and then the 4-bit comparator produces the final output signal [6].

Figure 4. Circuit diagram of 64bit comparator

2. Circuit Description

To improve the speed and reduce power consumption, several designs rely on pipelining and power-down mechanisms to reduce switching activity with respect to the actual input operands' bit values. This design uses all-N-transistor (ANT) circuits to compensate for high fan-in with high line throughput. This circuitry leverage custom logic gates for performing comparison. This architecture splits a 64-b comparator into two comparator stages, the first stage consists of eight modules performing 8-b comparisons and the modules' outputs are input into a second stage. The second stage uses a 4 bit comparator to get the final result [7].

This proposed design strategy uses a hierarchical design of a fast 64-bit comparator is shown in Figure 4.3, which is composed of eight 8-bit comparators and one final 4-bit comparator. The 64 bits are divided into eight bytes which are evaluated at the same time, and then the 4-bit comparator produces the final output signal. This modified 64 bit comparator depicts A<B, A=B and A>B respectively [8].

3. Simulation Result & Analysis

Figure 5. Experimental result of CMOS based 64 bit comparator for A>B

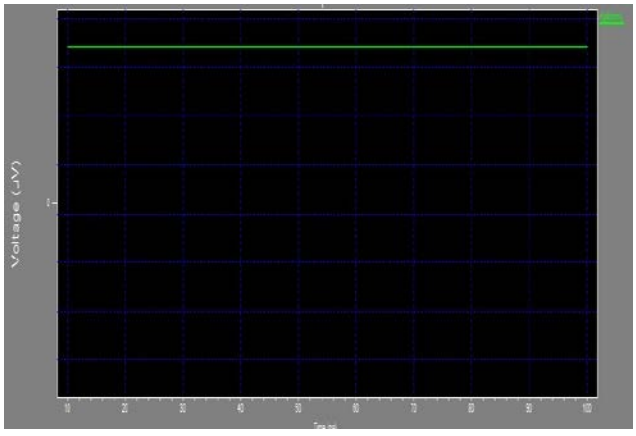

Figure 6 Experimental result of CMOS based 64 bit comparator for A≤B

We have performed simulation of the proposed design by using Tanner EDA tools with 180 nm technology at room temp. i.e. 27°C. In this experiment we have adjusted the aspect ratios i.e. (W/L) of both PMOS and NMOS transistors so as to get the accurate results.

The experiment has been performed by considering different values of the two 64 bit numbers.

The design is simulated at different power supply voltage ranging from 1v to 5v and corresponding delay is measured with the target to reach less power delay product (PDP) I.e. energy.

3.1. Power Comparison

The average power consumption is also measured by applying a complete pattern during a long period of time. In this experiment, the Existing and modified comparators are simulated at 180 nm nm feature size by varying supply voltages ranging from 1v to 5v with 1v as step size.

Table 1. Comparision between power supply and power consumed

supply voltage (volts)	Power consumption (watts)	Capacitance (farade)	Delay time (seconds)
1.0	2.9228e-003	2.0000e-013	4.0818e -009
2.0	3.5848e-002	4.0000e-013	4.132e -009
3.0	1.3017e-001	6.0000e-013	4.2053e-009
4.0	3.2768e-001	8.0000e-013	4.2654e-009
5.0	6.5548e-001	1.0000e-012	4.3286e-009

Simulation results for 64 bit digital comparator using CMOS style.

Table 2. comparision between power supply and pdp

supply voltage (volts)	Power consumption (watts)	Delay time (nano seconds)	power delay product (nano wattsec)
3.0	1.72521e-001	130.69	22.7
4.0	3.6981e-001	40.47	18.0
5.0	4.6401e-001	40.20	15.0

Simulation results for 64 bit digital comparator using CMOS style.

3.1.1. Power Supply vs Power Consumed for Cmos

The power consumption for existing designs are calculated by performing simulation of circuit. Simulation results for power consumptions by varying supply voltage ranging from 1v to 5v with 1v as step size is shown as below.

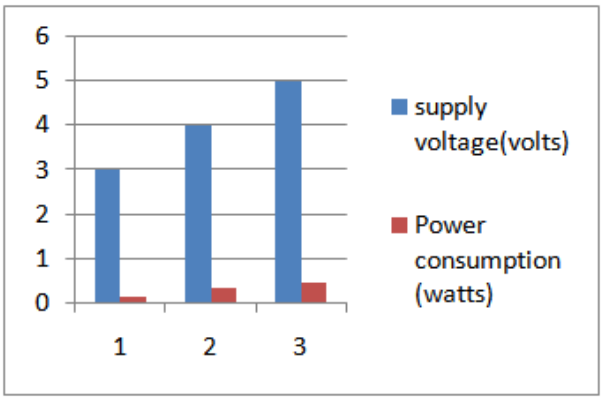

Figure 7. Graph between power supply and power consumed

3.2. Delay Consideration

The delay is also measured by applying a complete pattern during a long period of time. In this experiment, the comparators are simulated at 180 nm feature size by varying supply voltages ranging from 3v to 5v with 1v as step size.

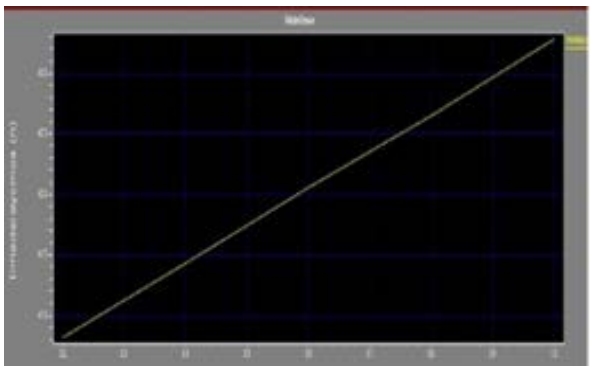

Figure 8. comparisons between delays of proposed design

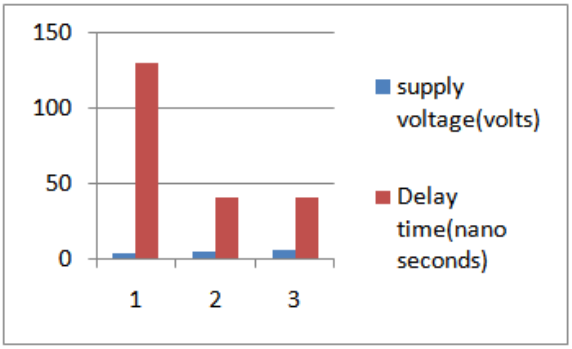

Figure 9. Comparision between power supply and delay

3.3. Power Delay Product Consideration

The PDP is a qualitative measure of efficiency and compromise between power dissipitation and speed. PDP is particularly important When low power operation is needed. The average power consumption and average delay is calculated to find the energy required for the proper operation of the circuit is calculated and tabulated as below.

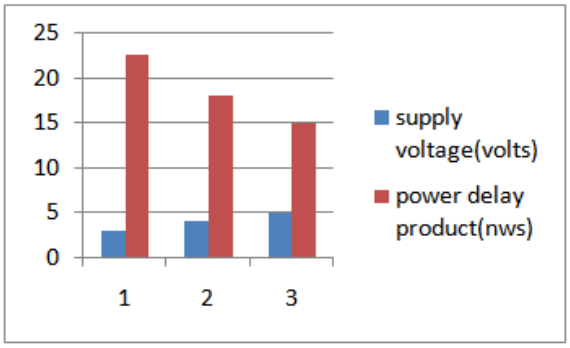

Figure 10. Comparision between power supply and pdp

From the above graph it is seen that in the proposed CMOS based design the PDP is decreasing with respect to power supply. The design having lowest PDP is very energy efficient.

4. Conclusion

The PDP represents a tradeoff between two compromising features of power dissipation & circuit latency. Therefore the experimental analysis are made by giving emphasis on PDP.

On the basis of experimental result analysis the CMOS based comparator is shown to be superior in terms of PDP over virtually all testing conditions.

Improvement in PDP is one of the essential requirement for the present scenario of IC design.

Acknowledgement

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