A Three-Level MOSFET Inverter for Low Power Drives

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***Abstract*-This paper proposes operating a three-level Neutral Point Clamped (NPC) inverter using a two-level PWM method. This allows for the clamping diodes to be rated at a fraction of the main switches due to their low average current requirement. The use of a charge pump as a low cost method to obtain the isolated gate drive power supplies is extended for use with the NPC topology. Using this control method and circuits, an inverter based on high volume, low-cost low-voltage power MOSFETs is experimentally demonstrated as a possible economic alternative to an IGBT based drive for 120 Vrms-supplied systems.**

I. Introduction

The three-level Neutral Point Clamped (NPC) inverter [1] shown in Fig. 1 has evolved into the standard for medium voltage motor drive systems as evidenced by the commercial availability of medium voltage drives based on both IGCT [2] and high voltage IGBT devices [3]. The topology has two important attributes that make it well suited to this market: lower harmonic content than a standard two-level inverter, and the fact that the main switching devices are required to block only one-half of the dc bus voltage. This latter attribute has traditionally been exploited to allow for higher voltage drives since device voltages have been limited. However, it also implies that a drive of a given voltage can be obtained with lower voltage devices by employing the NPC topology.

Low voltage power MOSFETs have achieved a significant (~4-5:1) cost advantage in terms of $/Amp over IGBTs due to their very widespread use in the automotive and power supply industries. This paper investigates the feasibility of a low power motor drive employing 150 V MOSFETs and the NPC topology. Since the NPC topology requires twice as many switches, the cost savings afforded by using inexpensive MOSFETs as the main switching devices can be eliminated by the extra gate drivers and clamping diodes that the NPC topology requires. In an effort to overcome this problem, this paper proposes a gate driver circuit designed around inexpensive discrete components. It also proposes a four level charge pump scheme, which eliminates the need for isolated gate drive power supplies. It further proposes a new control method for the NPC inverter that allows for the clamping diodes to be rated at only a fraction of the current rating of the main switches. This combination results in a low power drive that can be competitive in terms of component cost when compared to an IGBT based drive. The concept has important commercial implications since cost has been the largest drawback to the widespread consumer adoption of low voltage drives [4].

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II. Operating Principle

The NPC inverter is capable of connecting the load to the upper bus (level 2, S_{x1}, S_{x2} on), the dc bus neutral point (level 1, S_{x2}, S_{x3} on), and the lower bus rail (level 0, S_{x3}, S_{x4} on) [5]. When outputting a level 0, one of the clamping diodes (D_{x1}, D_{x2}) is conducting the phase current depending on the current polarity. If the converter is actively controlled to quickly transition through the level 1 output state, which is a requirement for proper commutation, the clamping diodes will only carry a small average current. As a result, they can be rated at a fraction of the current rating of the main switches, reducing their cost significantly. The use of high instantaneous currents but low average currents in low current rated devices has been previously applied to soft switching topologies as a cost saving measure [6]. Hence the inverter is actively operated as a two level inverter using the space vector diagram shown in Fig. 2. Operation by actively using the level 1 switching states shown in Fig. 2 is therefore not allowed for this NPC inverter with smaller diode ratings.

Since many micro controllers and motor control DSP's have embedded hardware or software to execute the traditional two-level PWM method, it is desirable to formulate the proposed PWM method for the NPC inverter to take advantage of these embedded functions. This would eliminate the need to encode a three-level PWM modulator. This embedded two-level PWM architecture in the controller is well suited to the proposed PWM method since the dead time that is inserted by the embedded architecture can be used to generate the level 1 output for this NPC inverter. The high and low level outputs of the two-level modulator are used as level 2 and level 0 outputs for the proposed PWM method respectively. Fig. 3 shows how the two-level modulator can be used in conjunction with two low cost inverter gates to generate the four required gate signals for each phase of the NPC inverter.

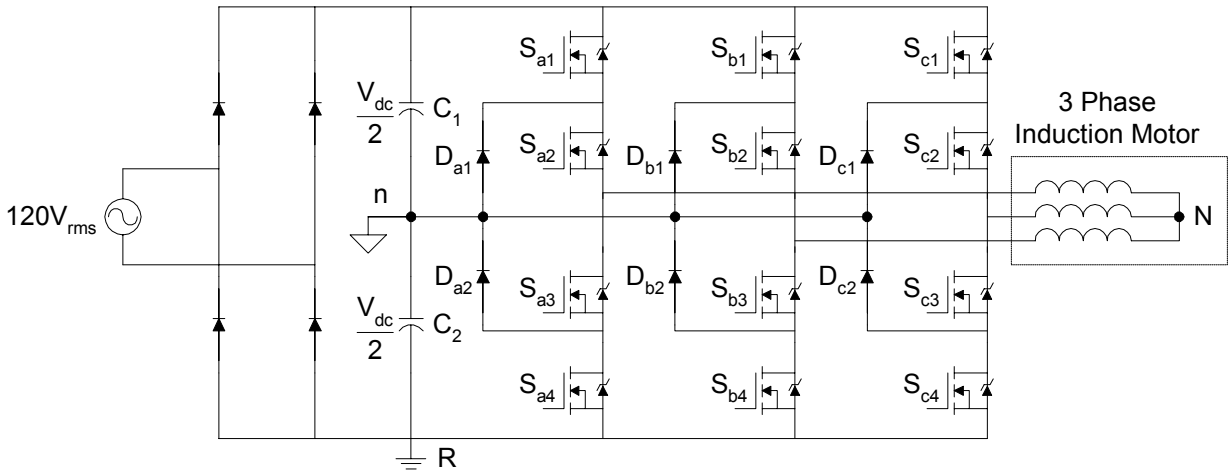


Fig. 1: Neutral point clamped three-level inverter driving a three-phase induction motor.

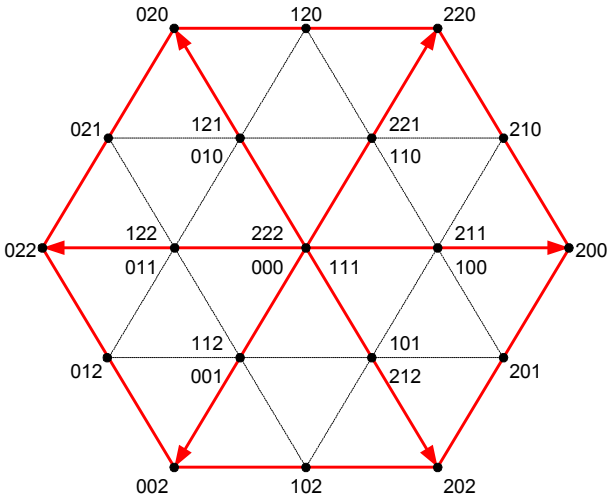
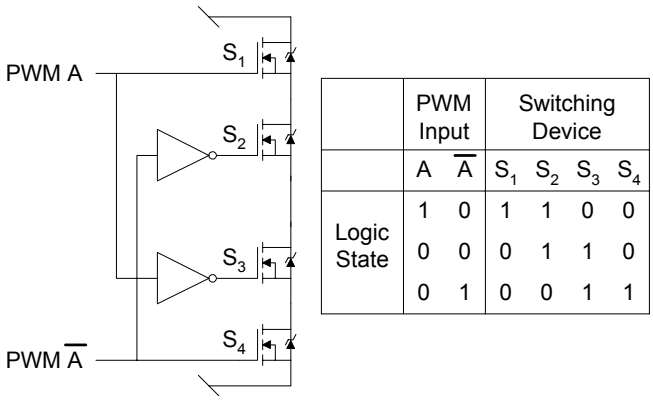


Fig 2: Space vector diagram with two-level operation in solid lines, traditional three-level diagram shown dashed.



	PWM Input		Switching Device			
	A	Ā	S_1	S_2	S_3	S_4
Logic State	1	0	1	1	0	0
	0	0	0	1	1	0
	0	1	0	0	1	1

Fig. 3: Generation of the four gate signals using the outputs of a two-level PWM modulator.

It is important to note that employing logic gates to derive four PWM gate signals from the two signals from the modulator implies that there will be no inherent software based dead-time in this three-level NPC inverter. The consequences of this can be minimized with proper design of the converter. For the proposed converter, careful attention was paid to the gate driver design so that turn-on and turn-off switching and delay times were matched so that a shoot-through condition is avoided. As an alternative, or as an extra precaution, a passive dead-time lockout circuit using discrete components could be employed.

III. Gate Drive Circuitry

The gate drive design for the proposed control method for the NPC inverter requires careful consideration of economic issues for the target low cost application and timing issues relating to dead-time and shoot-through issues as discussed in the following two sections:

A. Gate Drive Power Supplies

Charge pump or bootstrap circuits have been the circuits of choice to achieve the gate drive power supplies for low cost two level inverters since they provide the required power supplies referenced to the ground of each switch without the use of expensive transformers to create each supply. This paper extends their use to the three-level NPC inverter. This four level charge pump shown in Fig. 4 works as follows: A single low voltage gate drive power supply, V_{G4}, is referenced to the negative dc bus. When the switch S_4 is turned on, V_{G3} is charged through diode D_{G3}. Since S_3 now has a power supply, S_3 and S_4 can both be turned on. This will charge V_{G2} through D_{G2} and recharge V_{G3}. Finally, V_{G1} is charged by V_{G2} through D_{G1} by turning on S_2. As a result, after this startup sequence, each of the gate drive power supplies is charged during each PWM cycle with the size of the capacitor determining the length of holdup time that each switch can remain on without the respective gate drive supply

recharging. Due to the holdup time requirements, it is unlikely that this charge pump circuit would be practical to be compatible with six-step operation of the drive. However, this limitation is common to all bootstrap circuits such as this.

When using the proposed control method, V_{G3} and V_{G2} are charged during a level 0 output, V_{G2} and V_{G1} are charged during a level 1 output, and V_{G1} is charged during a level 2 output.

This charge pump has several practical restrictions that must be considered during the design process. The charging diodes need to be rated to block the full dc link voltage instead of only half like the main switching devices. Economically, this is of no consequence as the price of low power switching diodes is not dependant on voltage. It is also important that the worst-case device voltage drops be considered when deciding what voltage to use for the one independent supply of V_{G4}. For example, the voltage ultimately at V_{G1} will be the supply voltage V_{G4} minus three main switching device drops (S_4, S_3, and S_2) and two charging diode drops (D_{G2} and D_{G1}). Furthermore, the minimum capacitance chosen for V_{G3} and V_{G2} must, for practical purposes, be larger than the other capacitors since they serve as the source of charge during parts of the PWM control cycle.

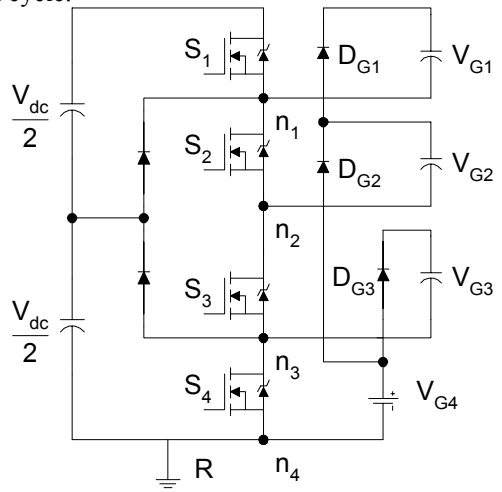


Fig 4: Phase leg shown with connections of the four-level charge pump for gate drive power supplies.

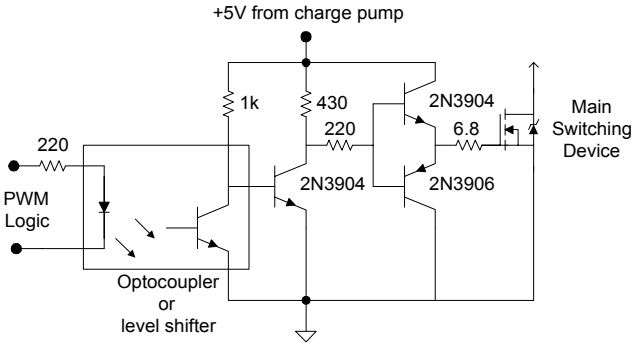


Fig. 5: Individual gate driver circuit design.

B. Gate Driver Topology

A gate drive circuit based on low cost discrete components was designed as shown in Fig. 5. The PWM input signal to the gate driver was obtained through an optocoupler for purposes of this paper. While this provides superior performance, it is likely that some other form of level shifter or pulse transformer would provide the required performance at a lower cost. The gate driver itself is composed of three small TO-92 NPN and PNP transistors and four resistors.

For this paper, the gate drive power supply voltage was set to a nominal 12 V referenced to the bus ground, R, at the lower most switch. In order to obtain consistent switching performance for the four gate drivers and switches in each phase, the nominal 12 V gate drive power supply obtained by the charge pump was regulated via a low-cost 5 V zener diode in series with a resistor. This regulated voltage helps ensure consistent turn-on and turn-off delay times between the devices as the miller plateau voltage of the MOSFETs used was approximately 3 V, hence the gate drive current during charging and discharging of this gate capacitance is not substantially different.

III. Experimental Results

To verify the operation of proposed converter and control, a hardware prototype was constructed with 150 V, 12 A IRL3215 MOSFETs and 200 V, 1 A UF1003 clamping diodes. The prototype inverter is shown in Fig. 6. Experimental results of the three-phase system are shown in Figs. 7–14. All of the results presented here were obtained with the inverter connected to the induction motor described in the Appendix. The inverter was operated using an open loop V/f control method. The motor was unloaded, operating at 60Hz and at rated flux. The average dc bus voltage was 152V obtained from a nominal 120 V_{rms}, 60 Hz input.

Fig. 7 shows the pre-regulated output voltages of the charge pump circuit. This result verifies the proposed charge pump circuit as a low cost method to obtain the individually referenced gate drive power supplies. In the figure, some

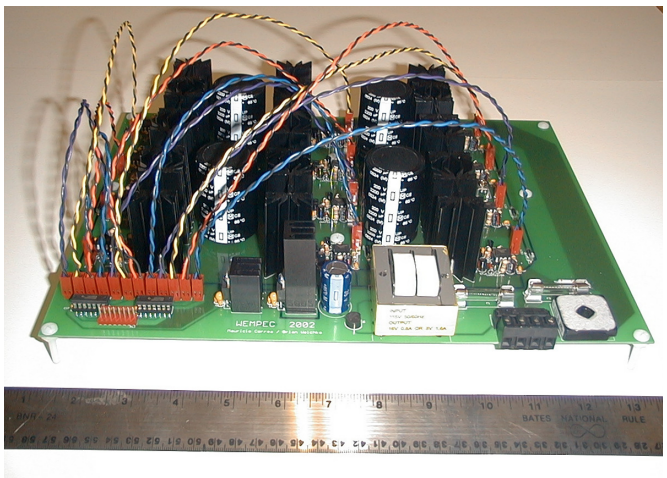


Fig. 6: The constructed three-level NPC inverter.

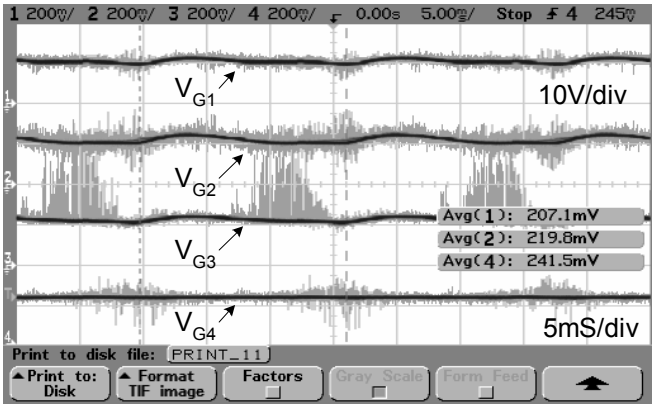


Fig. 7: Pre-regulated gate drive supply voltages obtained via the charge pump. Ch1–V_{G1}, Ch2– V_{G2}, Ch3– V_{G3}, Ch4– V_{G4}. 10V/div.

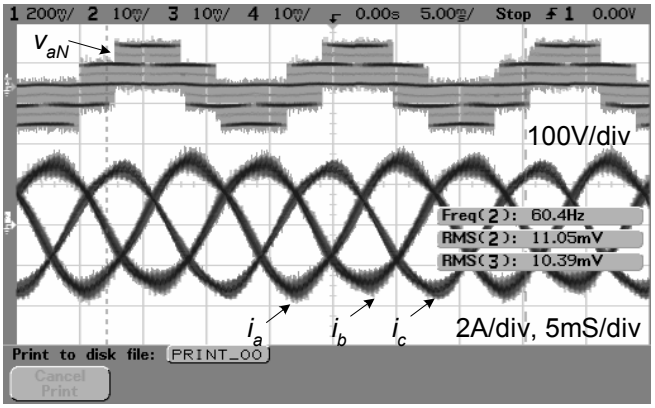


Fig. 8: Motor phase *a* voltage and phase currents. Ch1–v_{aN} (100V/div), Ch2–i_a, Ch3–i_b, Ch4–i_c (2A/div)

variation with the output fundamental output frequency (60 Hz) is seen due to the change in load current, and hence, switch voltage drops throughout the cycle. On average, the voltage drops from 12.07 V at the lower referenced supply to 10.35 V at the upper most referenced supply due to these device drops. The noise seen in this figure is a consequence of using the main switches in the charge pump circuit since any ringing on their drain-to-source voltage due to switching is propagated through to the 12 V outputs of the charge pump.

Fig. 8 shows the phase voltage and current waveforms produced by the inverter. The fundamental phase output voltage had a value of 45.4 V_{rms} as measured by a spectrum analyzer. The phase currents shown are high quality sinusoids and are well balanced despite the open-loop nature of the control algorithm.

Fig. 9 shows the drain-to-source voltages of the phase *a* devices during a typical PWM cycle. Some coupling on the dc bus voltage is seen from the operation of the other phases as evidenced by the voltage spikes when this phase is not switching. The switching frequency of the converter was 10 kHz. From this picture, it is not possible to discern the presence of the level 1 output state of the converter during the transition from a level 0 to 2 or level 2 to 0 output.

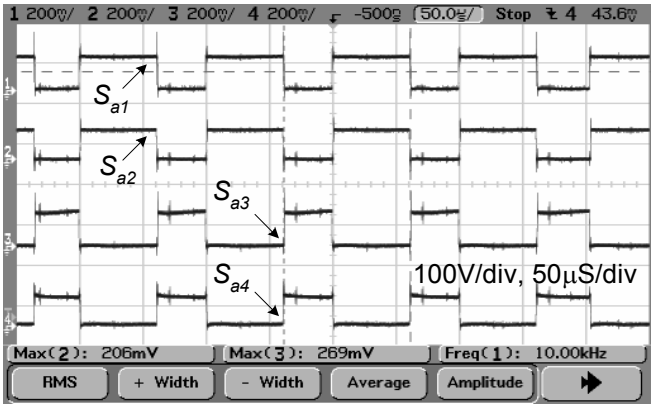


Fig. 9: Drain-to-Source voltages during a typical PWM cycle. Ch1–S_1, Ch2–S_2, Ch3–S_3, Ch4–S_4. 100V/div.

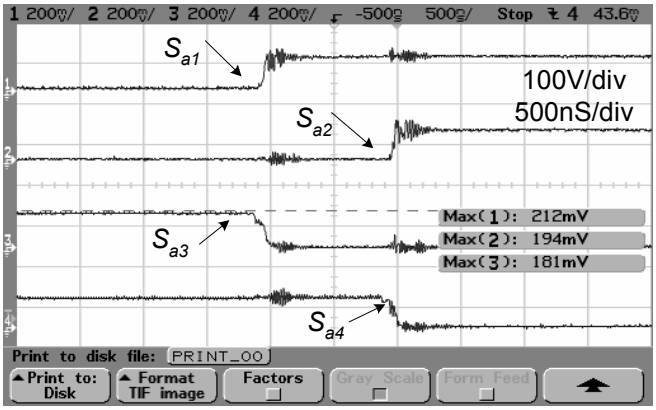


Fig. 10: Drain-to-Source voltages during a level 2 to level 0 output transition. Ch1–S_1, Ch2–S_2, Ch3–S_3, Ch4–S_4. 100V/div.

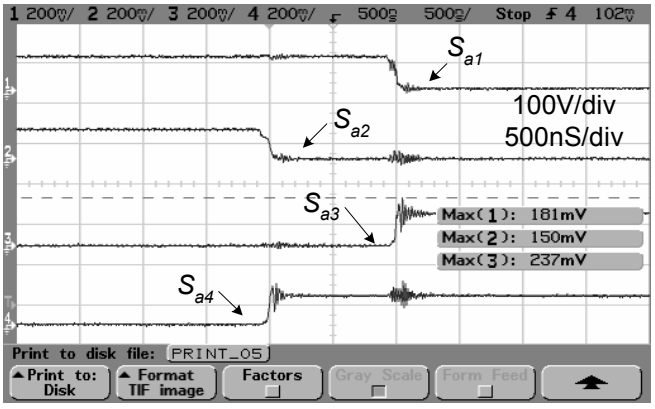


Fig. 11: Drain-to-Source voltages during a level 0 to level 2 output transition. Ch1–S_1, Ch2–S_2, Ch3–S_3, Ch4–S_4. 100V/div.

Figs. 10–11 show details of the switching behavior of the converter with Fig. 10 showing the transitions from a level 2 to level 0 output and Fig. 11 showing the transition from a level 0 to level 2 output. As seen in the figures, the time duration for the level 1 output state was set to 1 µS. This represents a loss of 2% of the output voltage capacity of the inverter since there are two transitions per PWM cycle. Due to the clamping diodes, the overshoot of the drain-to-source

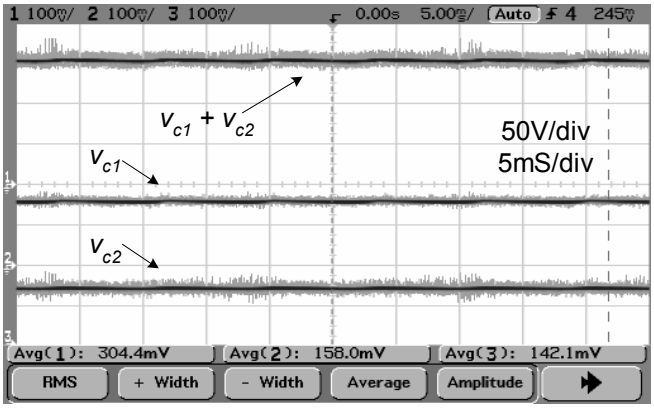


Fig. 12: Bus capacitor voltages.
Ch1−v_{c1}+v_{c2}, Ch2−v_{c1}, Ch3−v_{c2}. 50V/div.

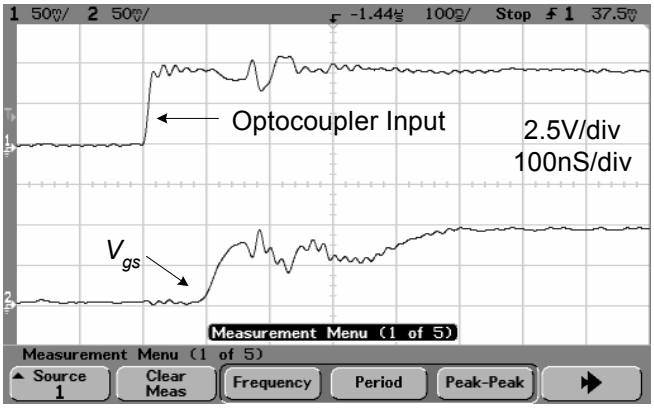


Fig. 13: Gate drive signals during turn-on.
Ch1−Optocoupler input, Ch2−v_{gs}. 2.5V/div.

voltage at turn off is limited by the bus capacitor voltages. In that sense, the bus capacitors provide a built in snubber for the switches. It is important to note, that because of the stray inductance between this snubber and the devices, along with the poor high frequency properties of electrolytic capacitors, a local snubber circuit may be needed for a particular layout and choice of devices. For the constructed prototype, no such local snubber circuit was used. Due to the clamping diodes, switching transients on one switch will affect the voltage seen by adjacent series switch. The devices in the figures are switching simultaneously and no evidence of shoot-through is present.

Fig. 12 shows the bus capacitor voltages over a typical fundamental output cycle. As seen in the figure, there is an imbalance between the two capacitor voltages of 10%. In the circuit configuration, the capacitor neutral voltage is not referenced to a fixed quantity. Without using the level 1 output as an active state, the voltage unbalance cannot be actively removed. It should also be pointed out, that by not using the active 1 state, the voltage balancing issue is the same as it would be for any two level converter employing series capacitors in the dc link. For the constructed circuit, small 10 kΩ resistors were used as bleeder resistors on each capacitor. These resistors provided the only balancing necessary for the constructed drive.

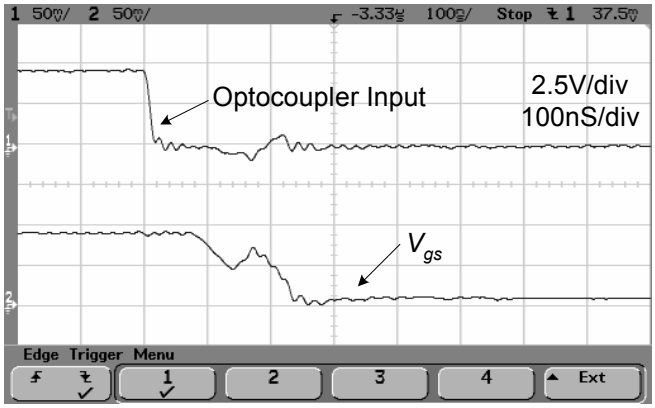


Fig. 14: Gate drive signals during turn-off.
Ch1−Optocoupler input, Ch2−v_{gs}. 2.5V/div.

Figs. 13−14 show the switching performance of the gate drive circuit from the input to the optocoupler to the gate-to-source voltage of one of the main switches. From the figure, it takes about 500 nS to switch on and 300 nS to switch off. The difference is due to the plateau voltage of the device which is 3 V. During switch-off, the voltage across the gate resistor is 2 V while it is 3 V during turn-on. This difference was used as an effective dead time control since it is desirable for the devices to turn off faster than they turn on in order to avoid any possibilities for shoot-through failures.

IV. Conclusion

This paper has proposed a new PWM control method for a three-level NPC inverter. It operates the three-level inverter effectively as a two-level inverter. This allows for a significant reduction in the rating requirements of the clamping diodes, which would result in a lower cost implementation of this topology. The paper also extends the NPC topology to the use of a charge pump circuit as a method to obtain the required independently referenced gate drive power supplies. This charge pump circuit eliminates the need for individual power transformers for each of the gate drive supplies which significantly reduces the cost and size of these required supplies. With these proposed methods, a low power motor drive was constructed using inexpensive high-volume low-voltage power MOSFETs and other low cost discrete components. Thus the paper demonstrates the possibility of basing a low power motor drive around inexpensive power MOSFET switches that previously could not be used due to voltage limitations.

While the proposed converter was constructed using discrete power devices, it should be noted that the two-level control principle and four-level charge pump make this topology attractive for integration into a single device package much like a standard six-pack arrangement. With the lower voltage rating requirement of the main switches, and the familiar and standard two-level control principles, this topology could become even more economical than a standard two-level inverter depending on what future device dies are developed and manufactured. This is important since

the trend of integration into standard packages and automated manufacturing focus attention on performance and total cost while making the actual topology inside the package of lesser importance.

APPENDIX

MACHINE PARAMETERS

The 1 hp 5000 rpm 2-pole 115/230-V three-phase squirrel-cage-rotor dual-wound-stator induction machine used for this paper had the following characteristics when configured for low-voltage operation:

$$R_1 \approx 0.50\ \Omega \qquad R_2 \approx 0.35\ \Omega$$

$$L_1 \approx L_2 \approx 1.9\ \text{mH} \qquad L_m \approx 55\ \text{mH}$$

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