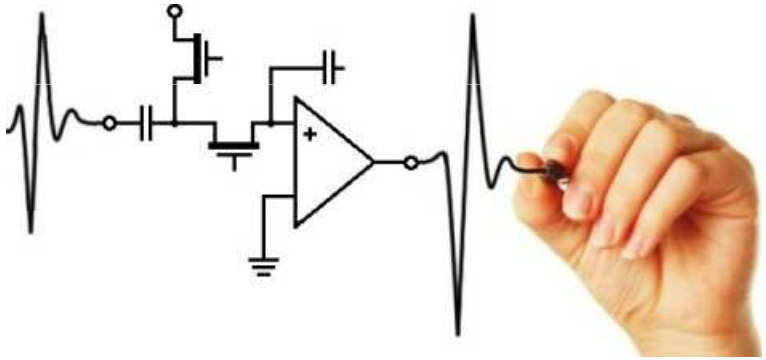
Semi-Empirical Optimization of CMOS Low-noise Amplifier for Biomedical Data Acquisition



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- Amplifier for Biomedical Data Acquisition
- Optimization Methodology:
  - Orthogonal-Convex Optimization
  - All-Inversion Region MOS Model
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Prologue

- Design of neural recording interfaces.

  [for biomedical measurements]
- Generic structure of neural recording interfaces.
- Low-Noise Amplifier (LNA): A Key Element.
- Design challenge.

  [stringent noise-power-area trade-off]
- Application domain of biomedical LNAs.

  [ECG, EEG, EMG]

Amplifier for Biomedical Data Acquisition

- Capacitive feedback network (CFN) topology.
- Prerequisites.

  - low power, low input-referred noise and high CMRR
- ♥ of the CFN LNA: Preamplifier.

Table 1

Signal	Frequency (Hz)	Amplitude (V)
ECG	$0.05 - 250$	$5\times10^{-6} - 8\times10^{-3}$
EEG	$0.5 - 200$	$2\times10^{-6} - 200\times10^{-6}$
EMG	$0.01 - 10\times10^{3}$	$50\times10^{-6} - 10\times10^{-3}$

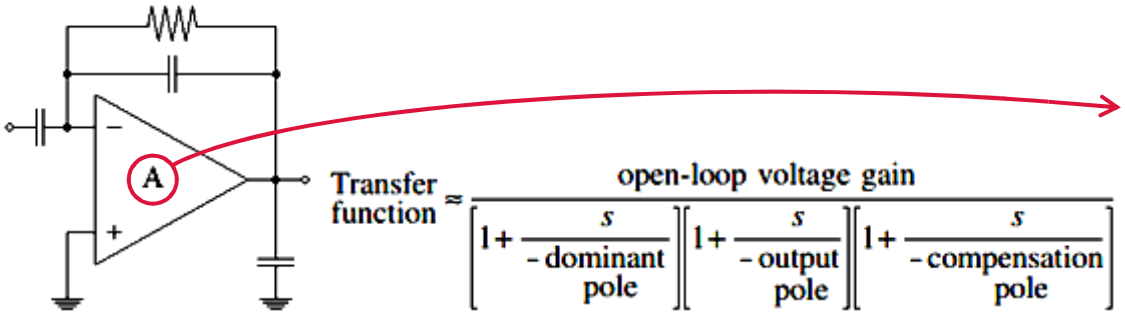


Figure 1

$$\text{Transfer function} \approx \frac{\text{open-loop voltage gain}}{\left[1+\frac{s}{-\text{dominant pole}}\right]\left[1+\frac{s}{-\text{output pole}}\right]\left[1+\frac{s}{-\text{compensation pole}}\right]}$$

Figure 2

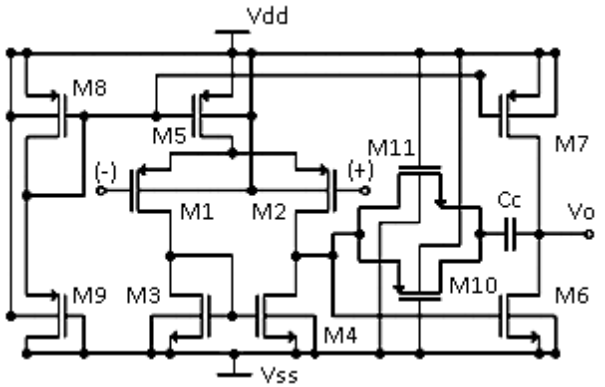
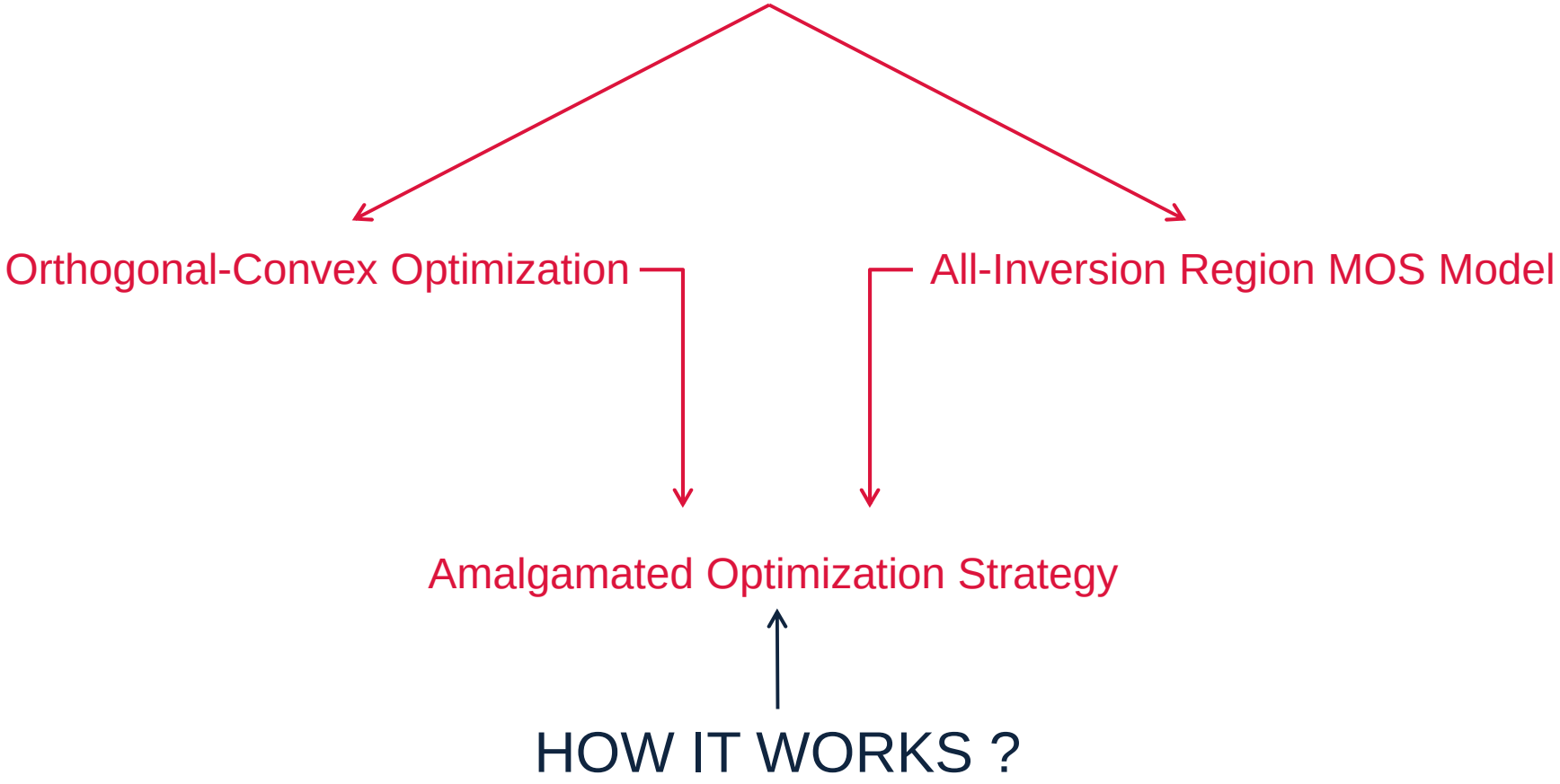


Figure 3

Optimization Methodology



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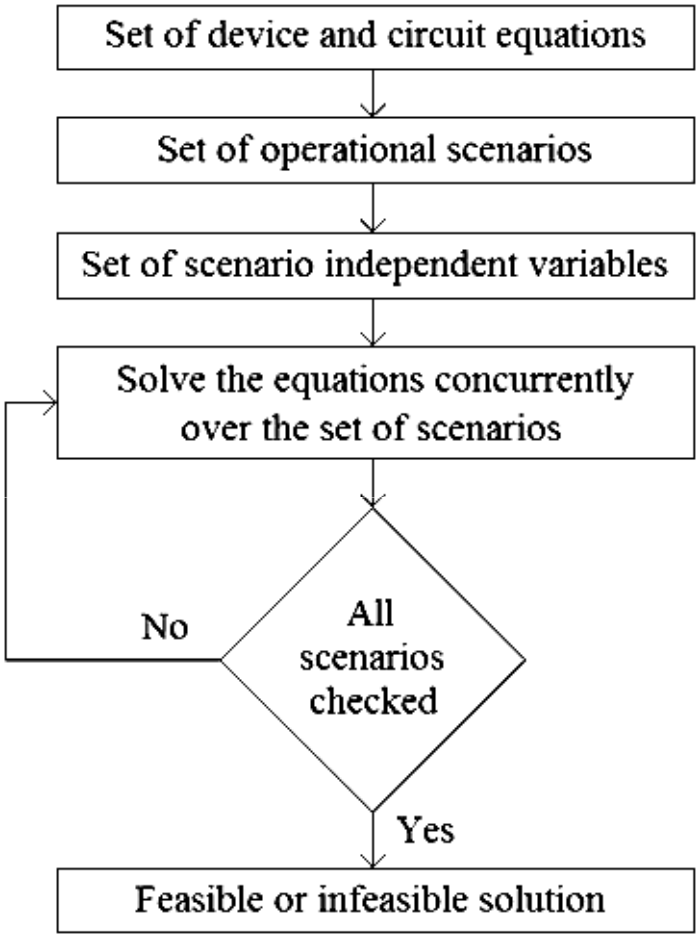

Figure 4

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Orthogonal-Convex Optimization

- Objective & Constraint Based Optimization.
- Problem Formulation:

$$\begin{aligned} \text{optimize} \quad & f_0(x) \\ \text{subject to} \quad & f_i(x) \le 1, \quad i = (1,\ldots,m) \\ & g_i(x) = 1, \quad i = (1,\ldots,p) \\ & x_i > 0, \quad i = (1,\ldots,n) \end{aligned}$$

- Monomial & Posynomial:

$$g(x) = c x_1^{a_1} \ldots x_n^{a_n} \qquad f(x) = \sum_{k=1}^{K} c_k g_k(x)$$

- Logarithmic Transformation of Variables.

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All-Inversion Region MOS Model

- Inversion Coefficient of MOSFET Optimization.

$$ICF = \frac{I_D}{I_0 S} \qquad I_0 = 2n\mu C_{OX}\phi_T^2$$

Weak Inversion: ICF < 0.1

Strong Inversion: ICF > 10

Moderate Inversion: 0.1 < ICF < 10

- Transconductance Efficiency.

$$\frac{g_m}{I_D} = \frac{1}{n\phi_T}\frac{2}{\left(1+\sqrt{ICF+1}\right)}$$

Design Formulation

- Objective: Minimize Power Dissipation
- Constraints:

  - gain-bandwidth, voltage gain, common-mode rejection ratio, slew-rate, phase margin, noise spectral density
- Upper and/or Lower Bounds on Design Parameters.
- Example 1:

Open-loop Gain = Gain of 1st Stage x Gain of 2nd Stage

$$= \left(\frac{g_{m2}}{g_{o2}+g_{o4}}\right)\left(\frac{g_{m6}}{g_{o6}+g_{o7}}\right)$$

$$= \frac{\left(\frac{g_{m2}}{I_{D2}} I_{D2}\right)}{\left(\frac{I_{D2}}{V_{A2}}+\frac{I_{D4}}{V_{A4}}\right)} \frac{\left(\frac{g_{m6}}{I_{D6}} I_{D6}\right)}{\left(\frac{I_{D6}}{V_{A6}}+\frac{I_{D7}}{V_{A7}}\right)}$$

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- Example 2:

Nulling Active Resistor = Rz

$$= \frac{1}{g_{m6}}$$

$$= \frac{1}{\frac{g_{m6}}{I_{D6}} I_{D6}}$$

- Design Summary:

[180-nm BSIM3 CMOS Model]

Table 2

Transistor length	$0.18\mu m \leq L \leq 1.8\mu m$
Device width	$0.18\mu m \leq W \leq 180.0\mu m$
Supply voltage	1.25V
Load capacitance	1pF
Oxide thickness	4.1nm
Open-loop voltage gain	≥ 60dB
Common-mode rejection ratio	≥ 60dB
Gain-bandwidth	≥ 1MHz
Slew-rate	≥ 1V/μS
Phase margin	≥ 60°
Input-referred noise	≤ 450nV/√Hz
Power	Minimize

Result Interpretation

- 2-Tier Process: Estimation and Verification.

Table 3

Transistor length	$L_1 = L_2$	1.8µm
	$L_3 = L_4$	1.8µm
	$L_5 = L_7 = L_8$	1.43658µm
	L_6	1.8µm
Transistor width	$W_1 = W_2$	180µm
	$W_3 = W_4$	180µm
	W_5	180µm
	W_6	20.87414µm
	W_7	10.43707µm
	W_8	1.43658µm
Nulling active resistance	R_Z	420.7278kΩ
Compensation capacitance	C_C	1.780275pF
Open-loop voltage gain	G	80.0dB
Common-mode rejection ratio	$CMRR$	82.70868dB
Gain-bandwidth	GBW	22.44995MHz
Slew-rate	SR	1V/µS
Phase margin	PM	78.07401°
Input-referred noise	$S_{in}(f)$	319.6656nV/√Hz
Power	P	64.8477µW

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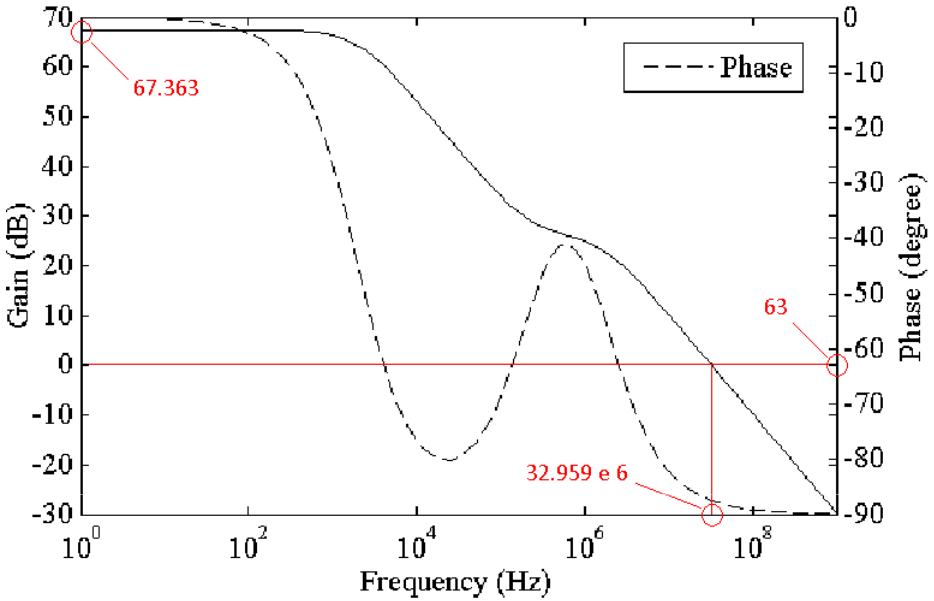

Figure 5

Table 4

Parameter	This method	SPICE	Unit
G	80.0	67.363	dB
CMRR	82.70868	94.124	dB
GBW	22.44995	32.959	MHz
SR	1	1.45	V/μS
PM	78.07401	63	degree
P	64.8477	64.8476	μW

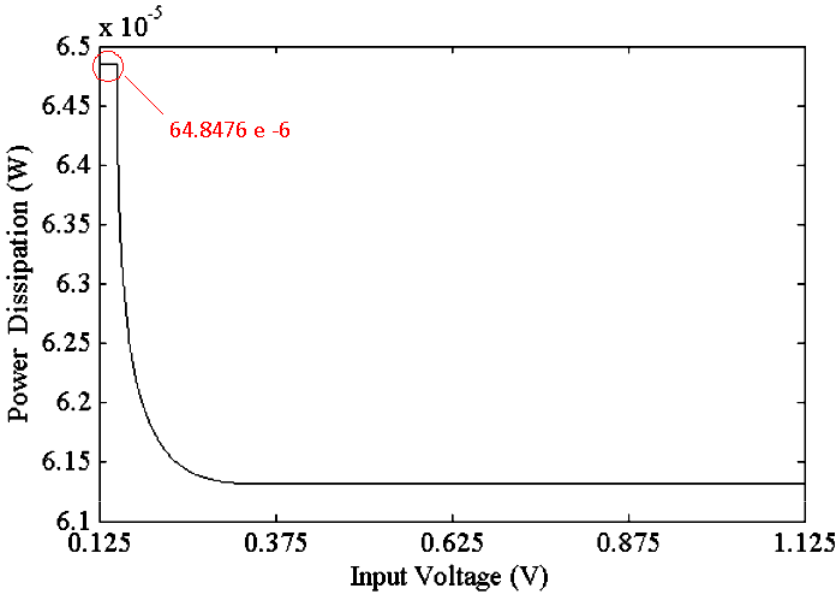

Figure 6

Epilogue

- Amalgamated Optimization Strategy:

  effectiveness of Orthogonal-Convex Optimization

  +

  flexibility of All-Inversion MOSFET Model

- Pertains Prompt & Globally Optimal Solutions.
- Increased Fidelity and Flexibility of Design.
- Rigorous Initial Computation.
- Limited Function Handling Capability.

"Further Accuracy is Achievable by Adopting Judicious Design Strategies"

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QUESTIONS / SUGGESTIONS

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