

Digitally Reconfigurable Two DVCC Based Biquadratic Analog Filter

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Abstract In this paper, a digitally reconfigurable Multi Input Single Output (MISO) voltage mode multifunctional biquadratic analog filter has been presented. The circuit has three input terminals and one output terminal. It employs two Differential Voltage Current Conveyor blocks (DVCC), two capacitors and two resistors. Filter responses like low-pass, band-pass, high-pass and band-reject can be obtained from the same topology by applying voltages to different input terminals. The digital re-configurability is obtained using a current-summing network (CSN). Cut-off frequency of the various filter responses is controlled and varied with the help of a 3-bit digital control word. Further quality factor is also controlled with the 3-bit control word. PSPICE simulations using TSMC 0.25 μ CMOS technology have been performed to validate the theoretically predicted results.

Keywords: Voltage-mode, Differential Voltage Current Conveyor (DVCC), analog filter, digitally reconfigurable circuits, cut off frequency, quality factor, second-generation current conveyor, biquadratic filter

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1. Introduction

Recently current mode circuits due to their various advantages like wider bandwidth, greater linearity, higher slew-rate, better dynamic range, simple circuitry and lower power consumption have achieved considerable popularity over the voltage mode circuits [1]. Although voltage mode circuits served the purpose for a long period but current mode circuits came as an improvement.

Communication, analog signal processing, instrumentation and automatic control are some of the application fields of current mode circuits. Apart from this the most significant use is in the realization of the current mode filters and oscillators. These significant application areas and demands led to the development of a number of current mode active building blocks [2,3].

CCII (Current Conveyor Second Generation) became the first in this area [4] which proved to be the most popular and successful current mode building block. Although it provided all the advantages of current mode circuits but there were some limitations associated with it. CCII does not provide with the proper solution to an application demanding differential or floating inputs. For example impedance converter circuits and current-mode instrumentation amplifiers, which also require two high input impedance terminals, a single CCII block was no more sufficient. Further these applications employed floating elements to minimize the number of CCII blocks used. Keeping these drawbacks into consideration some

new building blocks were introduced to serve the purpose. In 1996 differential difference current conveyor (DDCC) was presented [5] followed by differential voltage current conveyor (DVCC) in 1997 which came as a modification in DDCC block. DVCC was actually DDCC block having its Y_3 terminal grounded [6].

This new modified building block named DVCC provided a sufficient solution to the drawbacks of CCII. It enhanced the performance of the existing CCII. Various works have been done on DVCC in the recent literature along with its scope in a large number of application areas. In this field some of the recent works includes a DVCC Based High Input Impedance Voltage-Mode Multifunctional filter by Jiun-Wei Horng. In this all-pass, high-pass and low-pass signals were obtained simultaneously from the same circuit configuration [7]. Later Hua-Pin Chen, Kuo-Wei Huang, and Po-Ming Huang introduced a voltage-mode First-Order Filter based on DVCC which simultaneously realized low-pass, high-pass and all-pass filter responses from the same configuration. Lesser number of active and passive components were used here [8]. More recently Iqbal A. Khan and Ahmed M. Nahhas came up with a digitally controlled current conveyor. It has been used to realize a digitally controlled voltage mode first order filter [9].

In this paper the circuit proposed in [10] by Jiun-Wei Horng, Maw-Huei Lee, Hsi-Chih Cheng and Chia-Wen Chang employing two second generation current conveyors (CCIIs) and four passive components has been modified and implemented using DVCC further it is also used to design and implement a digitally reconfigurable

voltage-mode multifunctional biquadratic filter. The second-order low-pass, band-pass, high-pass and band-reject responses along with the quality factor variation of the band-pass filter can be realized without changing the circuit topology which further enhances the circuit versatility. PSPICE simulations of the CMOS based reconfigurable multifunctional filter are performed to demonstrate results.

2. DVCC

The DVCC block is as shown in the Figure 1. It is a five-terminal active building block. The terminal characteristics of DVCC can be described by the following matrix equation: [11]

$$\begin{pmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z+} \\ I_{Z-} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_{Y1} \\ I_{Y2} \\ I_X \\ V_{Z+} \\ V_{Z-} \end{pmatrix} \quad (1)$$

While the X terminal voltage (V_X) follows the voltage difference of terminals Y_1 and Y_2 ($V_{Y1} - V_{Y2}$), the output currents I_{Z+} and I_{Z-} follow the input current injected at the X terminal (I_X), where I_{Z+} is the positive-type output current and I_{Z-} is the negative-type.

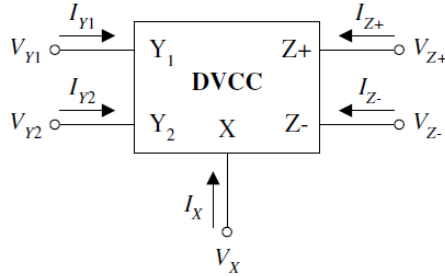


Figure 1. Symbolic representation of the DVCC [11]

An ideal DVCC exhibits an input resistance of zero value at the terminal X whereas both the Y terminals as well as the Z terminal have infinite resistance. The current flow direction at the output and the input terminals is such that either both currents flow into or out of the device. The CMOS implementation of DVCC is as shown in Figure 2.

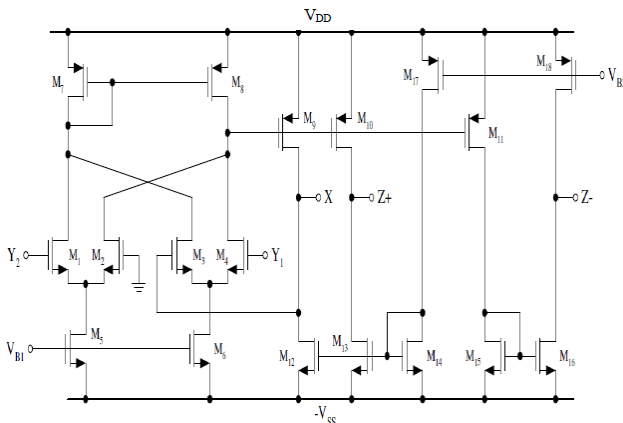


Figure 2. CMOS realization of the dual-output DVCC [11]

3. Implementation of the Dvcc Filter

The implemented voltage-mode multifunctional filter [11] is illustrated in Figure 3.

The analysis of the circuit yields the Eq. 2 which can be made the transfer functions of the second order voltage-mode low-pass, high-pass, band-pass and band reject response by applying voltage at different input terminals as shown in Table 1.

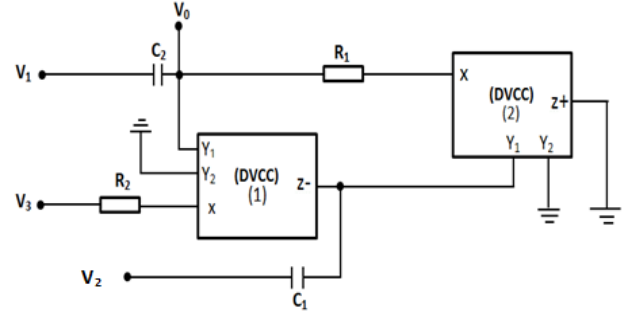


Figure 3. Circuit diagram of the multifunction biquadratic filter

$$V_0 = \frac{s^2 V_1 + s V_2 \frac{G_1}{C_2} + V_3 \frac{G_1 G_2}{C_1 C_2}}{s^2 + s \frac{G_1}{C_2} + \frac{G_1 G_2}{C_1 C_2}} \quad (2)$$

Where the resonant angular frequency ω_o , and the quality factor, Q are given as shown:

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \quad (3)$$

$$Q = \sqrt{\frac{G_2 G_2}{G_1 C_1}} \quad (4)$$

Table 1. Realization of filters with input combinations

V_1	V_2	V_3	Filter Type
V_{IN}	0	0	High-pass
0	V_{IN}	0	Band-pass
0	0	V_{IN}	Low-pass
V_{IN}	0	V_{IN}	Band-reject

We can see that low-pass, band-pass, high-pass and band-reject functions can be realized without changing the circuit topology. In simulations, using PSPICE the DVCC was realized by the CMOS implementation as shown in Figure 2 using TSMC 0.25- μ m process parameters. The aspect ratios of the CMOS transistors of the DVCC are presented in Table 2. $V_{DD} = -V_{SS} = 2$ V are the supply voltages and $V_{B1} = -1.32$ V and $V_{B2} = +0.7$ V are the two biasing voltages. The circuit was designed for $f_o = \omega_o/2\pi = 39.79$ kHz and $Q = 1$ by choosing $R_1 = 10$ k Ω , $R_2 = 1$ k Ω and $C_1 = 4$ nF, $C_2 = 0.4$ nF. The responses of the above given filter design are shown in Figure 4. The results are in accordance with the theoretical analysis.

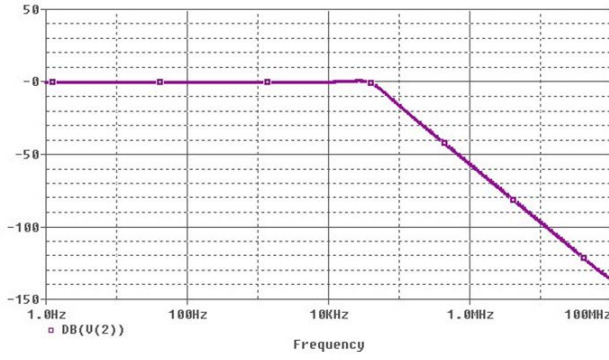


Figure 4(a). Simulated Low-pass response

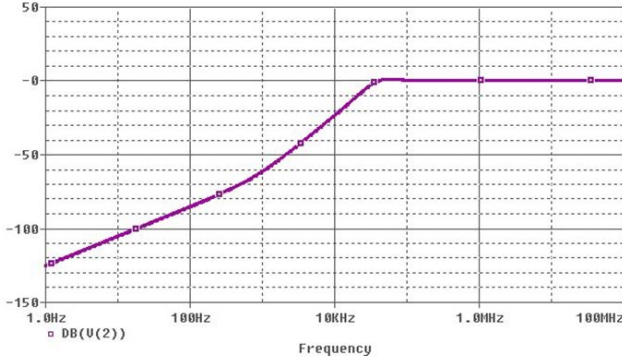


Figure 4(b). Simulated High-pass response

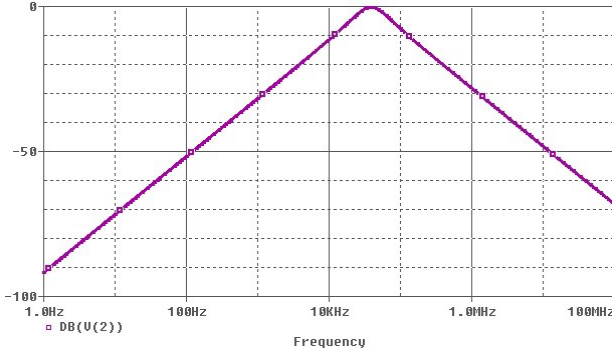


Figure 4(c). Simulated Band-pass response

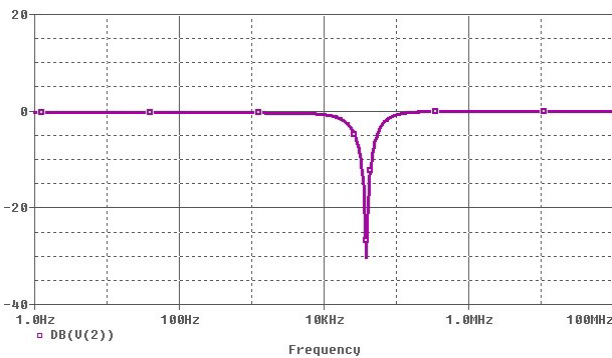


Figure 4(d). Simulated Band-reject response

Table 2. Aspect ratios of the cmos transistors of the dvcc [11]

Transistors	W (μm)	L (μm)
M ₁ -M ₄	1	0.8
M ₅ -M ₆	24.2	0.8
M ₇ -M ₈	6.8	0.8
M ₉ -M ₁₁ , M ₁₇	18.6	0.6
M ₁₂ -M ₁₄	25	0.8
M ₁₅	19.6	0.8
M ₁₆	18	0.8
M ₁₈	20	0.6

4. Digitally Controlled Dvcc (Dc-Dvcc)

To introduce the re-configurability in the multifunctional filter we have used a digitally controlled DVCC (DC-DVCC) shown in Figure 5. The modified terminal characteristics for the same are as follows:

$$\begin{pmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z+} \\ I_{Z-} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & k & 0 & 0 \\ 0 & 0 & -k & 0 & 0 \end{pmatrix} \begin{pmatrix} I_{Y1} \\ I_{Y2} \\ I_X \\ V_{Z+} \\ V_{Z-} \end{pmatrix} \quad (5)$$

For obtaining the digital control in the DVCC current summing networks (CSNs) are employed at the Z (Z+ and Z-) terminals for controlling the current transfer gain parameter k which can be varied from 1 to $(2^n - 1)$. This n represents the number of transistor arrays.

Where:

$$k = \frac{I_Z}{I_X}$$

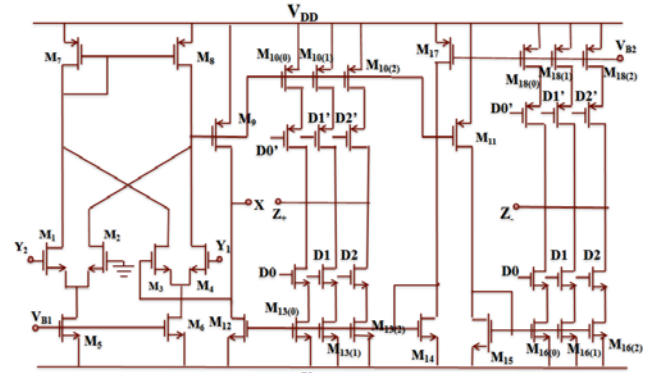


Figure 5. CMOS realization of DC-DVCC

The modified circuit of DVCC with the transistors arrays is as shown in Figure 5. The CSN consists of n transistor pairs, the aspect ratios of whose PMOS and NMOS transistors respectively are given by:

$$\left(\frac{W}{L}\right)_i = 2^i \left(\frac{W}{L}\right)_9 \quad (6)$$

$$\left(\frac{W}{L}\right)_i = 2^i \left(\frac{W}{L}\right)_{12} \quad (7)$$

Furthermore, the current at the output terminal (Z), is assumed to be flowing out of the DC-DVCC and can be expressed as:

$$I_Z = \sum_{i=0}^{n-1} d_i 2^i (I_9 - I_{12}) \quad (8)$$

Therefore, the proposed DC-DVCC provides a current transfer gain, k equal to:

$$k = \frac{I_Z}{I_X} = \frac{\sum_{i=0}^{n-1} d_i 2^i (I_9 - I_{12})}{(I_9 - I_{12})} = \sum_{i=0}^{n-1} d_i 2^i \quad (9)$$

Where d_i are the bits applied to the i -th branch in the CSN. Current flow in a particular branch is enabled or disabled depending upon whether d_i is a logic 1 or logic 0 [12].

5. Digitally Controlled Multifunctional Filter

In this section the proposed digitally reconfigurable voltage-mode multifunctional biquadratic filter has been presented as shown in Figure 6.

The introduction of the DC-DVCC comprising of CSN modifies the expression of pole-frequency ω_0 of the multifunctional filter. The expressions for the digitally reconfigurable filter responses can now be expressed as:

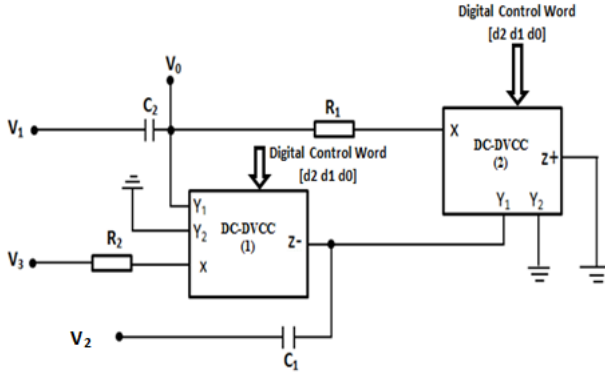


Figure 6. Proposed digitally reconfigurable voltage-mode multi-function biquadratic filter having two DC-DVCC blocks

$$V_0 = \frac{s^2 V_1 + s V_2 \frac{G_1}{C_2} + k V_3 \frac{G_1 G_2}{C_1 C_2}}{s^2 + s \frac{G_1}{C_2} + k \frac{G_1 G_2}{C_1 C_2}} \quad (10)$$

The digitally reconfigurable filters responses can be realized with different input combinations refer to Table I.

The resonant angular frequency ω_0 , and the quality factor, Q , are given by:

$$\omega_0 = \sqrt{\frac{k G_1 G_2}{C_1 C_2}} \quad (11)$$

$$Q = \sqrt{\frac{k G_2 G_2}{G_1 C_1}} \quad (12)$$

Thus according to the above equations the cut-off frequency (ω_0) and the quality factor (Q) both should show a square root variation with the control word (k).

6. Simulation Results

The proposed digitally controlled multifunctional biquadratic analog filter circuit in Figure 6 has been simulated and all the results are verified using PSPICE. Figure 7, 8, 9 and 10 shows the simulated responses obtained for the band-pass, high-pass, low-pass and band-reject filters respectively varying the digital control word $[d_2 d_1 d_0]$ from $[0 0 1]$ to $[1 1 1]$. Values of the cut-off frequency for the control word $[0 0 1]$ to $[1 1 1]$ obtained practically by simulation are recorded in the Table 3. Figure 11(a), (b), (c) and (d) are the plots showing the variation in the cut off frequency with the control word. It is to be observed that the cut-off frequency varies without changing the value of any of the passive components i.e. resistors and capacitors being used in the design.

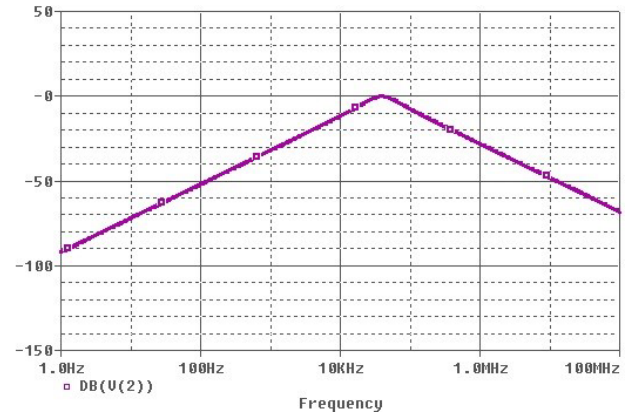


Figure 7(a). Simulated magnitude response (in dB) for band pass filter with $[d_2 d_1 d_0 = 0 0 1]$ control word selected

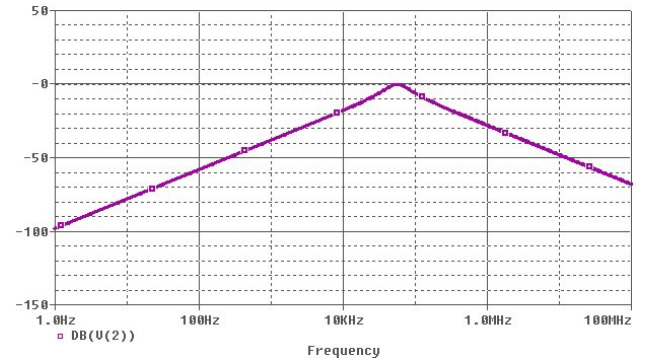


Figure 7(b). Simulated magnitude response (in dB) for band pass filter with $[d_2 d_1 d_0 = 0 1 0]$ control word selected

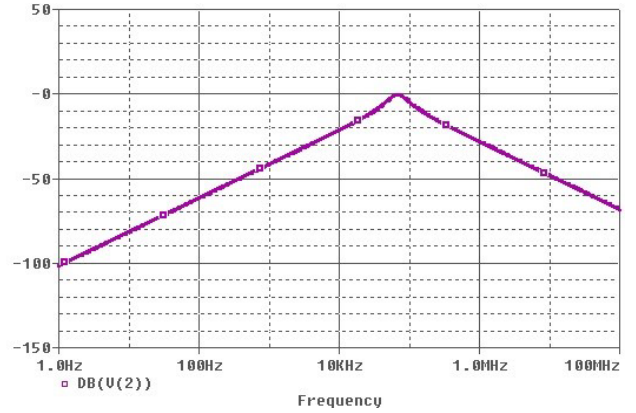


Figure 7(c). Simulated magnitude response (in dB) for band pass filter with $[d_2 d_1 d_0 = 0 1 1]$ control word selected

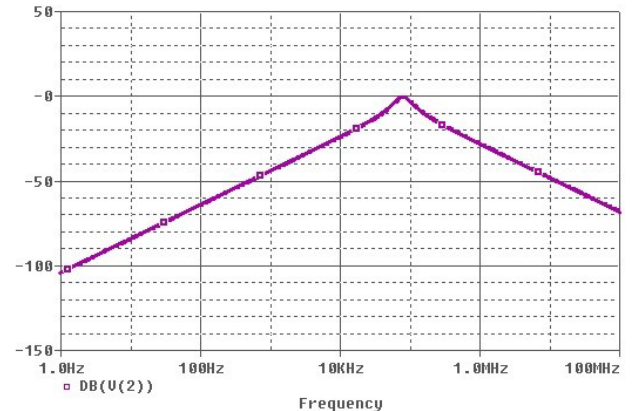


Figure 7(d). Simulated magnitude response (in dB) for band pass filter with $[d_2 d_1 d_0 = 1 0 0]$ control word selected

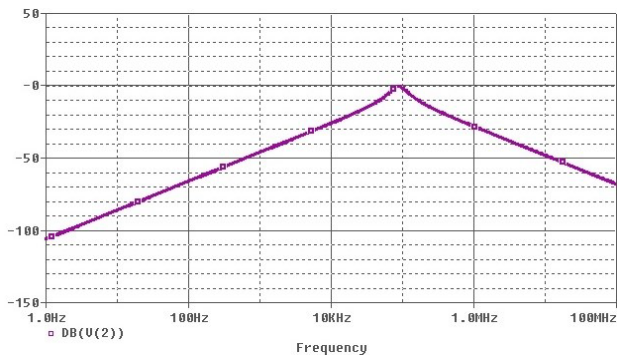


Figure 7(e). Simulated magnitude response (in dB) for band pass filter with $[d_2 d_1 d_0 = 1 0 1]$ control word selected

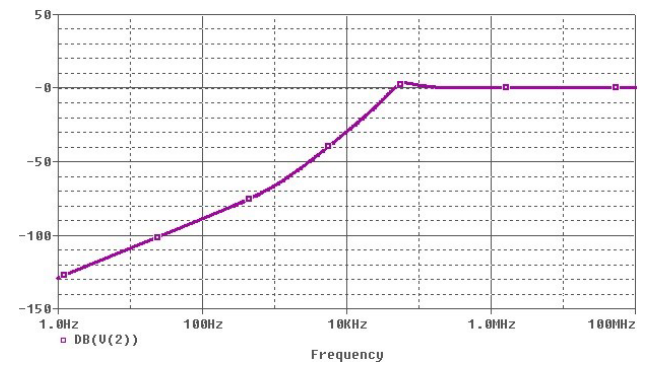


Figure 8(b). Simulated magnitude response (in dB) for high pass filter with $[d_2 d_1 d_0 = 0 1 0]$ control word selected

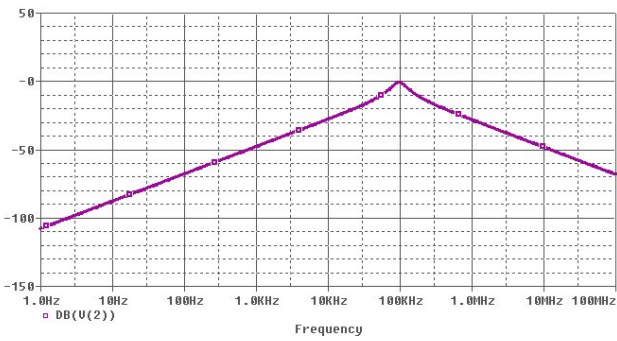


Figure 7(f). Simulated magnitude response (in dB) for band pass filter with $[d_2 d_1 d_0 = 1 1 0]$ control word selected

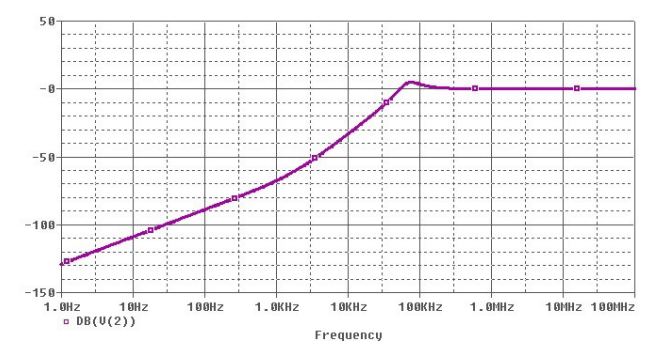


Figure 8(c). Simulated magnitude response (in dB) for high pass filter with $[d_2 d_1 d_0 = 0 1 1]$ control word selected

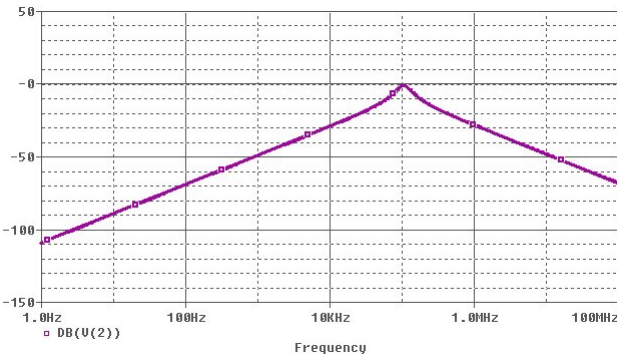


Figure 7(g). Simulated magnitude response (in dB) for band pass filter with $[d_2 d_1 d_0 = 1 1 1]$ control word selected

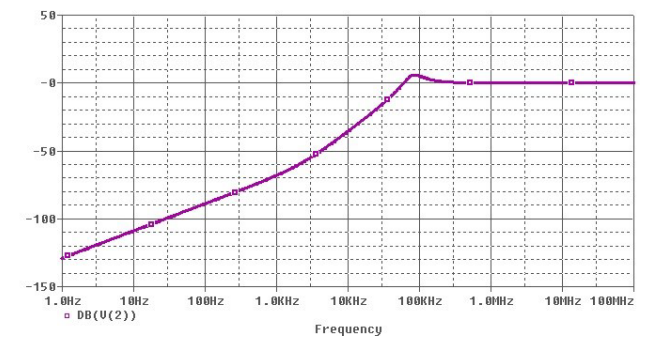


Figure 8(d). Simulated magnitude response (in dB) for high pass filter with $[d_2 d_1 d_0 = 1 0 0]$ control word selected

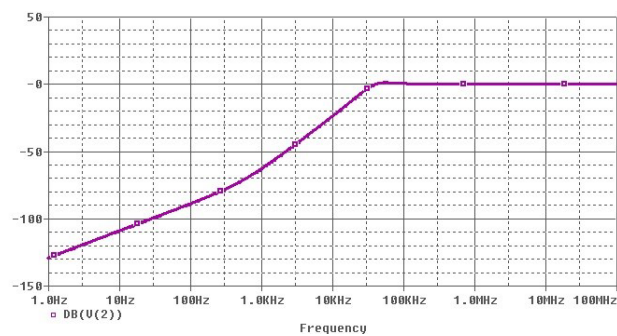


Figure 8(a). Simulated magnitude response (in dB) for high pass filter with $[d_2 d_1 d_0 = 0 0 1]$ control word selected

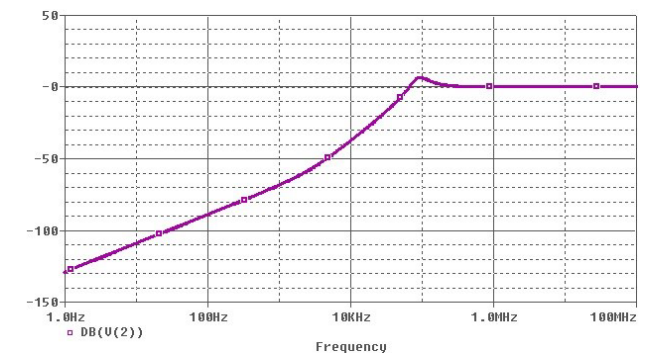


Figure 8(e). Simulated magnitude response (in dB) for high pass filter with $[d_2 d_1 d_0 = 1 0 1]$ control word selected

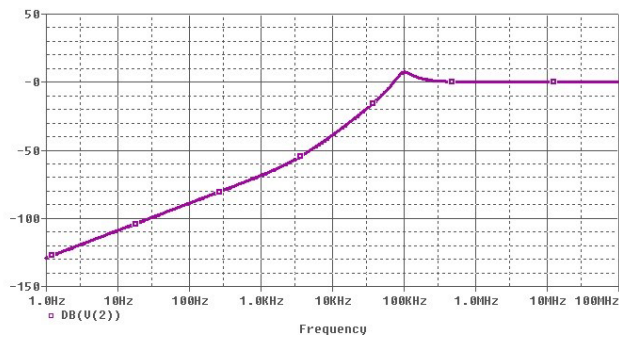


Figure 8(f). Simulated magnitude response (in dB) for high pass filter with $[d_2 d_1 d_0 = 1 1 0]$ control word selected

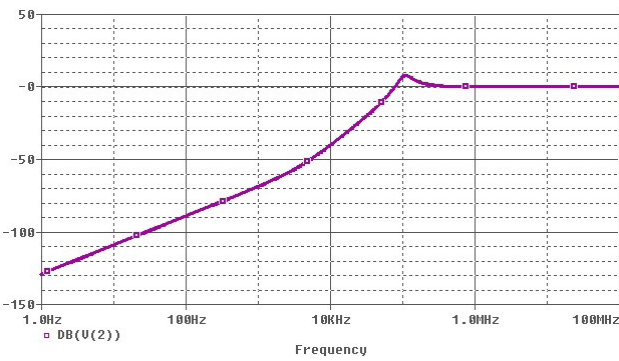


Figure 8(g). Simulated magnitude response (in dB) for high pass filter with $[d_2 d_1 d_0 = 1 1 1]$ control word selected

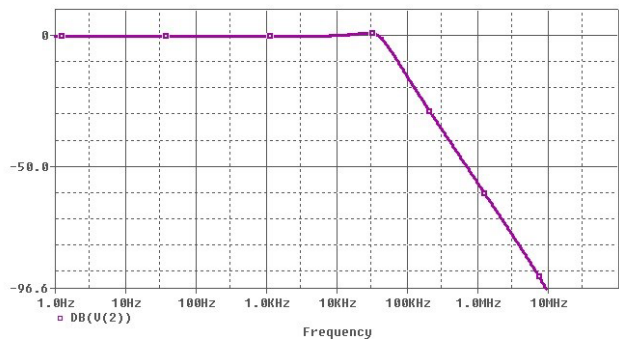


Figure 9(a). Simulated magnitude response (in dB) for low pass filter with $[d_2 d_1 d_0 = 0 0 1]$ control word selected

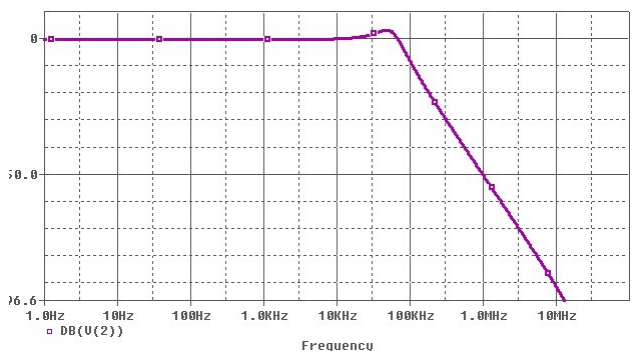


Figure 9(b). Simulated magnitude response (in dB) for low pass filter with $[d_2 d_1 d_0 = 0 1 0]$ control word selected

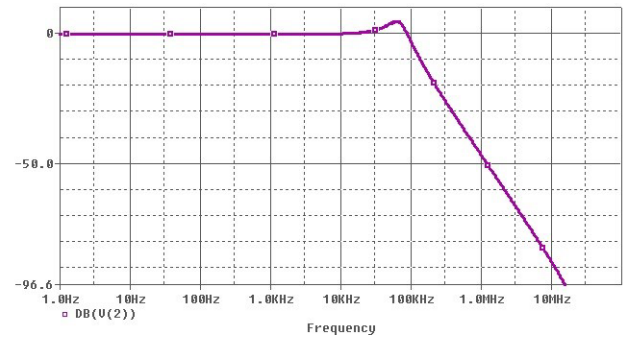


Figure 9(c). Simulated magnitude response (in dB) for low pass filter with $[d_2 d_1 d_0 = 0 1 1]$ control word selected

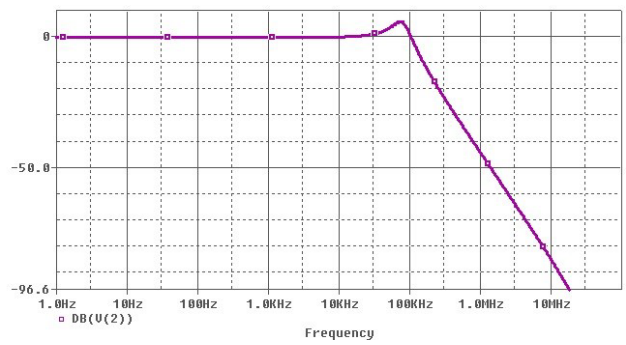


Figure 9(d). Simulated magnitude response (in dB) for low pass filter with $[d_2 d_1 d_0 = 1 0 0]$ control word selected

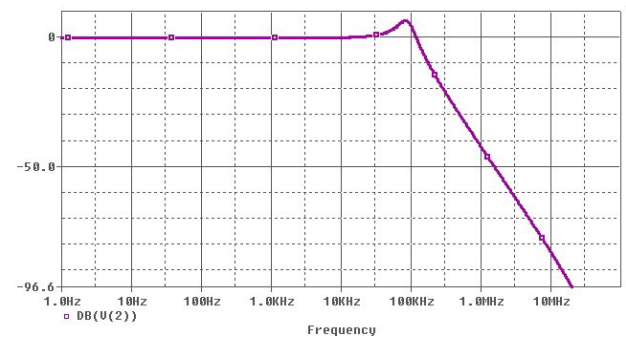


Figure 9(e). Simulated magnitude response (in dB) for low pass filter with $[d_2 d_1 d_0 = 1 0 1]$ control word selected

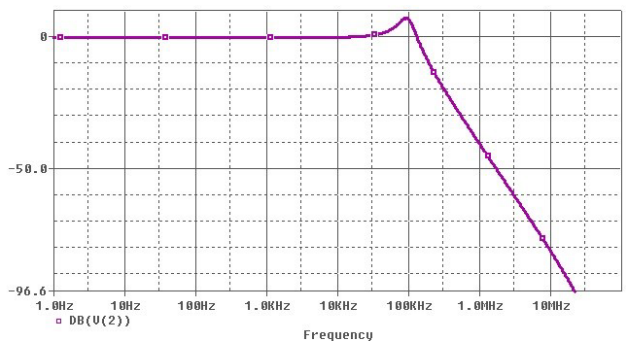


Figure 9(f). Simulated magnitude response (in dB) for low pass filter with $[d_2 d_1 d_0 = 1 1 0]$ control word selected

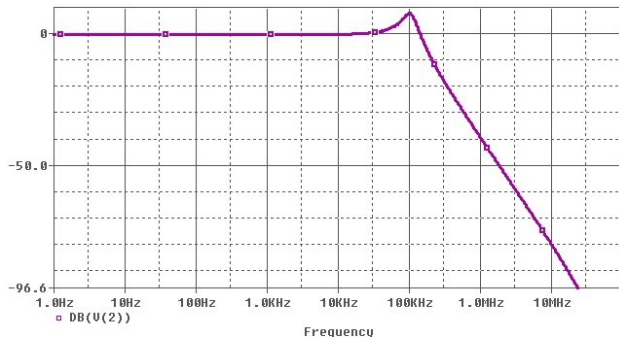


Figure 9(g). Simulated magnitude response (in dB) for low pass filter with $[d_2 d_1 d_0 = 1 1 1]$ control word selected

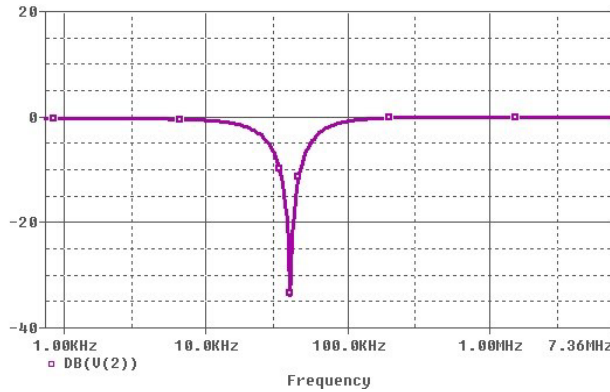


Figure 10(a). Simulated magnitude response (in dB) for band reject filter with $[d_2 d_1 d_0 = 0 0 1]$ control word selected

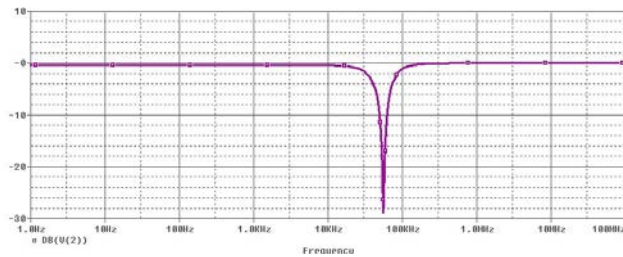


Figure 10(b). Simulated magnitude response (in dB) for band reject filter with $[d_2 d_1 d_0 = 0 1 0]$ control word selected

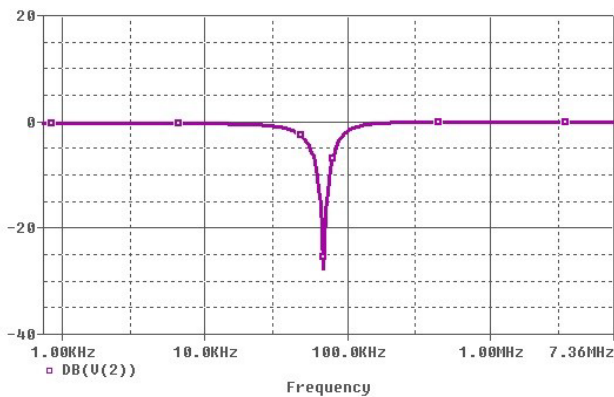


Figure 10(c). Simulated magnitude response (in dB) for band reject filter with $[d_2 d_1 d_0 = 0 1 1]$ control word selected

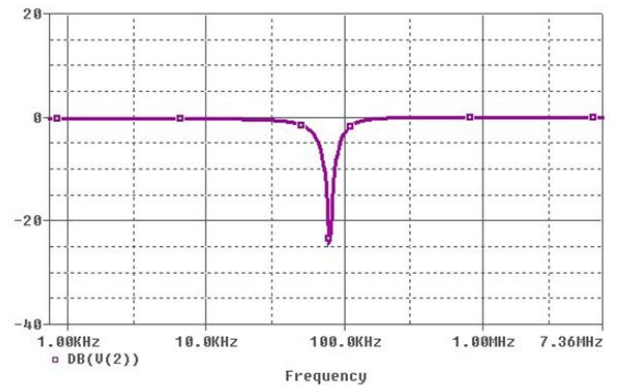


Figure 10(d). Simulated magnitude response (in dB) for band reject filter with $[d_2 d_1 d_0 = 1 0 0]$ control word selected

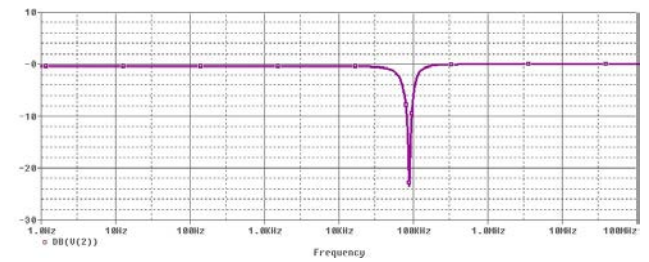


Figure 10(e). Simulated magnitude response (in dB) for band reject filter with $[d_2 d_1 d_0 = 1 0 1]$ control word selected

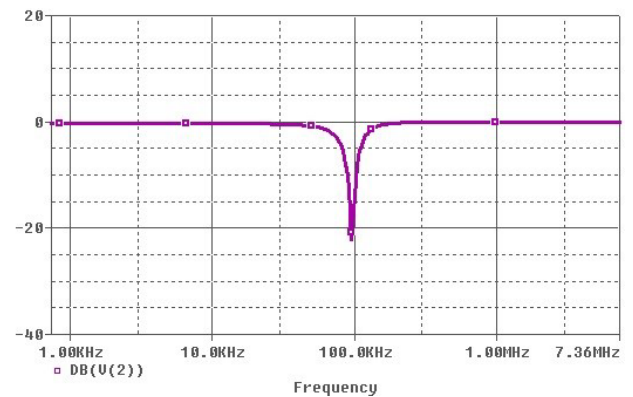


Figure 10(f). Simulated magnitude response (in dB) for band reject filter with $[d_2 d_1 d_0 = 1 1 0]$ control word selected

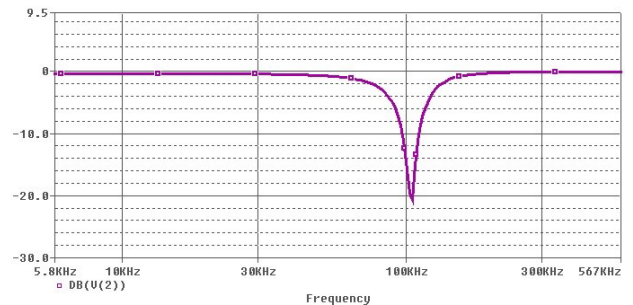


Figure 10(g). Simulated magnitude response (in dB) for band reject filter with $[d_2 d_1 d_0 = 1 1 1]$ control word selected

Table 3. Simulated values of the variation in cut-off frequency with the digital control word

Control word, k	Cut-off frequency of LPF (kHz)	Resonant frequency of BRF (kHz)	Resonant frequency of BPF (kHz)	Cut-off frequency of HPF (kHz)
1	46.61	38.90	40.17	34.19
2	67.08	54.70	56.66	47.55
3	81.51	67.89	68.81	58.68
4	93.34	79.99	79.90	68.35
5	103.60	87.60	88.73	76.97
6	112.75	96.32	98.50	84.85
7	121.18	104.72	104.59	92.13

Further variation in the quality factor (Q) along with the control word (k) was also taken into consideration. Table 4 shows the recorded values by simulation of the quality factor with the control word from [0 0 1] to [1 1 1]. Figure 12 shows the variation of the quality factor (Q) with the control word (k).

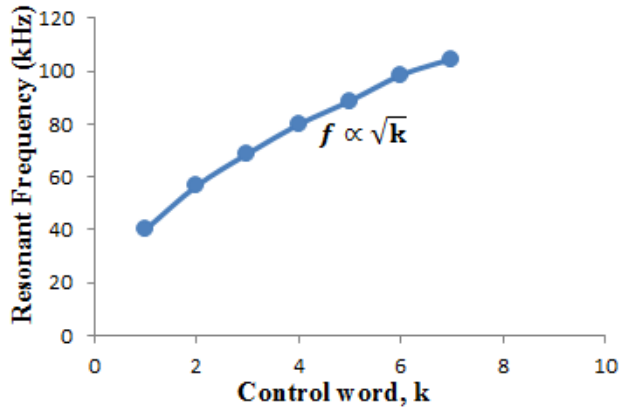


Figure 11(a). Variation of Resonant Frequency of BPF with digital control word

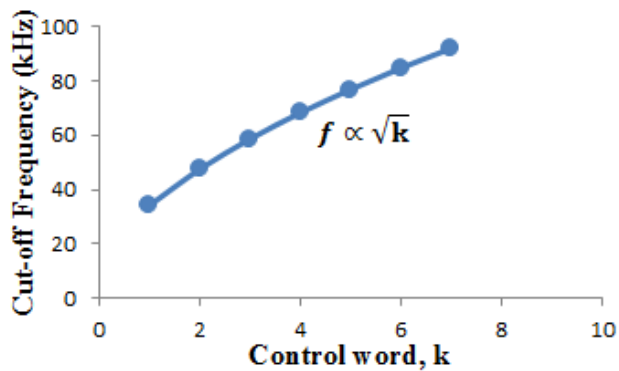


Figure 11(b). Variation of Cut-off of HPF with digital control word

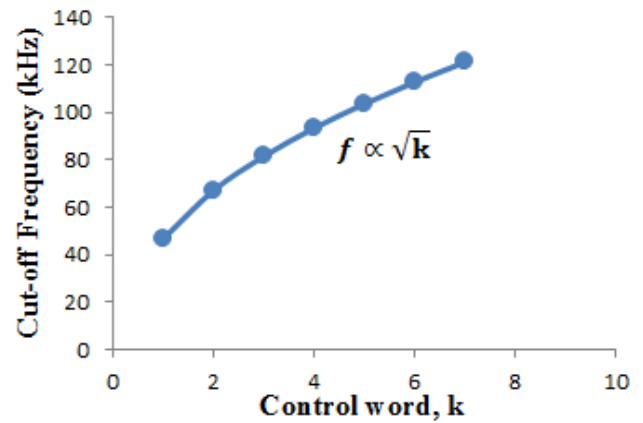


Figure 11(c). Variation of Cut-off Frequency of LPF with digital control word

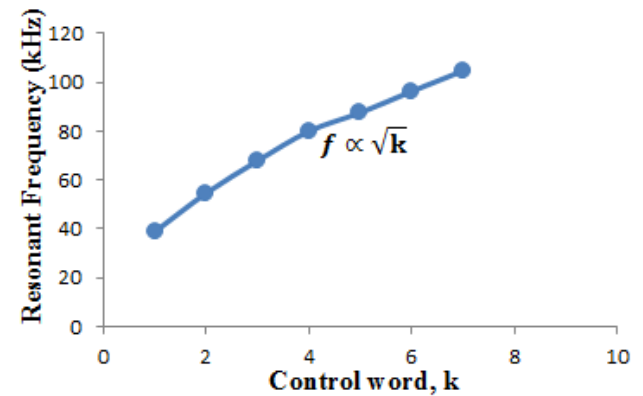


Figure 11(d). Variation of Resonant Frequency of Band Reject filter with digital control word

Table 4. Simulated values of the variation in quality factor with the control word

Control word k	Resonant frequency of BPF ω_0 (kHz)	3dB bandwidth of BPF ω_0/Q (kHz)	Quality Factor of BPFQ
1	40.17	39.90	1.007
2	56.66	40.41	1.402
3	68.81	40.90	1.682
4	79.90	41.42	1.929
5	88.73	41.90	2.118
6	98.50	42.42	2.322
7	104.59	43.01	2.432

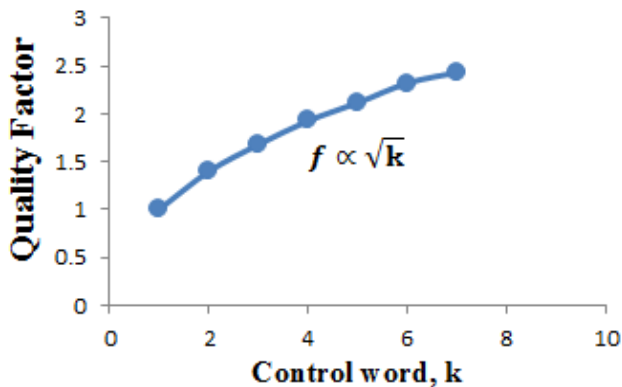


Figure 12. Variation of Quality factor (Q) of Band-pass filter with digital control word (k)

7. Conclusion

In this paper, a dual DVCC based digitally reconfigurable voltage-mode multifunctional biquadratic analog filter was presented. Digital control has been achieved by the variation of 3-bit digital control word using a Current Summing Network (CSN). Standard low-pass, high-pass, band-pass and band reject filter responses were obtained on providing voltages on different input terminals. Variation in the cut-off frequency with the digital control word was obtained for all four filter responses. Further digital control of the quality factor (Q) with the control word (k) was also obtained. PSPICE simulations were carried out to verify the working of the digitally controlled multifunctional biquadratic filter. Square root variation was observed and verified for both

the cut-off frequency (ω_o) and the quality factor (Q) with the control word (k). Both theoretical analysis and practical simulation work has been done which were found to be in full agreement with each other. This further confirms the above obtained results. Thus on the whole we got a multifunctional biquadratic analog filter which provides us with the low-pass, high-pass, band-pass and band-reject filter responses of varying cut-off frequency and a varying quality factor of a band-pass filter without changing any of the circuit components or the topology on the whole.

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