A 0.5V 3.6ppm/°C 2.2pW 2-Transistor Voltage Reference

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***Abstract*- A voltage reference using a depletion-mode device is designed in a 0.13µm CMOS process and achieves ultra-low power consumption and sub-1V operation without sacrificing temperature and supply voltage insensitivity. Measurements show a temperature coefficient of 3.6ppm/°C, line sensitivity of 0.033%/V, power supply rejection ratio of -67dB, and power consumption of 2.2pW. It requires only two devices and functions down to V_{dd}=0.5V with an area of 1350µm^2. A variant for higher V_{out} is also demonstrated.**

I. INTRODUCTION

Voltage references are vital to many digital and analog blocks including voltage regulators and A/D converters. They are also essential to bias analog circuitry. Temperature and supply voltage insensitivity along with power and area are key metrics for voltage references. There have been several approaches to designing voltage references in CMOS technology [1-5].

Recently sub-1V operation for voltage references has gained attention since technology forecasts project supply voltages well below 1V for highly-scaled low-power CMOS systems [6,7]. Also, energy efficient operation of digital systems has been demonstrated to occur at supply voltages in the 0.3-0.5V range [8,9]. Therefore it is desirable to have voltage references operating at sub-1V to avoid multiple supply voltages and/or other overhead.

Low power voltage references are also in great demand today given that recent advances in process, circuit, and architectural techniques have led to nW and pW systems for sensors and RFID [8,9]. Although a sub-100nW voltage reference was recently published [3], this would still dominate the total power consumption for such systems.

This work proposes a voltage reference, referred to as the 2T voltage reference, by exploiting subthreshold leakage current and a depletion-mode or ZVT (Zero-V_{TH}) MOSFET targeting low power and low voltage operation. Prototype chips show excellent TC (Temperature Coefficient), LS (line sensitivity), power consumption, and area. The 2T voltage reference functions at V_{dd} as low as 0.5V, at which point it consumes 2.22pW. The small power consumption and low supply floor enables it to be used in ultra-low power systems without substantial overhead. It is also suitable for high performance systems where its power consumption and silicon area are essentially negligible.

II. CIRCUIT DESIGN

Conventional voltage references, including well-known bandgap references, resort to amplifiers for error correction [1,2,5]. Although the amplifier provides good PSRR, line sensitivity and other error correction, the associated power and area overhead is significant. Recent designs use supply voltage independent current sources [3,4], however the current sources often rely on MOSFETs in saturation mode, which increases power consumption. In addition, the saturated MOSFETs require headroom, limiting supply voltage scalability. In this paper, we eliminate amplifiers and saturated devices while maintaining excellent voltage insensitivity, which enables improvements in supply voltage scalability, power consumption, and area.

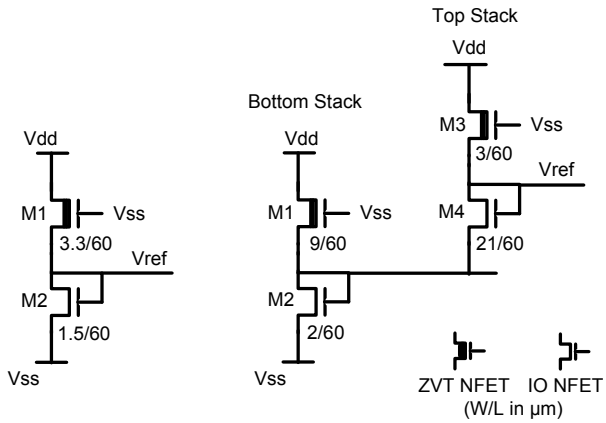

Fig. 1. Schematics of 2T and 4T voltage references.

The 2T voltage reference is shown on the left of Figure 1. Two different device types are used: a ZVT device for M1 and an I/O device for M2. The ZVT device is identical to a normal MOSFET with a near-zero V_{TH}. Both devices have thick gate oxides to support high V_{dd}. Depletion mode devices are widely available in modern foundry technologies. Although we have used a ZVT device for M1, any combination of two devices with a considerable V_{TH} difference can be used for the 2T voltage reference. The required V_{TH} difference will be discussed below.

The output voltage V_{ref} can be modeled by Equation 1, the well-known subthreshold current equation. Setting the current through M1 and M2 equal, EQ2 will hold given that 1) both devices are in weak inversion, 2) V_{ds} for M1 and M2 is greater than 3~4V_T (thermal voltage), and 3) M1 follows the subthreshold current equation at V_{gs} down to -V_{ref}.

From Equation 2, we obtain an analytical solution for V_{ref} in Equation 3, where both the first term and the second term are either proportional or complementary to absolute temperature. (Note that $V_{TH}=K_0+K_1 \bullet T$). By selecting the width

and length of the two devices appropriately, the temperature dependence of the two terms can be made to cancel out and excellent temperature insensitivity is obtained. The lack of a V_{dd} term in EQ3 leads to excellent line sensitivity and PSRR (Power Supply Rejection Ratio) with two transistors in subthreshold mode. M1 decouples the output from the supply voltage, acting as a subthreshold cascode.

$$I_{sub} = \mu C_{ox} \frac{W}{L}(m-1)V_T^2 \exp(\frac{V_{gs}-V_{TH}}{mV_T})(1-\exp(\frac{-V_{ds}}{V_T})) \quad \text{[EQ1]}$$

$$I = \mu_1 C_{ox1} \frac{W_1}{L_1}(m_1-1)V_T^2 \exp(\frac{0-V_{ref}-V_{TH1}}{m_1 V_T}) = \mu_2 C_{ox2} \frac{W_2}{L_2}(m_2-1)V_T^2 \exp(\frac{V_{ref}-V_{TH2}}{m_2 V_T}) \quad \text{[EQ2]}$$

$$V_{ref} = \frac{m_1 m_2}{m_1+m_2}(V_{TH2}-V_{TH1}) + \frac{m_1 m_2}{m_1+m_2} V_T \ln(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}) \quad \text{[EQ3]}$$

Sizing M1 and M2 in the 2T voltage reference aims to minimize both power consumption and temperature sensitivity. The longest gate length (L_1=L_2=60µm) allowed by the process design rules is used for both devices for ultra-low power consumption, although shorter gate length can be used to reduce footprint if energy budget for voltage references is relaxed. The widths (W_1=3.3µm, W_2=1.5µm) are chosen to minimize temperature sensitivity. In selecting widths, the different characteristics (µ and m) of two devices must be considered. As shown in Figure 2 and Equation 3, the optimum W_1 and W_2 balances out the temperature-dependent parts from the two terms in Equation 3, resulting in little temperature coefficient.

Since coupling through the parasitic MOSFET capacitance can affect PSRR, an output capacitor is added for signal robustness. Simulated behavior in Figure 3 shows that larger output capacitance improves PSRR as expected.

The minimum supply voltage is limited by whether V_{ds} of M2 is larger than 3-4V_T. If not, Equation 2 does not hold since the final V_{ds} term in Equation 1 cannot be neglected. On the other hand, the maximum supply voltage is set by reliability issues such as oxide breakdown. If necessary, diode connected transistors can be added between V_{dd} and M1 to increase the maximum V_{dd}.

Equation 3 implies a design constraint on the required difference of V_{TH} between the two devices (M1 and M2). Assuming typical subthreshold swing (90mV/dec) for the two devices (i.e., m1=m2=1.5), the minimum V_{TH} difference is approximately 1.33V_{ref} from Equation 3 if we can neglect the second log term to the first order. Note that V_{ref} is equivalent to V_{ds} of M1, which should be larger than 3~4V_T as shown above (i.e. to neglect the final V_{ds} term in Equation 1). Hence, the minimum V_{TH} difference is approximately 4-5.3V_T for this type of voltage reference.

III. 2T REFERENCE MEASURED RESULTS

Figure 4 shows measured results from a test chip fabricated in a standard 0.13µm CMOS technology with no process options. With a 0.4pF finger-shaped metal-to-metal output capacitor, the 2T voltage reference exhibits a TC of <4ppm/°C across a range of V_{dd}. The reference achieves an excellent line sensitivity of 0.033%/V and a PSRR of -67dB at 100 kHz. Higher frequency measurements are limited by the test setup at this time. The entire design requires only 1350µm^2 since there is no operational amplifier. Extremely low power of 2.22pW is realized at V_{dd}=0.5V and 20°C and 27.16pW at V_{dd}=3.3V and 20°C

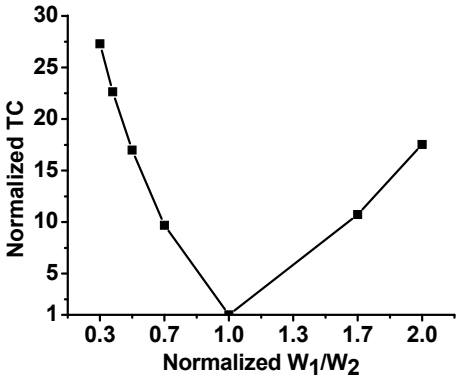

Fig. 2. Proper sizing of two transistors minimizes temperature dependency (simulated results).

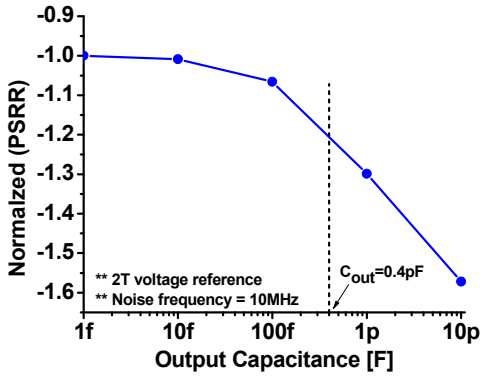

Fig. 3. A larger output capacitor provides better PSRR (simulated results).

To evaluate the tolerance of the 2T voltage reference to process variation, 47 dies from a single run are measured as shown in Figure 6. Although operation occurs in the sub-V_{TH} regime, process variation impact is small due to 1) the linear effect of V_{TH} on output voltage and 2) large device dimensions, suppressing both V_{TH} variation due to random dopant fluctuations and geometric variations. The standard deviation of the output voltage for the 2T voltage reference is 1.3mV without post-silicon trimming. Since all 47 dies are from a single wafer, it is hard to evaluate the tolerance to wafer-to-wafer variation yet. Corner case simulation shows +/- 2% maximum output voltage change due to global V_{TH} variation of the two different devices, which could be addressed using post-silicon trimming.

Table I compares the 2T voltage reference to recently published work in bulk CMOS [2-4] and SOI processes [5]. The TC and line sensitivity compare favorably with previous

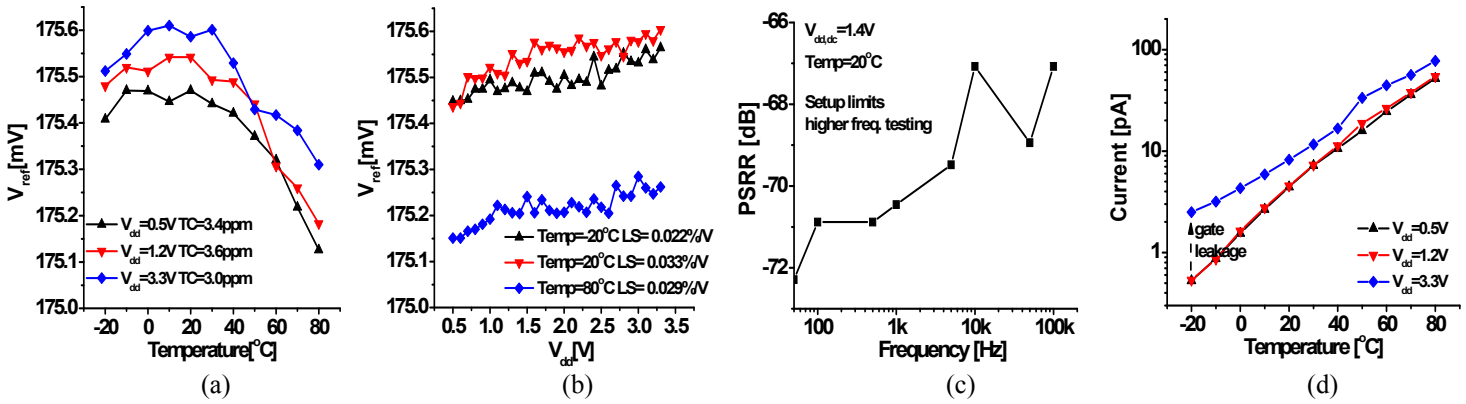

Fig. 4. Measured results for the 2T voltage reference: (a) temperature coefficient, (b) line sensitivity, (c) power supply rejection ratio, (d) current consumption.

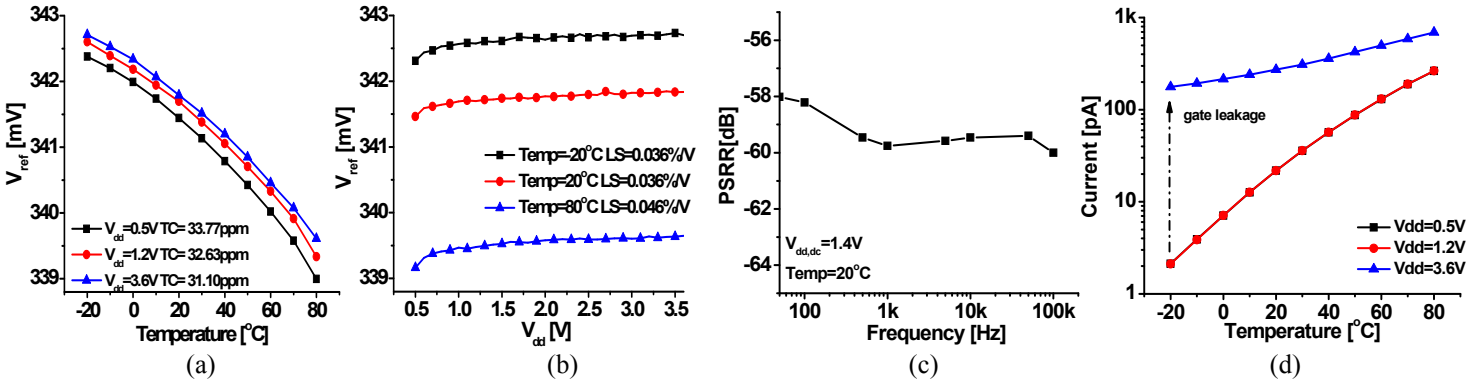

Fig. 5. Measured results for the 4T voltage reference: (a) temperature coefficient, (b) line sensitivity, (c) power supply rejection ratio, (d) current consumption.

work while silicon footprint is reduced significantly since it uses only two devices. In addition, power consumption is reduced by about three orders of magnitude, realizing a pW voltage reference for the first time. Also the 2T voltage reference is operational down to 0.5V. The small power consumption makes it feasible to use the 2T voltage reference for ultra-low power systems without dominating the total power budget.

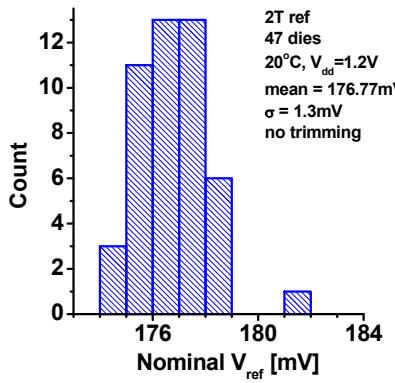

Fig. 6. Measured output distribution of the 2T reference.

IV. 4T VOLTAGE REFERENCE

We also demonstrate a 4T voltage reference to produce a higher V_{ref} by stacking two 2T voltage references, as shown in the right of Figure 1. Since the ground for the top stack is the output of the bottom stack, TC and PSRR are expected to degrade somewhat compared to the 2T reference.

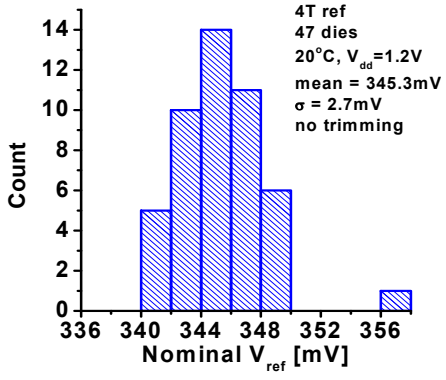

Fig. 7. Measured output distribution of the 4T reference

Table. I Comparison table (size in ( ) represents the area normalized to a 0.35µm technology).

	2T	4T	[2]	[3]	[4]	[5]
Process	0.13µm CMOS	0.13µm CMOS	0.35µm CMOS	0.35µm CMOS	0.6µm CMOS	CMOS/SIMOX
$V_{dd,min}$	0.5V	0.5V	1V	0.9V	1.4V	0.6V
V_{out}	175.5mV	341.5mV	190.1mV	670mV	309.3mV	530mV
TC	3.6ppm/°C	33.8ppm/°C	16.9ppm/°C	10ppm/°C	2.7ppm/°C	20ppm/ °C
LS	0.033%/V	0.036%/V	0.76%/V	0.27%/V	0.012%/V	N/A
PSRR	-70/-67dB (100/100kHz)	-58/-59dB (100/100kHz)	-41/-28/-17dB (100/100k/100MHz)	-47dB/-38/-41dB (100/100k/100MHz)	-47dB/-20dB (100Hz/10MHz)	N/A
Power	4.43pA×0.5V 8.23pA×3.3V	21.7pA×0.5V 272pA×3.6V	250nA×1V	40nA×0.9V	9.7µA×3V	0.1mA×1V
Size	1350(9785)µm^2	3500(25369)µm^2	49000µm^2	45000µm^2	55000(18715)µm^2	60000 µm^2

In Figure 5, measurements for the 4T voltage reference with a 0.4pF metal-to-metal output capacitor show a TC of 33.8ppm/°C, line sensitivity of 0.036%/V, PSRR of -59dB at 100kHz, and power consumption of 10.85pW at V_{dd}=0.5V. The design requires 3500µm^2 including the output capacitor. Figure 7 shows its output distribution over 47 dies. Without any post-silicon trimming, 2.7mV of standard deviation is measured. Measurement results are also summarized in Table I.

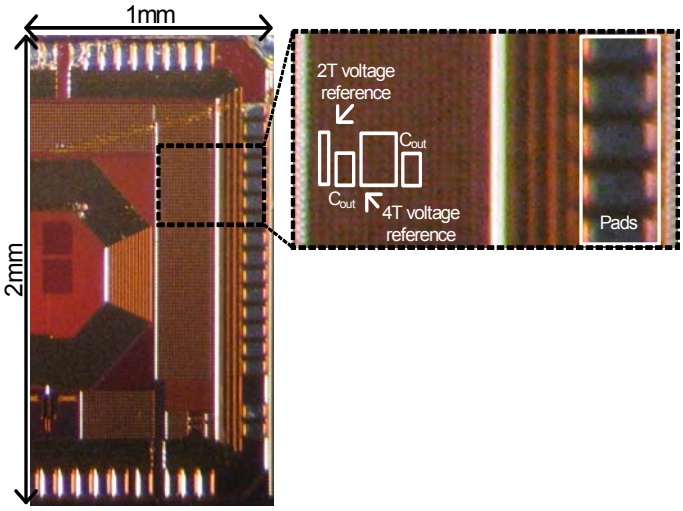

Fig. 8. Die photo of 2T and 4T voltage references.

The die photo is shown in Figure 8, showing the small footprint of the two different types of the proposed voltage references. Detailed information on dimension is listed in Table II.

Table II. Dimension information for the 2T and 4T voltage references and corresponding output capacitors

Module	Footprint
2T (0.4pF C_{out})	8.8µm × 62µm 20µm × 40µm
4T (0.4pF C_{out})	43µm × 62 µm 20µm × 40 µm

V. CONCLUSION

In summary, we propose 2T and 4T voltage references. Prototype circuits are fabricated in a commercial 0.13µm CMOS process. The 2T voltage reference, functional down to V_{dd} of 0.5V, achieves pW power consumption and small footprint with excellent TC, line sensitivity, and PSRR. Due to its small power and area, it can be incorporated into ultra-low power systems with low overhead.

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