

Modeling of a Second Order Sigma-Delta Modulator with Imperfections

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Abstract—Sigma delta modulators ($\Sigma\Delta$ Ms) form part of the core of today's mixed-signal designs. The ongoing research on these devices shows the potential of $\Sigma\Delta$ data converters as a promising candidate for high-speed, high-resolution, and low-power mixed-signal interfaces.

This work presents a new accurate behavioral model of a second order low-pass Switched Capacitor (SC) Sigma-Delta modulator. Our main contribution consists to predict the effect of almost sources of noise on the operation of sigma delta modulator such as non idealities of op-amp and switches.

The purpose of this work is the presentation of a behavioral model of a second order switched capacitor $\Sigma\Delta$ modulator considering (Error due to Clock Jitter, Thermal noise Amplifier Noise, Amplifier Slew-Rate, Non linearity of amplifiers, Gain error, Charge Injection, Clock Feed-through, and Nonlinear on-resistance). A comparison between the use of MOS switches and the use transmission gate switches use is analyzed.

Keywords—Charge injection; clock feed-through; Sigma Delta modulators; Sigma Delta non-idealities; switched capacitor.

I. INTRODUCTION

Sigma delta modulators are the most suitable Analog-to-Digital converter (ADC) topologies for digitizing with high-resolution analog signals characterized by a bandwidth (BW) much smaller than the sampling frequency f_s . With these architectures, a resolution up to 19–21 bits can be reached using standard Integrated Circuit (IC) technologies. Designers use sampling rates much higher than the Nyquist rate, typically higher by a factor between 8 and 512, and utilizing all preceding input values [1][2][3], they generate each output. The most popular approach is based on a sampled-data solution with switch capacitor implementation. For this reason these features make the solutions very attractive for a number of applications. For instance, they have gained increasing popularity in audio applications, in receivers for communication systems, in sensor interface circuits, and in measurement systems.

Because of the diversity of architectures implementing converter, it cannot exist a generic model for all ADCs. Each architecture implementation of converter requires its own model.

In this paper we will try analyze the performances of a second order sigma-delta modulator including non-idealities compared to its ideal model. To do this, we must define the parameters to estimate this feature which can characterize an ADC. Therefore, we present a complete set of SIMULINK [3] models, which allow us to perform exhaustive behavioral simulations of any Sigma-Delta modulator, taking into account most of the non-idealities, such as sampling jitter, kT/C noise, and operational amplifier parameters (noise, finite gain, finite bandwidth, slew-rate and saturation voltages).

In the first part we will focus on the parameters (errors) that can affect the performances of the Sigma-Delta modulator. In the second part, we will present a non-ideal Sigma-Delta modulator model and we will illustrate the different effects providing by each circuit imperfection, and the difference between the use of the NMOS switch and the transmission gate switch.

II. CLOCK JITTER

Ideally the sampling operation assumes a perfect clock, with its period is well defined and stable over time. The term clock jitter refers to the uncertainty of the time characteristics of the clock source. The clock oscillator affected by intrinsic noise will introduces some uncertainty t_j (jitter) on the exact moment of sampling.

Jitter is mainly caused by thermal noise, phase noise, and spurious components in every clock-generation circuitry. In a SC circuit, jitter is generally defined as short-term, non-cumulative variation of the significant instant of a digital signal from its ideal position in time [7]. Sampling clock jitter results in non-uniform sampling and increases the total error power in the quantizer output.

The magnitude of this error is a function of both the statistical properties of the jitter and the modulator input signal.

This effect can be simulated with SIMULINK[®] by using the model shown in Figure 2, which implements Eqn. (1). Here, we assumed that the sampling uncertainty δ is a Gaussian random process Figure 1 with standard deviation $\Delta\tau$ [14][8].

$$x(t + \delta) - x(t) \approx 2\pi f_{in} \delta A \cos(2\pi f_{in} t) = \delta \frac{d}{dt} x(t) \quad (1)$$

Where A is the input signal amplitude, f_{in} is the input signal frequency and δ is the sampling uncertainty.

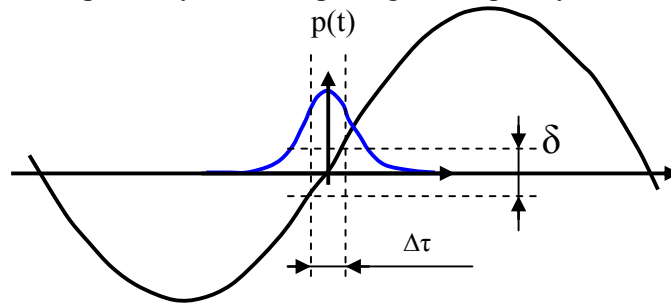


Figure 1. Effect of clock jitter in the sampling.

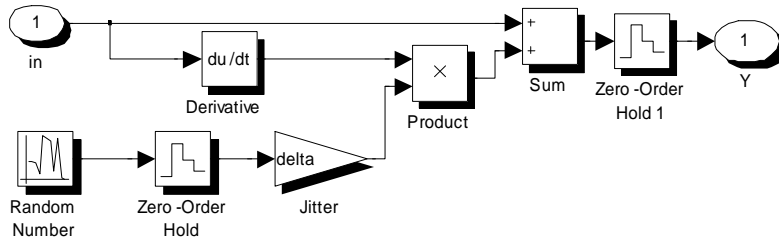


Figure 2. SIMULINK[®] Model of a random sampling jitter.

III. NOISE ON INTEGRATOR

The integrator is the fundamental block of a $\Sigma\Delta M$, and therefore its non idealities largely affect the $\Sigma\Delta M$ performance. The two important sources of noise in a switched-capacitor circuit are the on resistance of the switches and the non ideality of the amplifier [8]. To determine the density of noise introduced by the integrator, we must choose a topology of the integrator. The switched capacitor integrator is shown in Figure 3 with feedback.

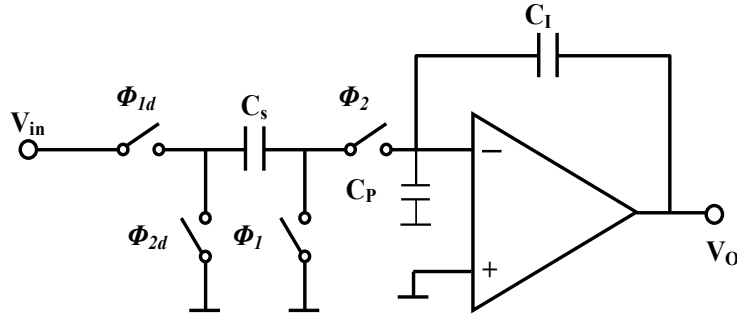


Figure 3. Simple integration with feedback.

A. Thermal noise

According to Nyquist theorem the spectral density of noise at the terminals of a dipole passive depends only on the temperature and the real part of impedance of the dipole. In a switched capacitor integrator, switches operate in ohmic region; the noise power at their terminals is equal to:

$$E_{sff}^2 = \gamma(f) \Delta f = 4KTR\Delta f \quad (2)$$

The noise due to switch on phases I and P is given by the eqns. (3) and (4):

Phase I

$$V_{thP}^2 = \frac{KT}{C_s} + \left(\frac{C_r}{C_s} \right)^2 \frac{KT}{C_r} \quad (3)$$

Phase P

$$V_{thI}^2 = \frac{KT}{C_s} + \frac{KT}{C_r} \quad (4)$$

K is the Boltzman constant ($K=1.38 \times 10^{-23} \text{ J/K}$) and T the absolute temperature in Kelvin.

Eqns. (3) and (4) show that if we wish reduce the thermal noise power, then we must increase the value of the sampling capacity C_s .

B. Amplifier Noise

The sources of noise present in an amplifier are generally due to two reasons: the thermal noise and the noise in $1/f$. For a MOS transistor in saturation, the noise produced by the tow sources is equivalent to the voltage generator given by:

$$S_{En} \approx 2 \frac{2}{3} KT \frac{1}{g_m} + \frac{k_f}{C_{ox}WL} \frac{1}{f} \quad (5)$$

The first term of this eqn. (5) represents the thermal noise of a MOS transistor and the second represents the noise equivalent to in $1/f$.

IV. INTEGRATOR IMPERFECTIONS

A. Gain error

The DC gain of the ideal integrator is infinite. In practice, the gain of the operational amplifier open loop A_0 is finite. This is reflected by the fact that a fraction of the previous sample out of the integrator is added to the sample input [4].

The model of a real integrator with an integrator delay is real considering the saturation op-amp, the gain over the finite bandwidth and slew-rate. The z transfer function of a perfect integrator is given by:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (6)$$

The transfer function of the real integrator becomes:

$$H(z) = \beta \frac{z^{-1}}{1 - \alpha z^{-1}} \quad (7)$$

where α and β are the integrator's gain and leakage, respectively [6].

$$\alpha = \frac{A_0 - 1}{A_0} \quad (8)$$

B. Distortion and settling time of the integrator

The distortion limits is the power effectively used by the system and its bandwidth. There are various reasons why a signal is distorted. Harmonic distortion is mainly due to two factors: the gain nonlinearity and the slew-rate of the amplifier.

- *Non linearity of amplifier*

Theoretically its ideal transfer function is:

$$V_s = AV_e \quad (9)$$

A is the amplification factor. However, HSpice gives us the curve in Figure 4, with its transfer function is approximated by (10) [5].

$$A \cong A_0 \left(1 + \alpha_1 |V_o| + \alpha_2 |V_o|^2 + \alpha_3 |V_o|^3 + \dots \right) \quad (10)$$

$(\alpha_1, \alpha_2, \alpha_3 \dots)$ are the amplification factors parasites, for a pure sinusoidal signal of frequency f in the input of the amplifier, we find that output of the amplifier is only not the input signal amplified with frequency of V_e but there is another parasitic signals with higher frequency and proportional to the frequency f_r , this because the fully differential configurations is nearly an even function and will hence produce the odd harmonic in the output.

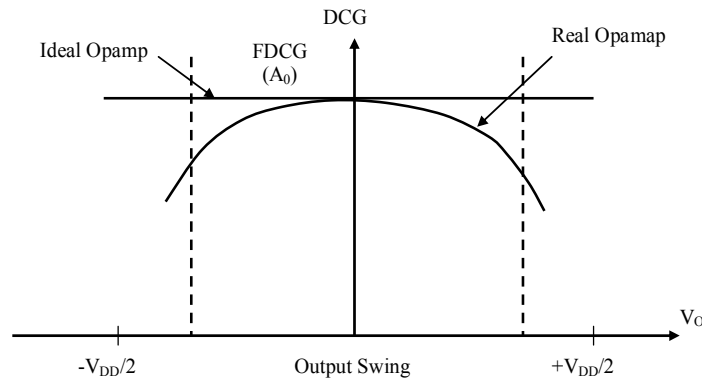


Figure 4. DC gain of an amplifier as a function of output voltage [9].

- *Amplifier slew-rate*

For a given constant amplitude, slew-rate characterizes the limit of the amplifier frequency (maximal speed).

When a signal is changing more slowly than the maximal speed, the amplifier follows and reproduces faithfully the signal. But when the signal frequency increases (for constant amplitude), the amplifier distorts the output signal. In this case, in addition to the original signal, there are additional frequencies (harmonics). The augmentation of the input signal frequency causes difficulties to the amplifier to restore

the signal faithfully.

In order to get a linearly response from the amplifier, we define generally a maximum frequency above which the amplifier distorts the output signal. For a sinusoidal signal of amplitude A and pulsation ω , this frequency is defined as:

$$GBW = 2\pi Af \leq SR \Rightarrow f = \frac{SR}{2\pi A} \quad (11)$$

For a converter it is:

$$f = \frac{1}{2\pi A 2^n \tau} \quad (12)$$

T is the settling time, $\tau = 1/2\pi GBW$ and n the resolution of the converter.

In the case of a SC integrator (the main constituent of a $\Sigma\Delta$ modulator) the maximum speed causes an error (settling error) on the output voltage of the integrator.

Indeed, the finite bandwidth and slew-rate of the amplifier are related and may occur in the switched-capacitor circuit. the non-ideal transient response (non-linear: called especial mode of operation "slew-rate" producing for each clock edge an incomplete charge transfer at the end of the integration period. The effect of the finite bandwidth and the slew-rate are related to each other and may be interpreted as a non-linear gain [16].

V. SWITCH NON-IDEALITIES

Switches are one of the major elements in SC circuits. The ideal role of them is to have zero or infinite resistance when they are ON or OFF. However, as switches in CMOS technology are realized by using nMOS and pMOS transistor, they manifest some non-idealities such as nonlinear on-resistance, clock-feed-through, and charge injection [12].

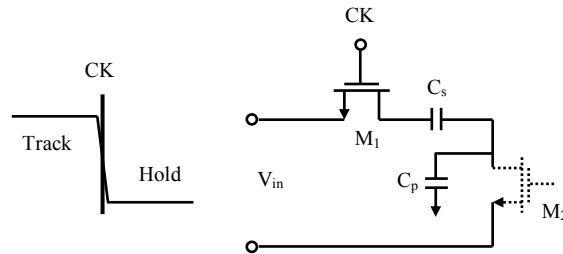


Figure 5. Simplest sample-and-hold circuit in MOS technology.

A. Charge Injection

When a MOS switch is on, it operates in the triode region and its drain-to-source voltage, V_{DS} , is approximately zero. During the time when the transistor is on, it holds mobile charges in its channel. Once the transistor is turned off, these mobile charges must flow out from the channel region and into the drain and the source junctions as depicted in Figure 6 [10][11].

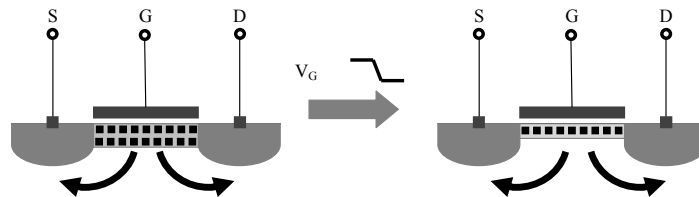


Figure 6. Channel charge when MOS transistor is in triode region.

For the sample and hold (S/H) circuit in Figure 6, if the MOS switch M_1 is implemented using an nMOS

transistor, the amount of channel charge Q_{ch} , is given by Eqn. (13) this transistor can hold charges while it is on.

$$Q_{ch} = -WLC_{ox}(V_{DD} - V_{tn} - V_{in}) \quad (13)$$

where W and L are the channel width and channel length of the MOS transistor respectively, C_{ox} is the gate oxide capacitance, and V_{th} is the threshold voltage of the nMOS transistor.

When the MOS switch is turned off, some portion of the channel charge is released to the hold capacitor C_s , while the rest of the charge is transferred back to the input V_{in} . The fraction k of the channel charge that is injected into C_s is given by Eqn. (14):

$$\Delta Q_{ch} = kQ_{ch} = -kWLC_{ox}(V_{DD} - V_{tn} - V_{in}) \quad (14)$$

As a result, the voltage change at V_{out} due to this charge injection is given by Eqn. (15):

$$\Delta V_{out} = \frac{\Delta Q_{ch}}{C_s} = \frac{-kWLC_{ox}(V_{DD} - V_{tn} - V_{in})}{C_s} \quad (15)$$

Notice that ΔV_{out} is linearly related to V_{in} and V_{th} . However, V_{th} is nonlinearly related to V_{in} [10][15]. Therefore, charge injection introduces nonlinear signal-dependent error into the S/H circuit.

B. Clock Feed-through

Clock feed-through is due to the gate-to-source overlap capacitance of the MOS switch. For the S/H circuit of Figure 5, the voltage change at V_{out} due to the clock feed-through is given by Eqn. (16) [10]:

$$\Delta V_{out} = \frac{-C_p(V_{DD} - V_{SS})}{C_p + C_p} \quad (16)$$

where C_p is the parasitic capacitance.

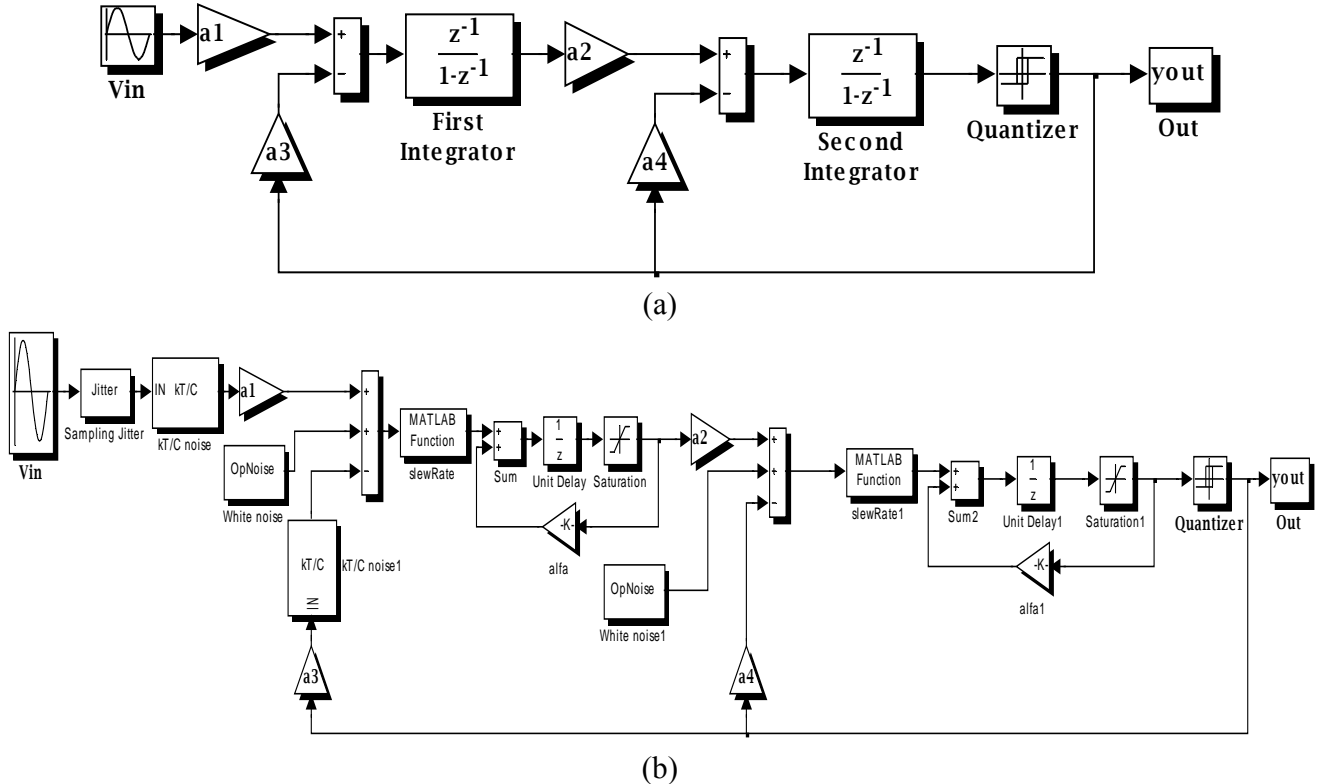


Figure 7. (a) Ideal second-order single-loop single-bit $\Sigma\Delta$ modulator. (b) Its non-ideal model.

The error introduced by clock feed-through is usually very small compared with charge injection. Also, notice that clock feed-through is signal-independent which means it can be treated as signal offsets that can

be removed by most systems. Thus, clock feed-through error is typically less important than charge injection.

Charge injection and clock feed-through are due to the intrinsic limitations of MOS transistor switches. These two errors limit the maximum usable resolution of any particular S/H circuit, and in turn, limit the performance of the whole system [10][15].

C. Nonlinear ON-resistance

Is a signal-dependent variation of the on-resistance of the switch introduces harmonic distortion into the circuit. There are many ways to degrade this nonlinearity, such as decreasing the S/H time constant, using transmission gates, clock-boosting and bootstrapping (in low-voltage applications), etc. [12][13].

VI. SIMULATION RESULTS

In order to validate the behavioral model of our modulator, we compare the effects of non-idealities with the ideal modulator Figure 7 (a). The fundamental blocks for the behavioral simulation of SC $\Sigma\Delta$ are: SC integrator, noise sources (such as sampling jitter, and thermal noise), and the basic circuits non-idealities (such as finite DC Gain, Slew-Rate, Charge Injection ...etc). The second-order low-pass modulator shown in Figure 7 (b) with the parameters listed in TABLE I was used. Where Figure 7. (a) shows a model of an ideal modulator and Figure 7. (b) a real one.

TABLE I
NOISE DUE TO THE SWITCH

Parameter	Value
Oversampling Ratio (OSR)	256
Clock Frequency (MHz)	12.28
Input Sinusoidal frequency (kHz)	7.3
Samples number	65536
a1, a3	0.2
a2	0.5
a4	0.25
a	1

It is important to note that when an analog signal is sampled, the variation of the sampling period was not a direct effect on circuit performance. Therefore, the clock jitter is only introduced by the sampling signal and thus the effect of this error on a $\Sigma\Delta$ converter is independent of the structure or the order of the modulator. We can see that, when the jitter error increases, the total noise power at the output of the quantizer increases. For the same value of uncertainty, frequency of input signal introduces a high power noise more important. Thus a compromise must be made between a high error and high frequency. Figure 8 shows the output PSD of the modulator for different values of clock jitter.

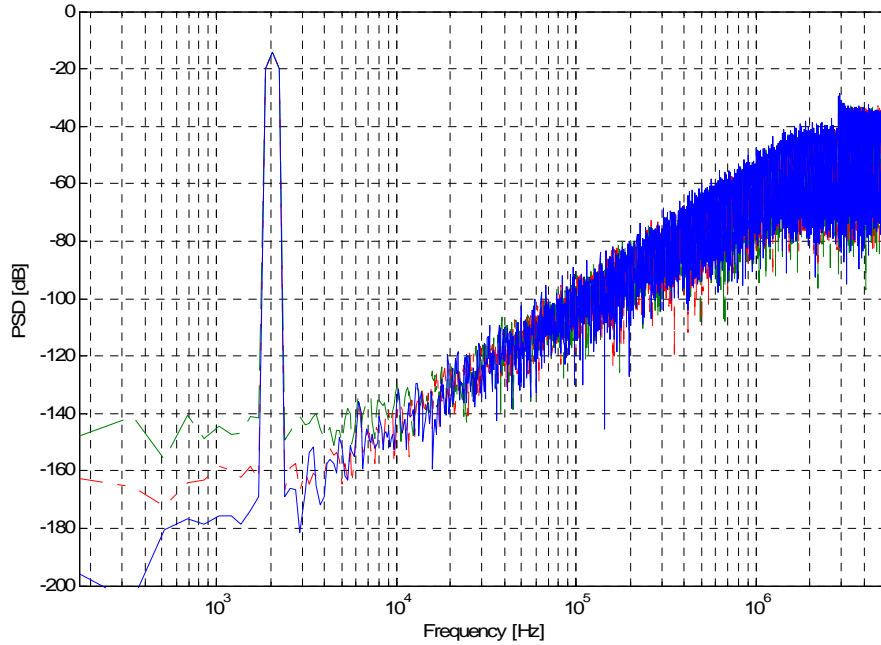


Figure 8. The PSDs of the modulator output with deferent Clock Jitter.

It is clearly seen that the non linear effect of clock jitter in (green and red curves) introduces non ideal behavior of the modulator.

To reduce the non-linearity introduced by the switch the bootstrapping technique is often used. In this case a dedicated circuit drives the gates of the MOS transistors with a voltage dependent on the input signal (e.g. $V_{DD}+V_{in}$ in the ideal case) in order to maintain the V_{GS} constant. Actually the gate voltage cannot be exactly $V_{DD}+V_{in}$, but is typically $V_{DD}+BSV_{in}$, with BS ranging from 0 (no bootstrapping) to 1 (ideal bootstrapping). In this case, the on-resistance of a complementary CMOS switch becomes [14]:

$$R_{QN} = G_{SN} + G_{SP} = K'_N \frac{W}{L} (V_{DD} - V_{thN} - V_{in} + BSV_{in}) + K'_P \frac{W}{L} (-V_{SS} + V_{thP} + V_{in} - BSV_{in}) \quad (17)$$

which is almost independent of the input signal.

where V_{in} is the input voltage, V_{thN} (positive) and V_{thP} (negative) are the threshold voltages of the nMOS and pMOS transistors, K'_N and K'_P are the gain factors of the nMOS and pMOS transistors and V_{DD} and V_{SS} are the positive and negative supply voltages used for driving the gates of the nMOS and pMOS transistors, respectively.

Figure 9 shows the PSD of a $\Sigma\Delta$ using nMOS switches, and the use of a transmission gate switches. Where Table III summarize the specifications of the modulator shown in Figure 7 with the parameters listed in Table II.

TABLE II Parameters of the $\Sigma\Delta$ shown in Figure 7 with specifications listed in TABLE I.

TABLE II
PARAMETERS OF THE $\Sigma\Delta$ SHOWN IN FIGURE 7 WITH PARAMETERS LISTED IN TABLE I.

Parameter	Value
Sampling Capacitor (pF)	5
Thermal Noise (μV_{rms})	10
Clock Jitter (ns)	1

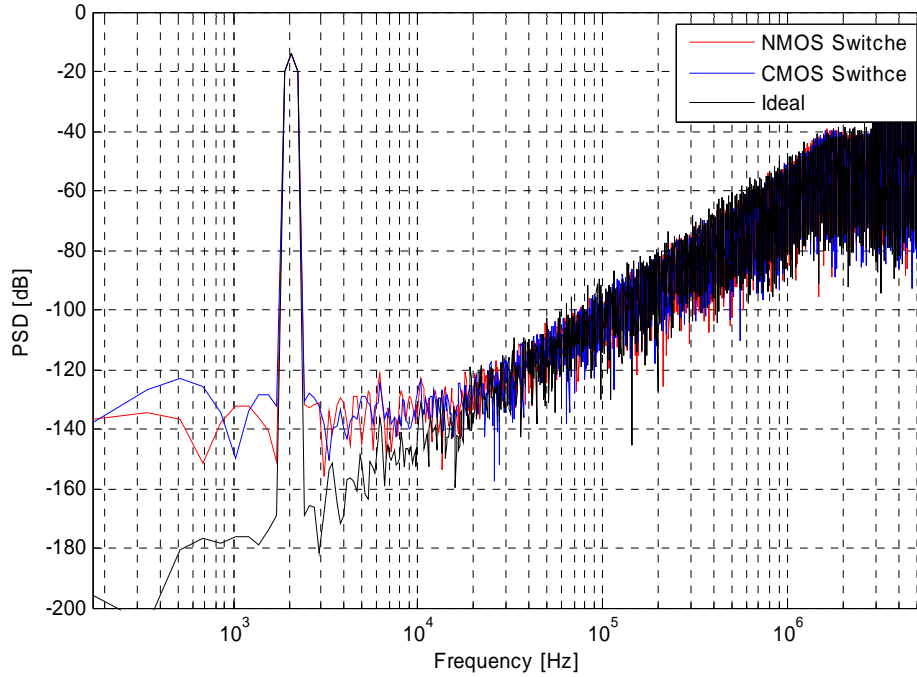


Figure 9. The PSDs of the modulator output with deferent values of bootstrap.

TABLE III shows the deference between the use of a NMOS switches and the use of a transmission gate switches.

TABLE III
SNR AND ENOB FOR THE USE OF NMOS SWITCH AND TRANSMISSION GATE SWITCH.

	NMOS switch	Transmission gate switch
SNR	96.06	96.37
ENOB	15.66	15.71

We can see that the use of transmission gate switches have not a considerable effect on the behavior of the sigma delta modulator, but they have an effect on the power dissipation and many other parameters.

VII. CONCLUSION

In this paper, a presentation of a behavioral model of a second order SC $\Sigma\Delta$ modulator including noise (switches' and op-amp's thermal noise), clock jitter, the finite DCG and UGBW of the integrators, slew-limiting, DCG nonlinearities switches' clock feed-through, and charge injection are presented. The SC $\Sigma\Delta$ modulator, has been analyzed, and modeled in SIMULINK. Evaluation and validation of the models were done via behavioral simulations for the two models (Ideal second-order single-loop single-bit $\Sigma\Delta$ modulator and its non-ideal model) using SIMULINK.

A comparison was made between the use of an NMOS switch and the use of a CMOS (transmission gate) switch.

REFERENCES

- [1] B. E. Boser and B. A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 22, no. 12, pp. 1298–1308, Dec. 1988.
- [2] Schreier R., Temes G. C, "Understanding Delta-Sigma Data Converters," New York : *IEEE Press*, 2005.

- [3] S. R. Northworthy, R. Schreier, and G. C. Temes, "Delta-Sigma Data Converters," *Piscataway, NJ: IEEE Press*, 1997.
- [4] G. Temes, "Finite amplifier gain and bandwidth effects in switched-capacitor filters," *IEEE J. Solid-State Circuits*, vol. 15, pp. 358–361, June 1980.
- [5] F. Medeiro et al., "Modeling opamp-induced harmonic distortion for switched-capacitor SD modulator design," in *IEEE Int. Symp. Circuits Systems*, vol. 5, May-Jun. 1994, pp. 445–448.
- [6] H. Zare-Hoseini and I. Kale, "On the effects of finite and nonlinear DC-gain on the switched-capacitor delta-sigma modulators," in *Proc. IEEE Int. Symp. Circuits Systems*, May 2005, pp. 2547–2550.
- [7] S. Lee and K. Yang, "Design a Low-Jitter Clock for High-Speed A/D Converters". *Sensors*, vol. 18, no. 10, October 2001.
- [8] S. Brigati, F. Francesconi, P. Malcovati, D. Tonietto, A. Baschiroto and F. Maloberti, "MODELING SIGMA-DELTA MODULATOR NON-IDEALITIES IN SIMULINK®," *IEEE International Symposium*, pp 384 - 387 vol.2, 1999.
- [9] F. MEDEIRO, "CAD Methodology for High-Resolution, High-Speed S-D Modulators with Emphasis in Cascade Multi-Bit Architectures", *ICM-Neue Messe*, Munich, 2001.
- [10] L. Dai, R. Harjani, "CMOS Switched-Op-Amp-Based Sample-and-Hold Circuit" *IEEE Journal of Solid-State Circuits*, vol. 35, no. 1, pp. 109-113, January 2000.
- [11] J. Shieh, M. Patil, and A. J. Sheu, "Measurement and analysis of charge injection in MOS analog switches," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 4, pp. 277–281, Apr. 1987.
- [12] J. Shieh, M. Patil, and A. J. Sheu, "Measurement and analysis of charge injection in MOS analog switches," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 4, pp. 277–281, Apr. 1987.
- [13] X. Weize and E. G. Friedman, "Clock-feedthrough in CMOS analog transmission gate switches," in *Annu. IEEE Int. ASIC/SOC Conf.*, Sep. 2002, pp. 181–185.
- [14] Category: Control Systems, File: SD Toolbox [Online]. Available: <http://www.mathworks.com/matlabcentral/fileexchange>
- [15] D.A. Johns, K. Martin, "Analog Integrated Circuit Design," *John Wiley & Sons, Inc.*, Toronto, 1997
- [16] F. Medeiro, B. Perez-Verdu, A. Rodriguez-Vazquez, J. L. Huertas, "Modeling OpAmp-Induced Harmonic Distortion for Switched-Capacitor $\Sigma\Delta$ Modulator Design", *Proceedings of ISCAS 94*, vol. 5, pp. 445-448, London, UK, 1994.



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