

First Time, Every Time – Practical Tips for Phase- Locked Loop Design

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Outline

- Introduction
- Basic Feedback Loop Theory
- Jitter and Phase Noise
- Common Circuit Implementations
- Circuit Verification
- Design for Test

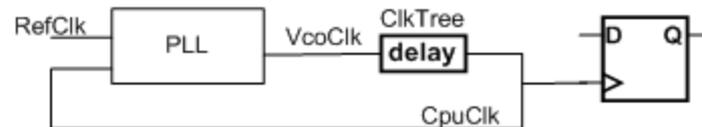
Introduction

How Are PLL's Used?

- Frequency Synthesis (e.g. generating a 1 GHz clock from a 100 MHz reference in a CPU)

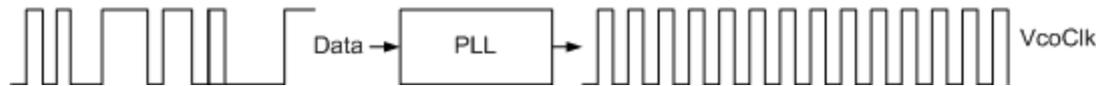


- Skew Cancellation (e.g. phase-aligning an internal clock to the I/O clock) (May use a DLL instead)

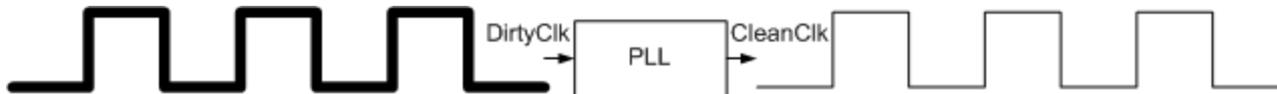


How Are PLL's Used?

- Extracting a clock from a random data stream (e.g. serial-link clock-data recovery)



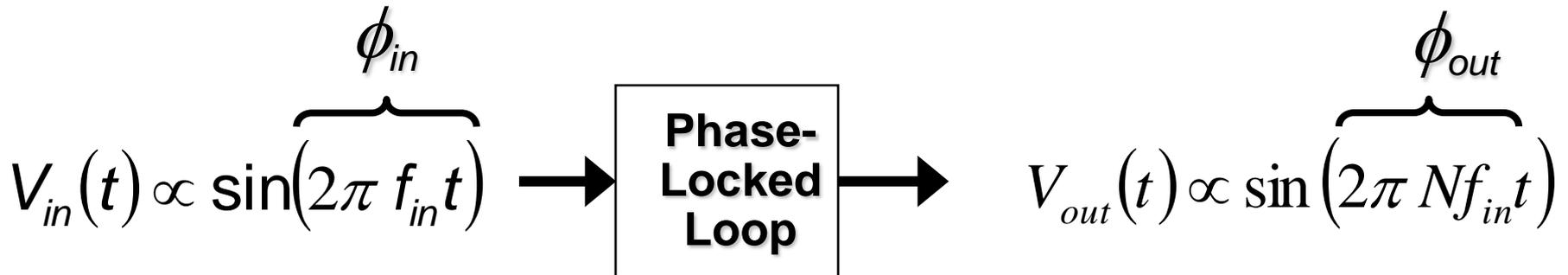
- Reference Clean-Up (e.g. low-pass filter source-synchronous clock in high-speed I/O)



- **Frequency Synthesis** is the focus of this course.
- Design Priority? Frequency and/or phase accuracy?

What is a PLL?

- Negative feedback control system where f_{out} tracks f_{in} and rising edges of input clock align to rising edges of output clock
- Mathematical model of frequency synthesizer

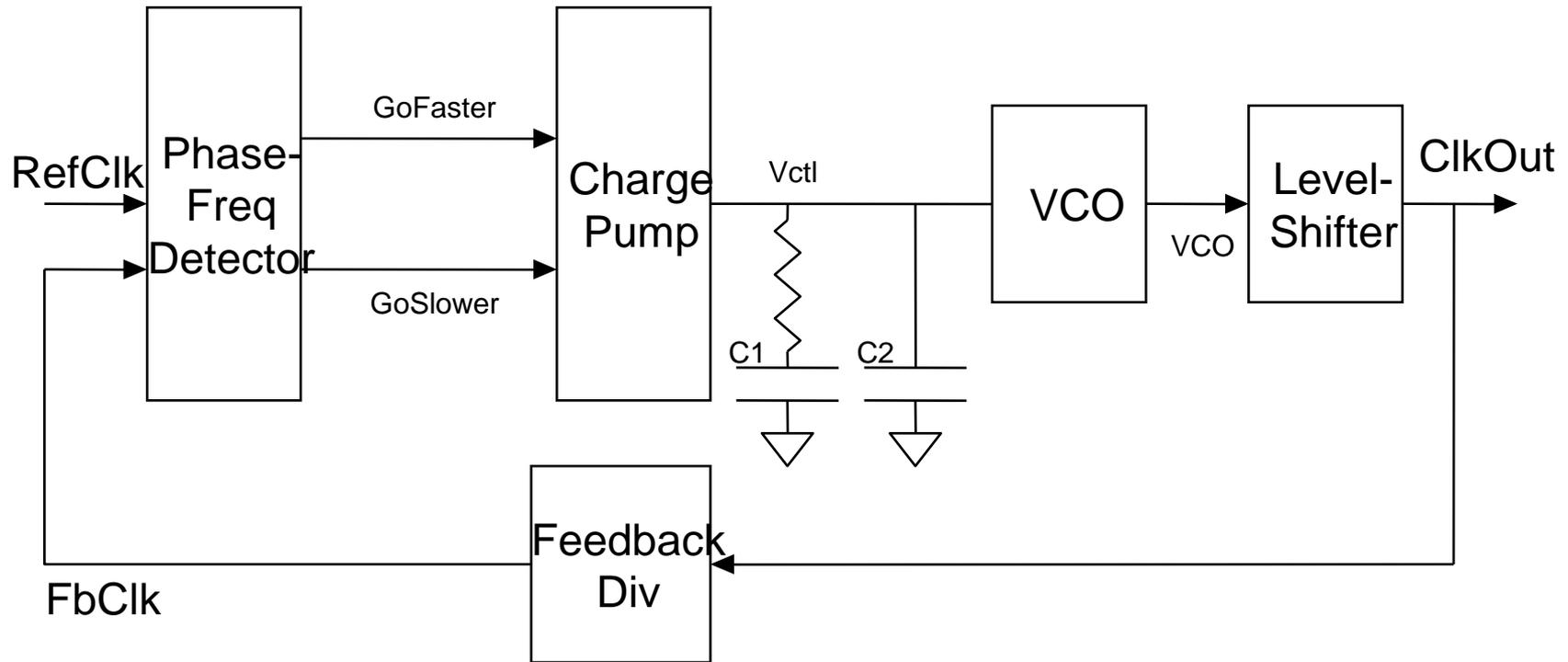


- **Phase = ∫ frequency**

$$\phi(t) = 2\pi \int f(t) dt \leftrightarrow f(t) = \frac{1}{2\pi} \frac{d\phi(t)}{dt}$$

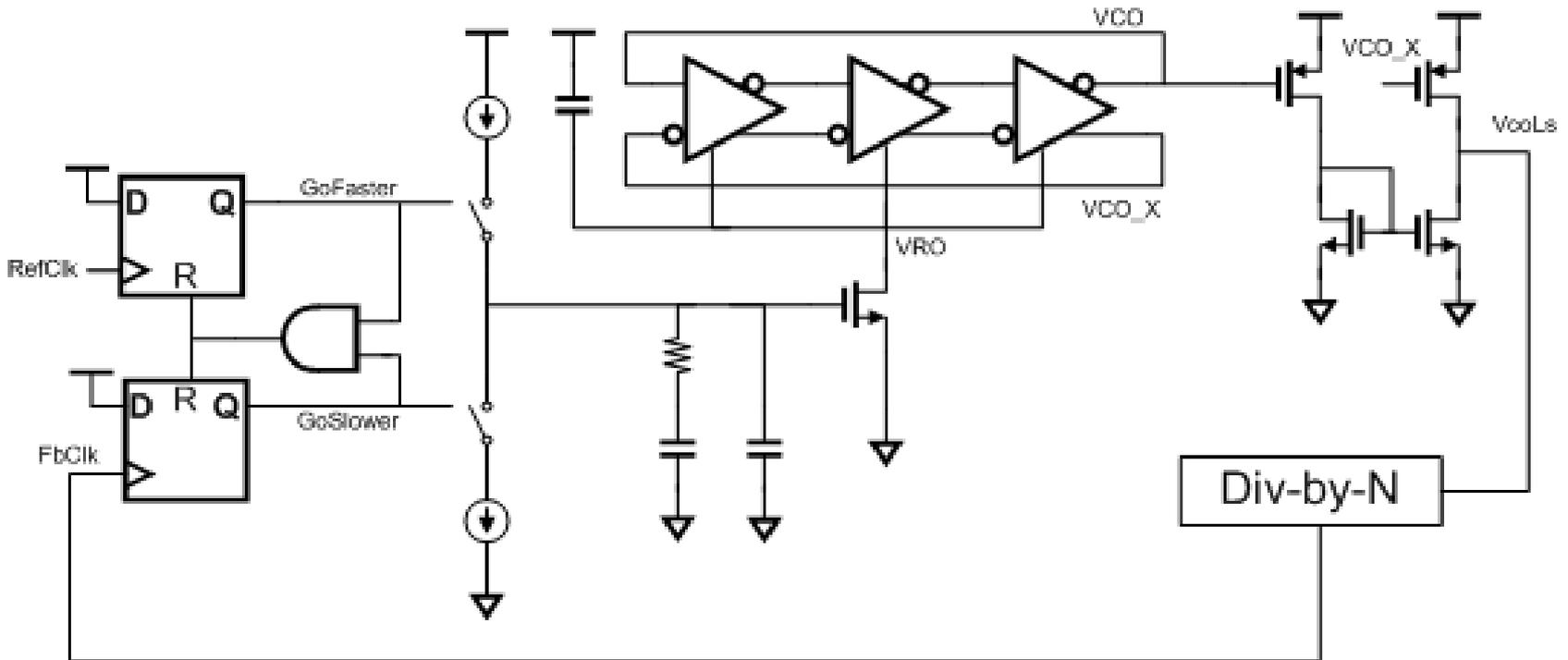
- **When phase-locked,** $\phi_{out} = N\phi_{in} \rightarrow f_{out} = Nf_{in}$

Charge-Pump PLL Block Diagram

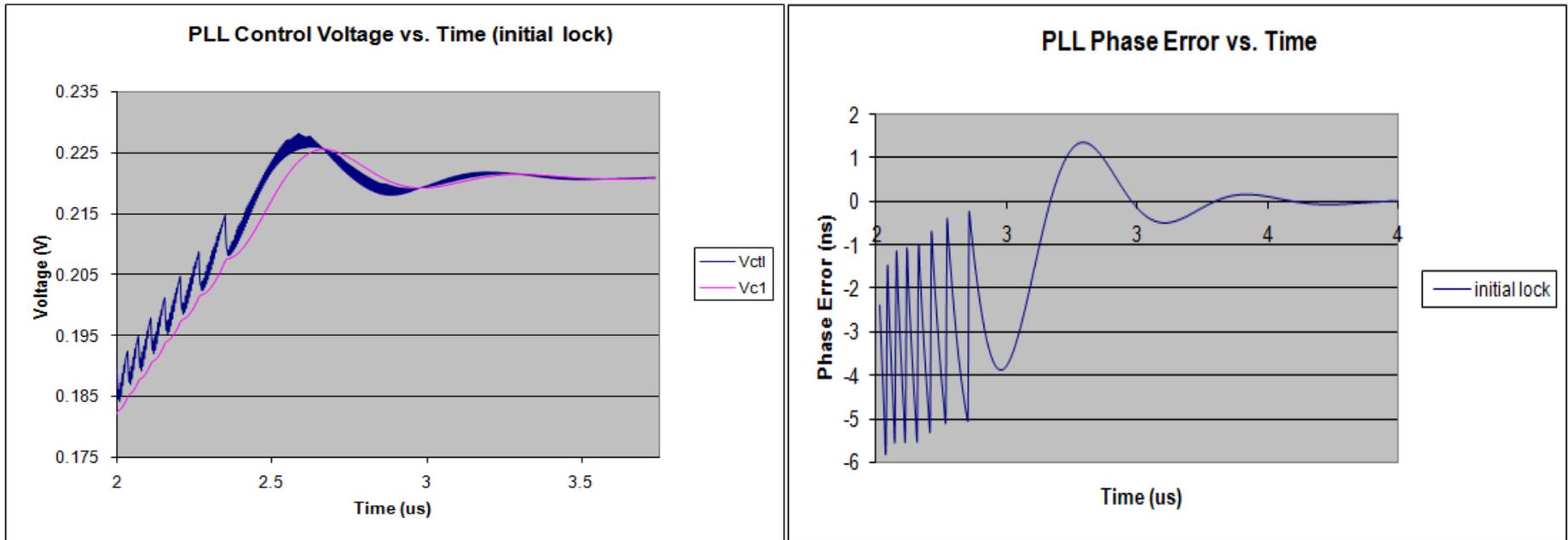


- Sampled-system (phase-error is input variable)
- Phase error is corrected by changing frequency ($\phi(t) = \int f(t) dt$)
- Resistor provides means to separate correction of frequency error from correction of phase error

PLL Circuit Diagram



PLL Circuit Diagram



- Observations

- Under-damped PLL - ringing
- Effect of cycle slips on Vctl
- Net integrating cap voltage Vc1 lags control voltage Vctl

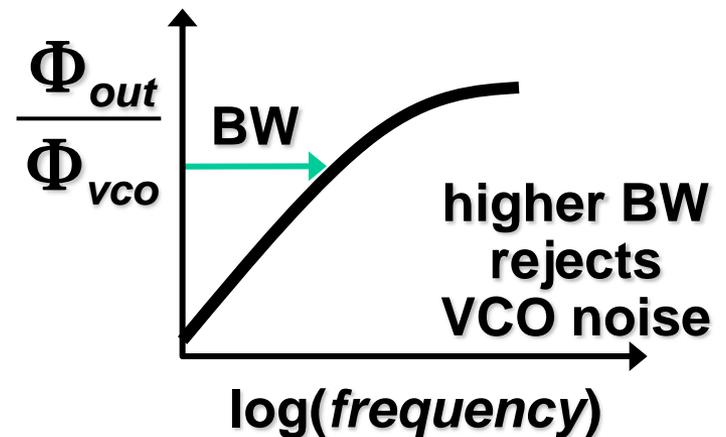
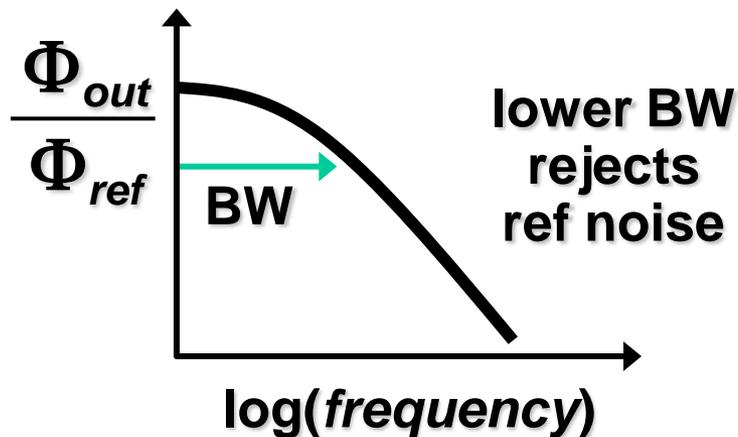
Components in a Nutshell

- **Phase-Frequency Detector (PFD)**: outputs digital pulse whose width is proportional to sampled phase error
- **Charge Pump (CP)**: converts digital error pulse to analog error current
- **Loop Filter (LPF)**: integrates (and low-pass filters in continuous time) the error current to generate VCO control voltage
- **VCO**: low-swing oscillator with frequency proportional to control voltage
- **Level Shifter (LS)**: amplifies VCO levels to full-swing
- **Feedback Divider (FBDIV)**: divides VCO clock to generate FBCLK clock for phase comparison w/reference

PLL Feedback Loop Theory

What Does PLL Bandwidth Mean?

- PLL acts as a low-pass filter with respect to the reference modulation. High-frequency reference jitter is rejected
- Low-frequency reference modulation (e.g., spread-spectrum clocking) is passed to the VCO clock
- PLL acts as a high-pass filter with respect to VCO jitter
- “Bandwidth” is the modulation frequency at which the PLL begins to lose lock with the changing reference (-3dB)



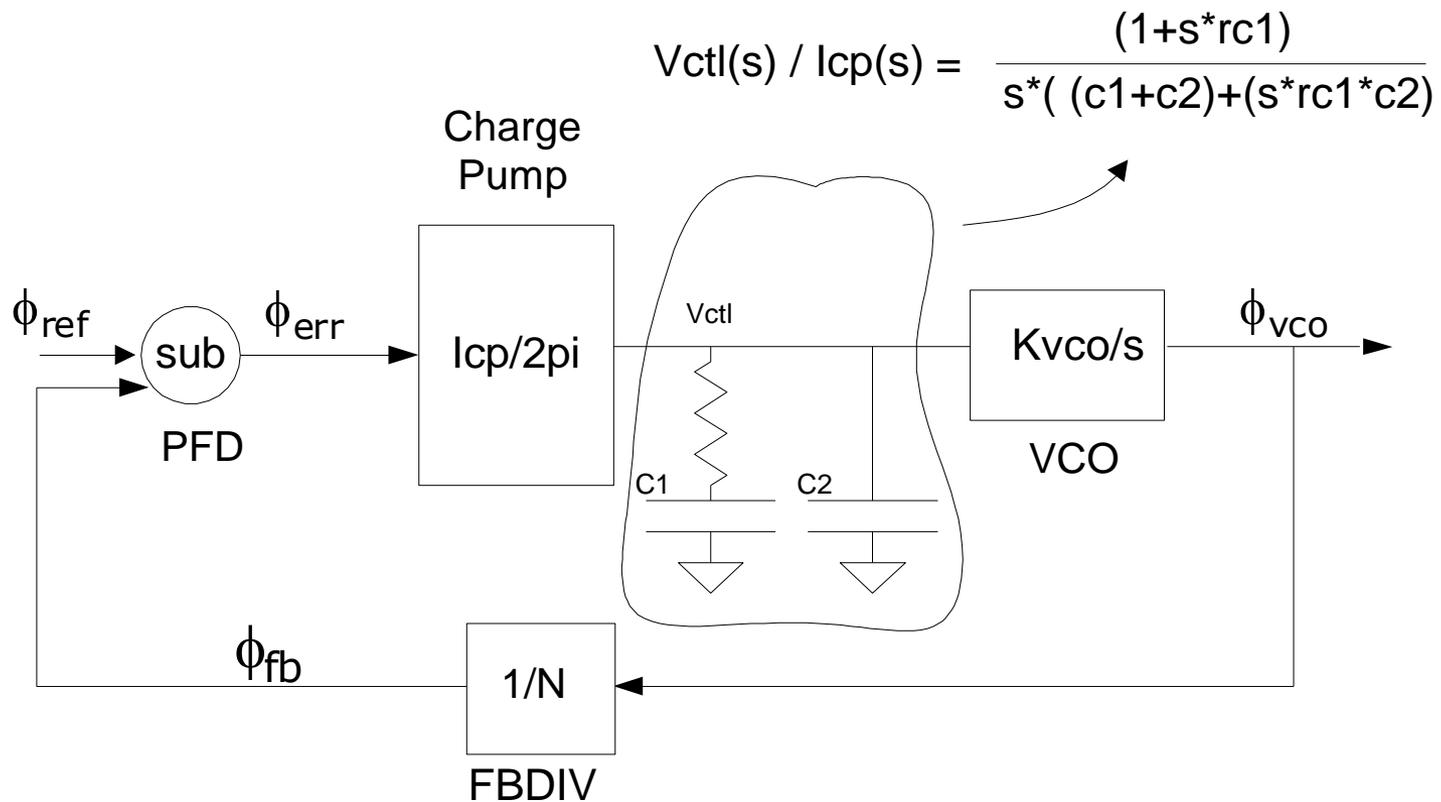
Closed-Loop PLL Transfer Function

- Transfer function describes how PLL responds to “excess” reference phase. i.e. RefClk phase modulation
- Analyze PLL feedback in frequency-domain
 - *Phase* is state variable, not frequency
 - “s” is the reference modulation frequency, not reference oscillation frequency
 - Assumes continuous-time (not sampled) behavior
- $\phi_{fb} = (\phi_{ref} - \phi_{fb}) * G(s)$ where $G(s) ==$ open-loop gain
- $H(s) = \phi_{fb}/\phi_{ref} = G(s)/(1+G(s))$

Open-Loop PLL Gain

- $G(s) = (K_{VCO}/s)I_{cp}F(s)*e^{-sT_d}/M$
 - where ϕ_{err}
 - K_{VCO} = VCO gain in Hz/V
 - I_{cp} = charge pump current in Amps
 - $F(s)$ = loop filter transfer function in Volt/Amp
 - M = feedback divisor
 - T_d = delay in feedback-loop (e.g. $FBDIV, T_{pfd}/2$)

PLL Components in Frequency Domain

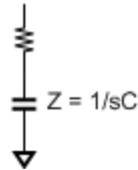


Closed-loop PLL Transfer Function

- $H(s) = \omega_n^2 (1 + s/\omega_z) / (s^2 + 2s\zeta\omega_n + \omega_n^2)$
 - where
 - ω_n = undamped natural frequency (rad/s)
 - ω_z = stabilizing zero = $1/RC_1$ (rad/s)
 - ζ = damping factor
 - 2nd-order (two poles p_1, p_2 and one zero)
 - 2nd-order ignores C_2 cap and feedback delays
- If $\zeta < 1$, complex poles lead to damped oscillation
 - Real \rightarrow exponential decay ($\zeta\omega_n$), Imag \rightarrow oscillation (ω_n)
- If $\zeta > 1$, z and p_1 cancel: BW(-3dB) $\sim 2\zeta\omega_n$
 - Acts like single-pole system

What is a “Zero”?

- The “Zero” in the numerator of the closed-loop transfer function is the frequency in radians/s where the gain of the integral and proportional paths are equal.



- Classic loop: $\omega_z = 1 / RC_1$ (rad/s)
- Concept can be applied to loop filters that do not contain a resistor.

Natural Frequency

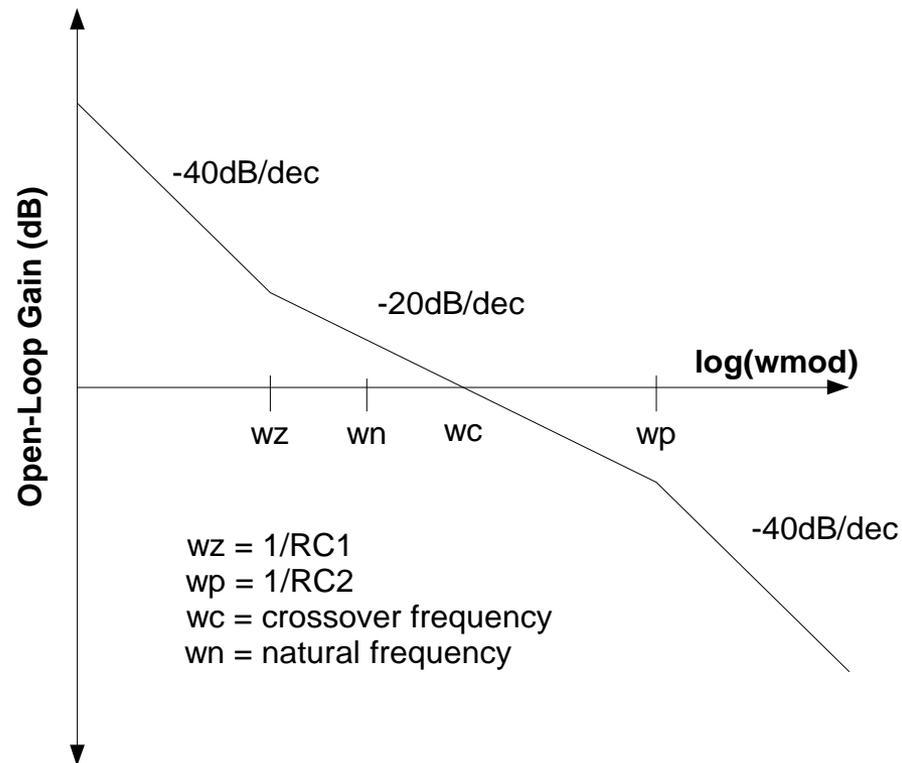
- Related to bandwidth
 - $\omega_n = (2\pi * BW) / \text{sqrt}(1 + 2\zeta^2 + \text{sqrt}((1 + 2\zeta^2)^2 + 1))$
- Undamped Natural Frequency:
 - $\omega_n = \text{sqrt}(K_{\text{vco}} * I_{\text{cp}} / (M * C_1))$ in rad/sec
 - where
 - $K_{\text{vco}} = \text{VCO gain in Hz/V}$
 - $I_{\text{cp}} = \text{charge pump current in Amps}$
 - $M = \text{feedback divisor}$
 - $C_1 = \text{large LPF capacitor}$
 - For stability: $\omega_n / 2\pi < \sim 1/15$ reference frequency
- Typical value: $500 \text{ kHz} < \omega_n / 2\pi < 10 \text{ MHz}$

Damping Factor

- Related to stability
- Damping Factor: $\zeta = R_{\text{lpf}} * C_1 * \omega_n / 2$
 - Dimensionless, Usually $\sim 0.45 < \zeta < \sim 2$
 - Lower end of range for low period jitter
 - Higher end of range for accurate ref phase tracking
 - R_{lpf} provides means to set stability independent of bandwidth

Open-Loop Transfer Function

- $20 \cdot \log(\text{Gain})$ vs. $\log(\text{Modulation Frequency})$
- 2 poles @ origin, 1 zero @ w_z , 1 pole @ w_p

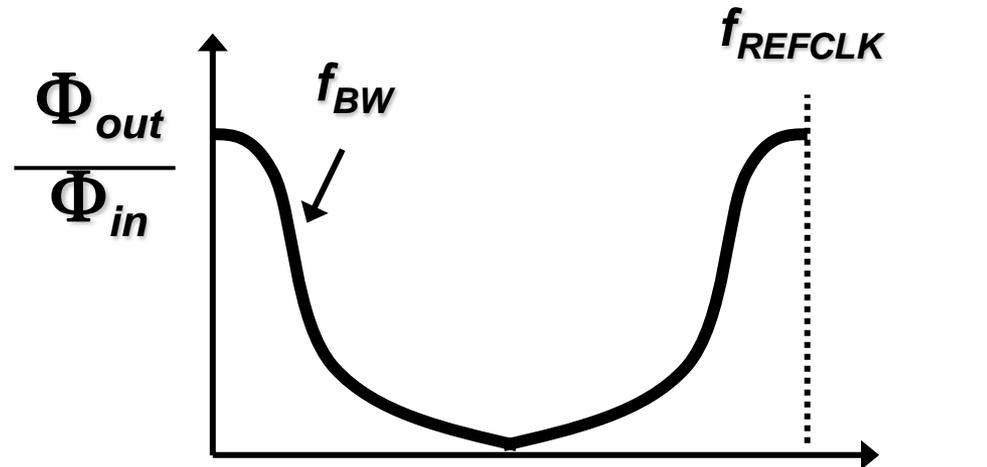


Stability and Phase Margin

- Phase margin determines stability as in other feedback loops $\rightarrow 180$ - phase of open-loop transfer function at crossover frequency
- ϕ_m (degrees) = $(180/\pi) * (\text{atan}(\omega_c * RC_1) - \text{atan}(\omega_c * RC_2) - \omega_c * T_{dly})$
 - ω_c == crossover frequency
 - frequency where open-loop gain $G(s) = 0\text{dB}$
 - For stability: $1/RC_1$ (zero) $< \omega_c < 1/RC_2$ (parasitic pole)
 - Typical Range: $1.2 * \omega_n < \omega_c < 2.5 * \omega_n$
- Phase margin (ϕ_m) $\sim 100 * \zeta$ (for $\zeta < 0.5$)
 - Usually $45^\circ < \text{PM} < 70^\circ$

Aliasing in a Sampled Loop

- Sampling nature of PFD \rightarrow frequency-domain aliasing
 - Can't low-pass filter ref noise before PFD sampling – unlike A/D's
 - Need z-domain analysis for accurate PLL modeling – analogous to sample-and-hold
- Phase of modulation with respect to ref affects aliasing
 - e.g. ref modulation at $\frac{1}{2} * f_{ref}$. No jitter if sampled at $0^\circ, 180^\circ$, max at $90^\circ, 270^\circ$
- Modulation at frequencies $>$ Nyquist ($f_{ref}/2$) appears at other frequencies
 - e.g. $f_{ref}=100\text{MHz}$ \rightarrow ref modulation at 99MHz looks just like 1MHz ref modulation to the PLL
 - continuous-time model says that PLL should reject more 99MHz noise than 1 MHz noise



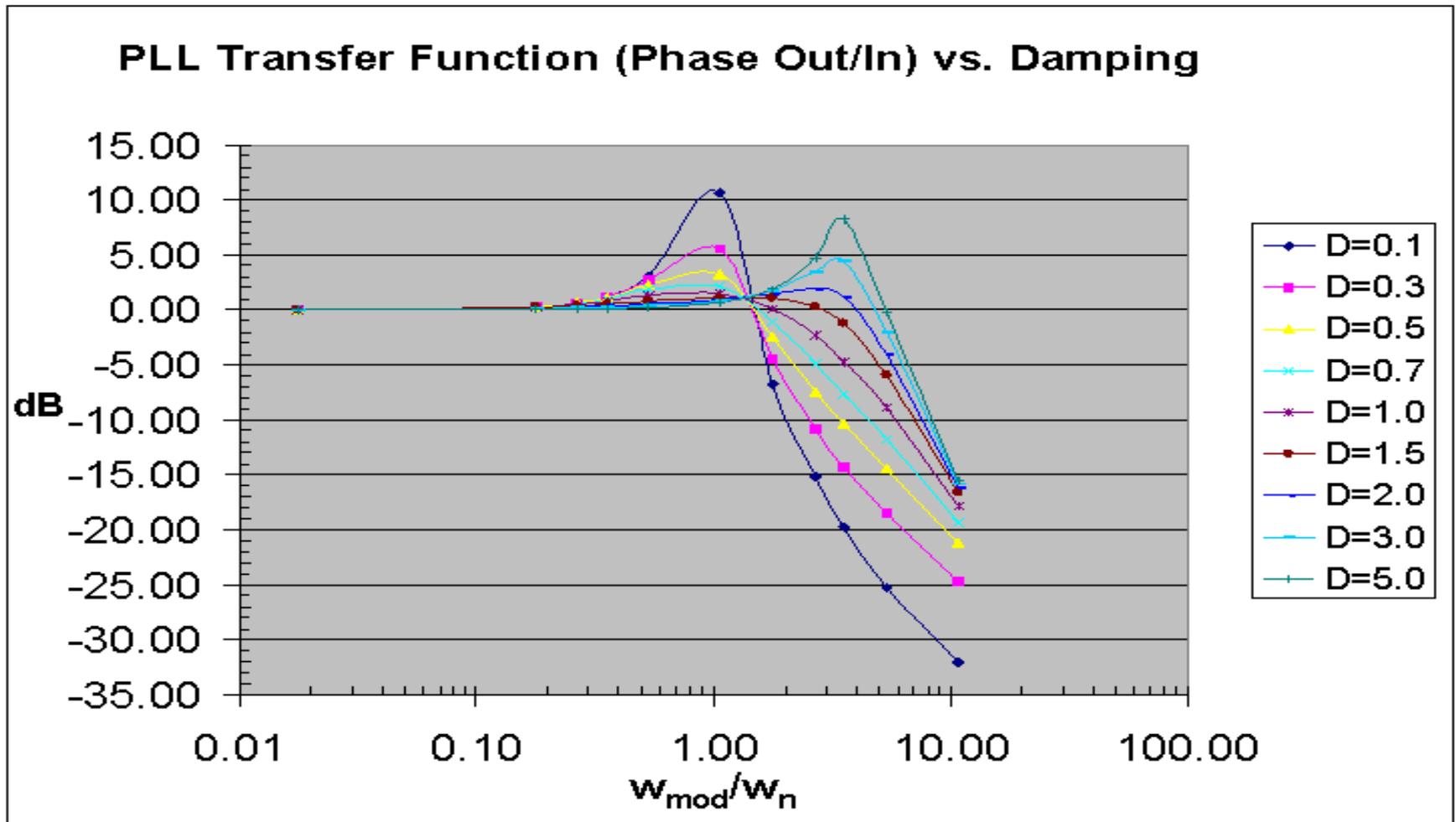
PLL Response to Reference Modulation

Phase Tracking vs. Damping

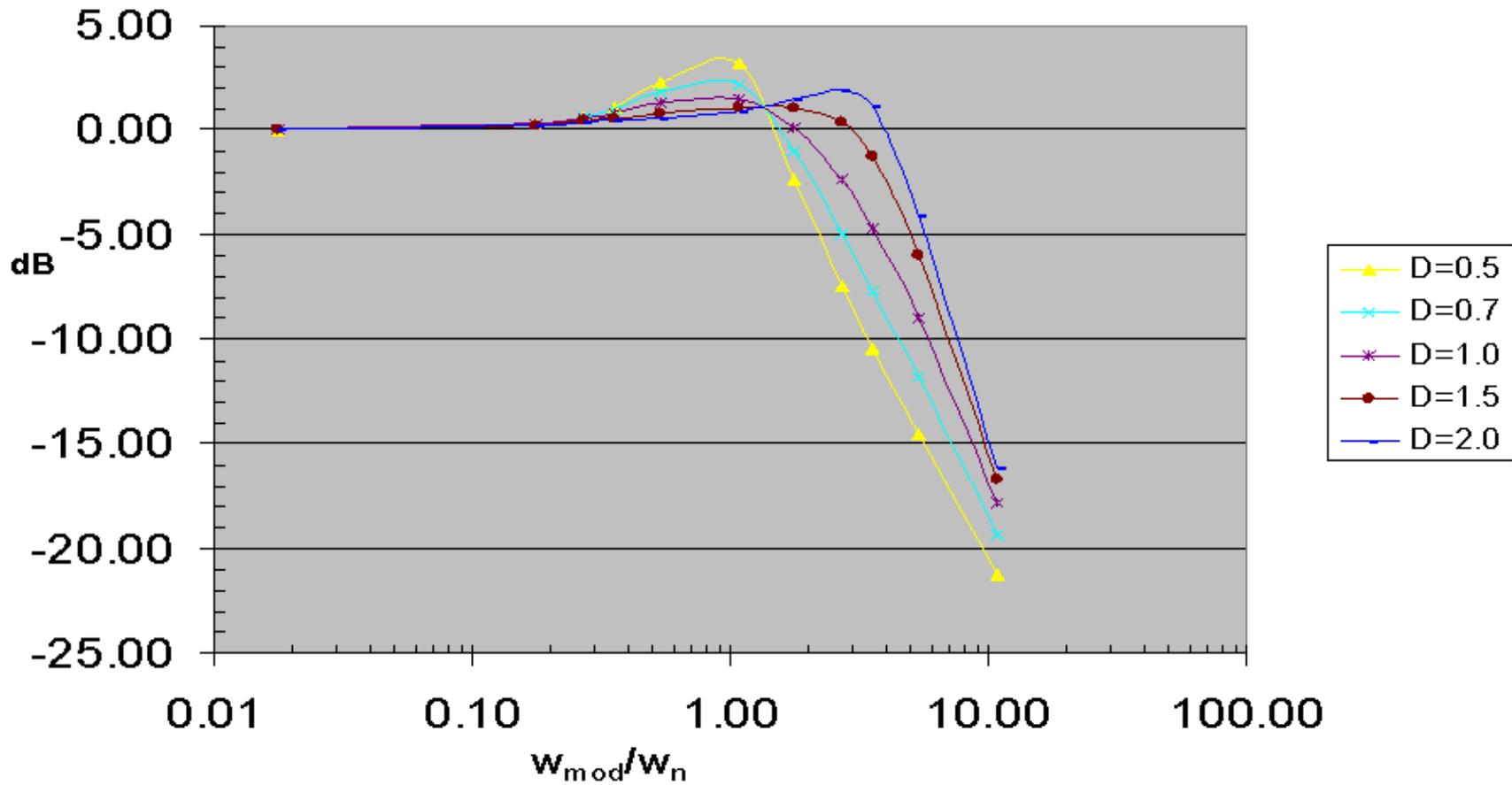
- Phase Tracking vs. Damping
- Closed-loop Transfer Function (ϕ_{fb}/ϕ_{ref})
- Phase Tracking → think “accumulated” period jitter or phase error
- Peaking at low and high damping factors → bad
- Peaking at high damping due to smoothing capacitor pole ($1/RC_2$) and/or under-sampling (Gardner)
- Peaking very sensitive to parasitic pole ($1/RC_2$) at high R
- Min peaking w/damping $\sim 1.0 - 1.5$ if $C_2 \sim 5\% * C_1$
- Typical peaking: 1 – 3 dB (CPU high-end, IO low-end)
- For lower peaking, damping > 2 and C_2 small

- Simulation Condition (following slides): $C_2 = 6.7\% * C_1$

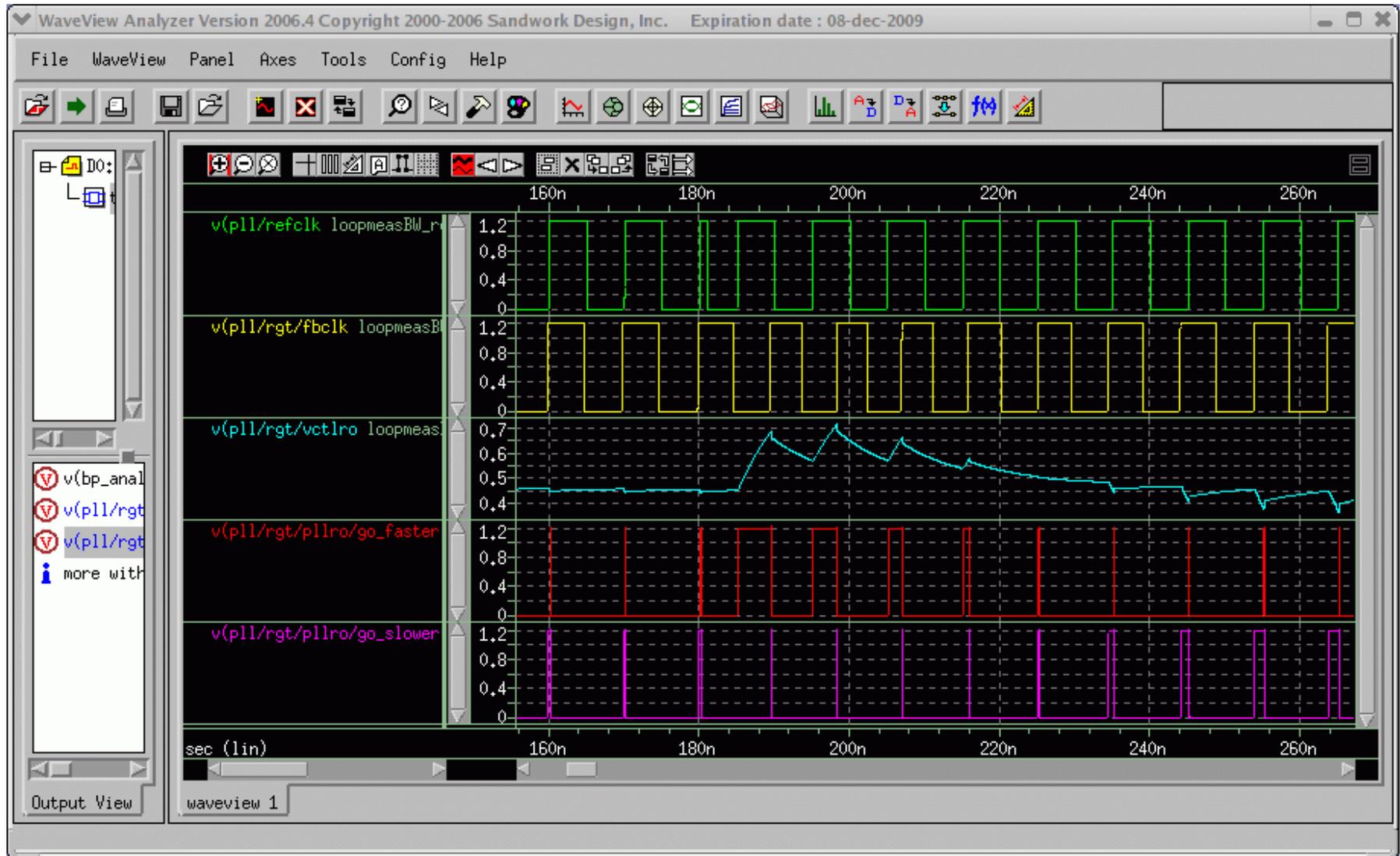
Closed-loop Transfer Function



PLL Phase Transfer Function (FB/Ref) vs. Damping



Phase Response to Ref Step



Time-Domain Phase Response to Reference Step

- Transient Simulation Conditions (behavioral model):
 - step reference phase by 2π radians. Observe phase overshoot
 - $C_2 = 10\% * C_1$ (high end of C_2 range requires lower ζ)
- Less ringing and overshoot as $\zeta \rightarrow 1$
- Severe under-damping \rightarrow slow ringing and overshoot
- Severe over-damping \rightarrow fast ringing and overshoot
- Ringing at high damping due to smoothing pole (large RC_2) and/or low over-sampling

Time-Domain Phase Response to Reference Step

- From Gardner "Phaselock Techniques, 3rd Ed." (p. 102) – ignores parasitic poles and over-sampling rate

- $\zeta < 1$

$$T_{err} = T_{step} * [(\cos(\sqrt{1-\zeta^2} * \omega_n t) - (\zeta/\sqrt{1-\zeta^2}) * \sin(\sqrt{1-\zeta^2} * \omega_n t))] * e^{-\zeta \omega_n t}$$

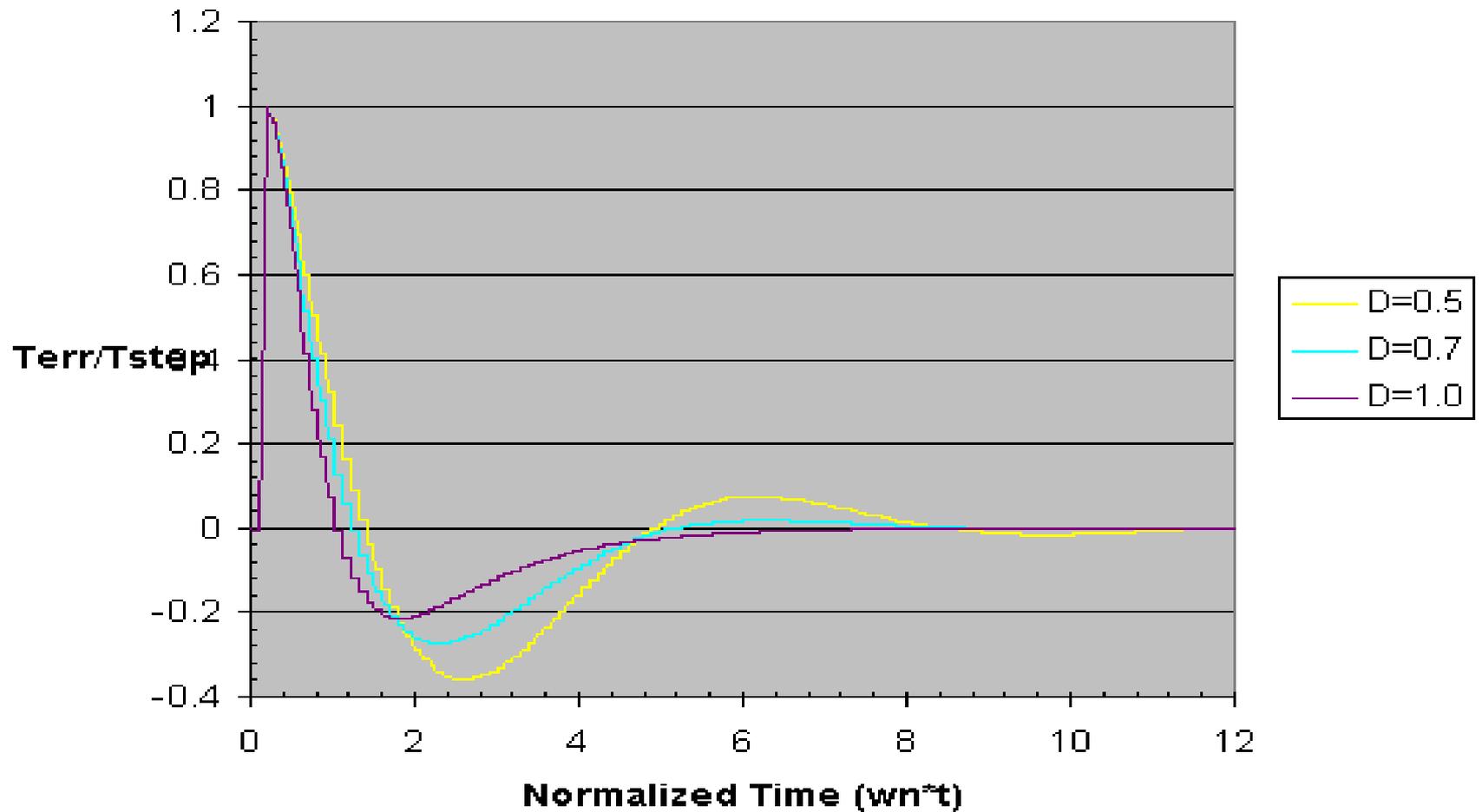
- $\zeta = 1$

$$T_{err} = T_{step} * (1 - \omega_n t) * e^{-\omega_n t}$$

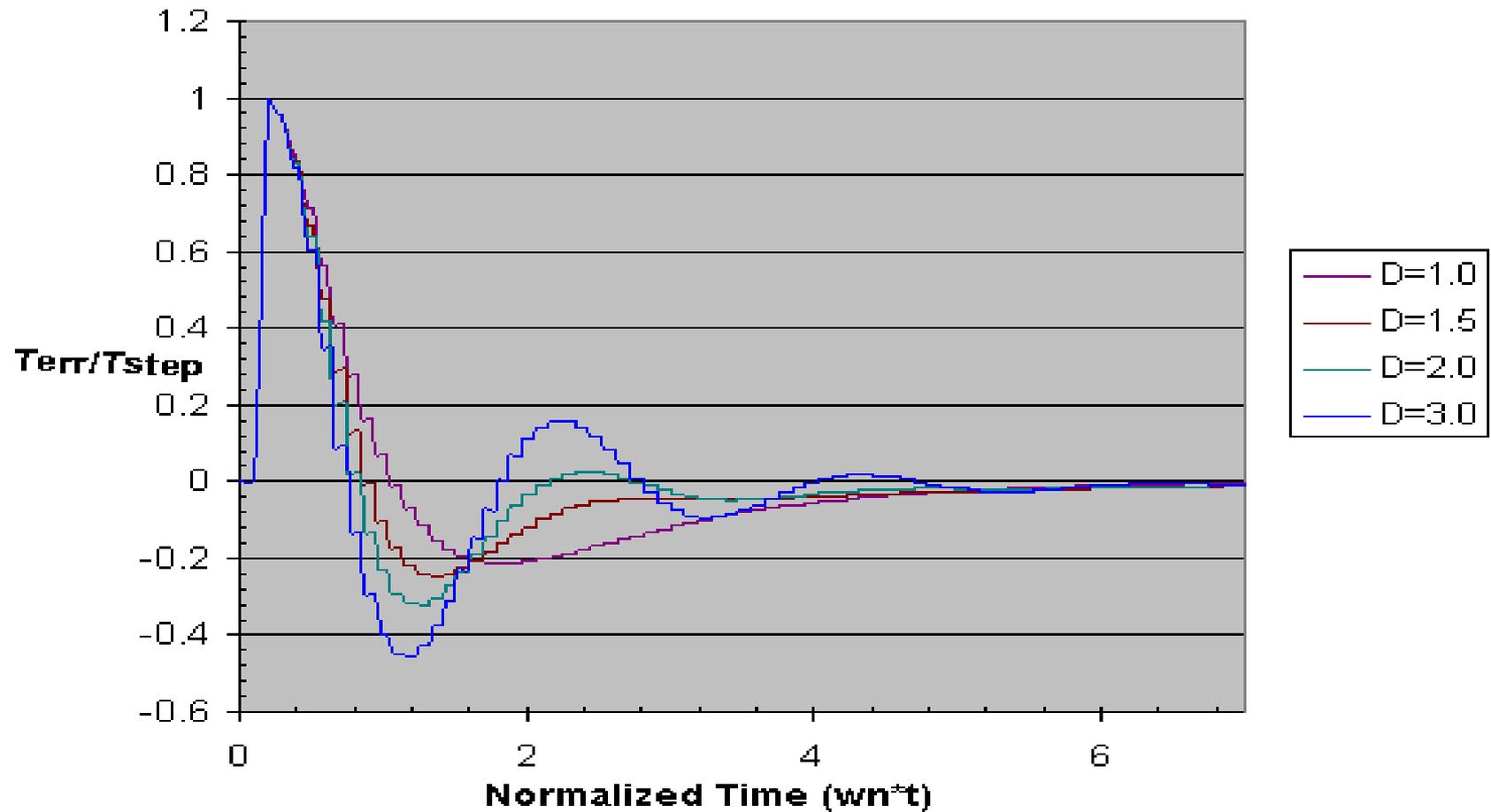
- $\zeta > 1$

$$T_{err} = T_{step} * [(\cosh(\sqrt{\zeta^2 - 1} * \omega_n t) - (\zeta/\sqrt{\zeta^2 - 1}) * \sinh(\sqrt{\zeta^2 - 1} * \omega_n t))] * e^{-\zeta \omega_n t}$$

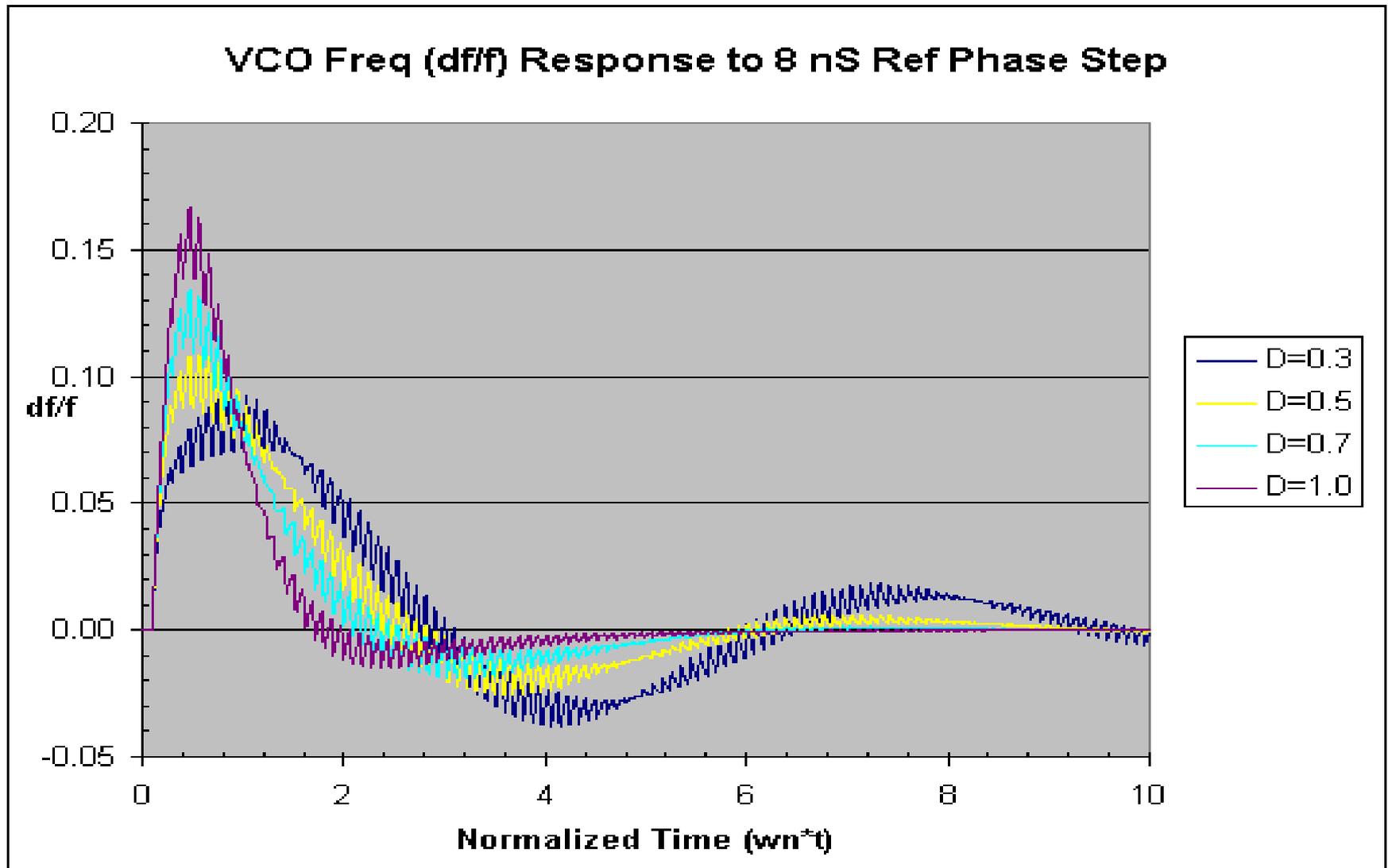
Phase Response (T_{err}/T_{step}) to 8 nS Ref Phase Step



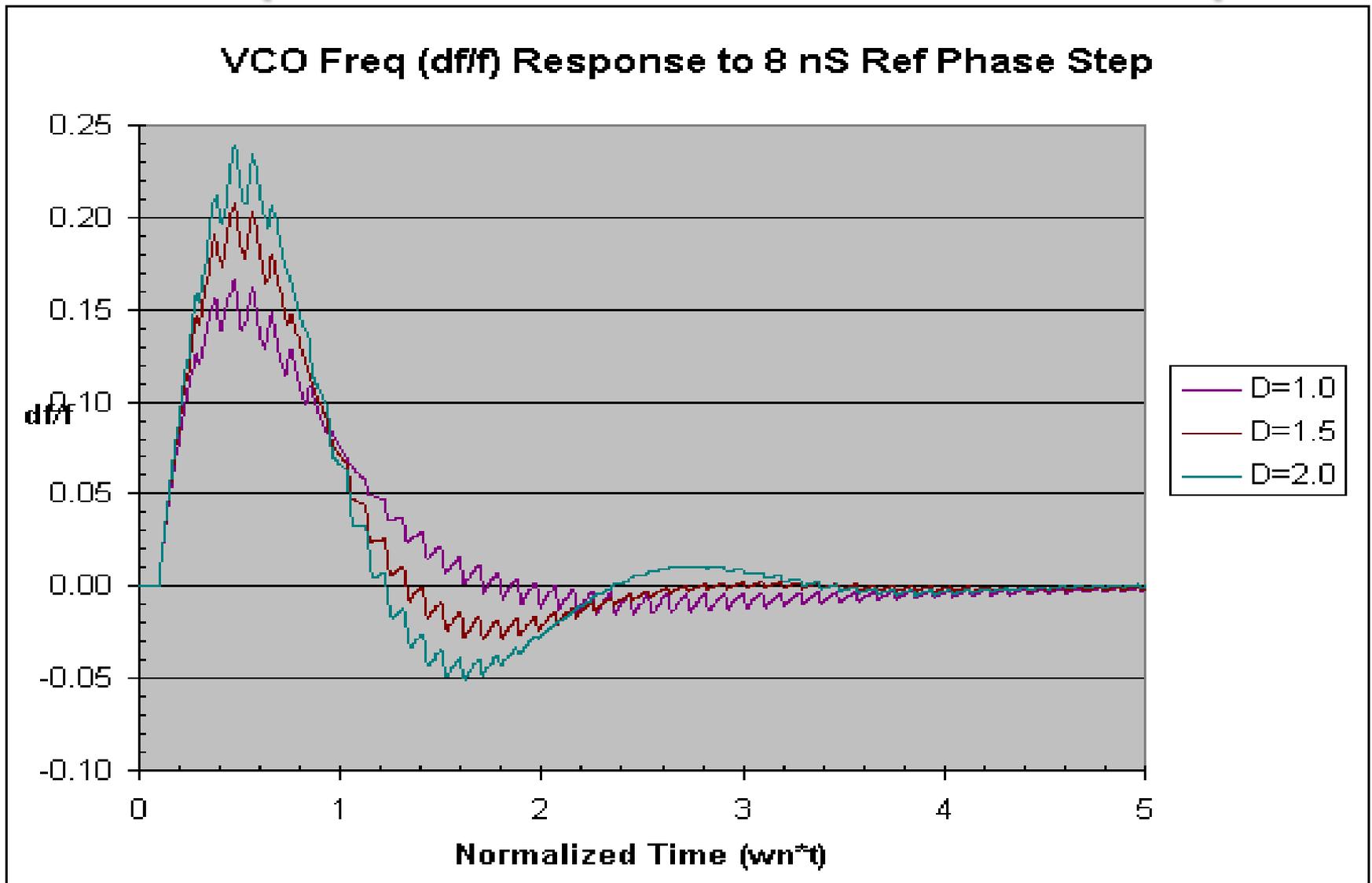
Phase Response (T_{err}/T_{step}) to 8 nS Ref Phase Step



Frequency Response to Ref Step



Freq Overshoot from Ref Step



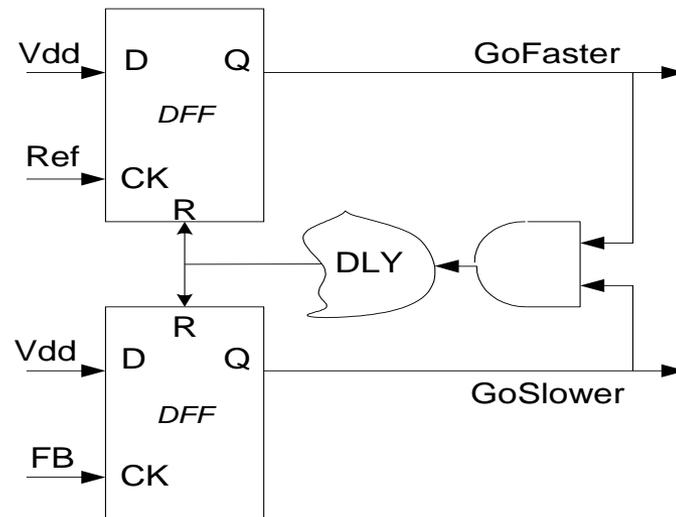
PLL Circuits

- Phase-Frequency Detector
- Charge-Pump
- Loop Filter
- Voltage-Controlled Oscillator
- Level-Shifter
- Feedback Divider
- Voltage Regulator

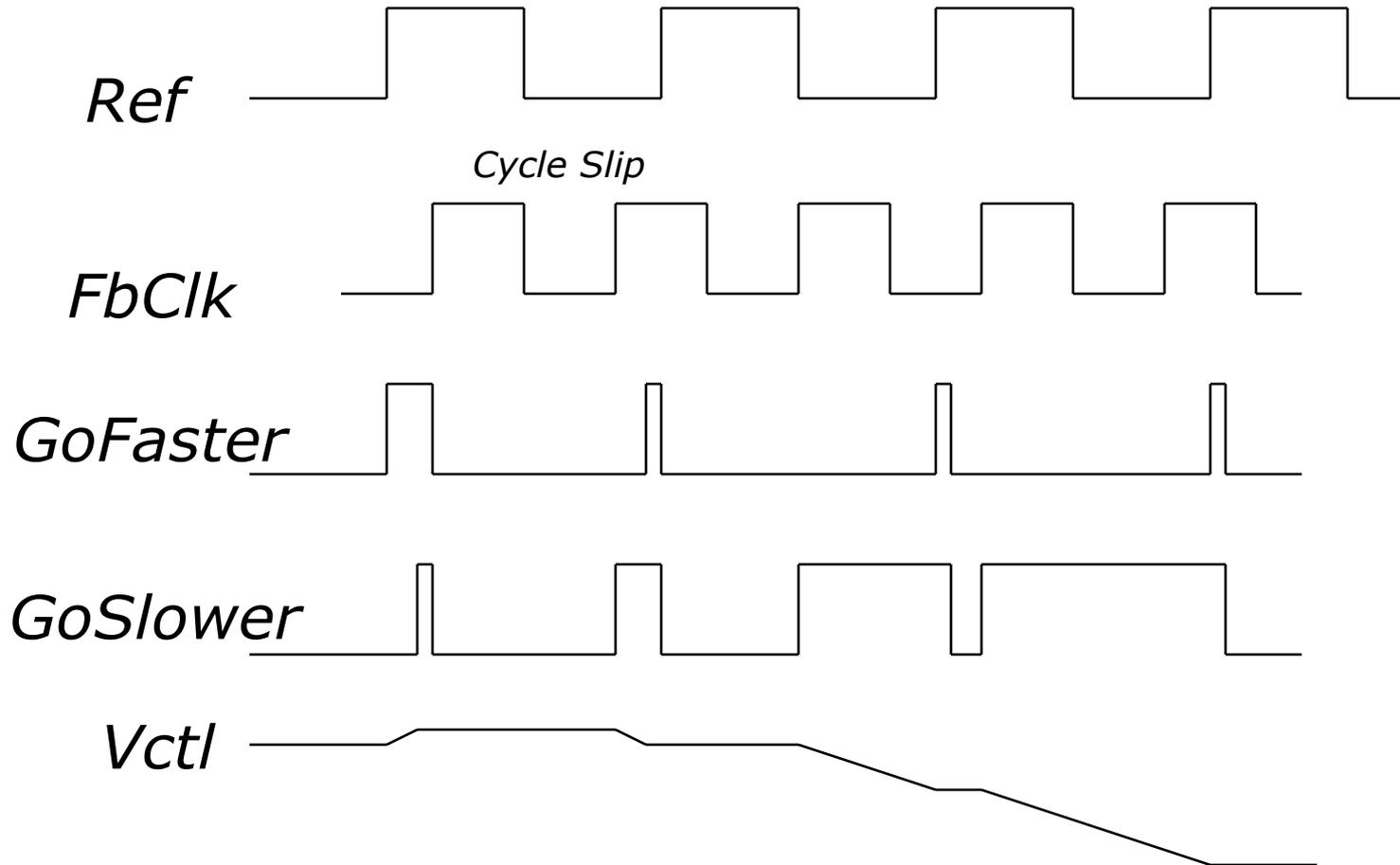
Phase-Frequency Detector(PFD)

PFD Block Diagram

- Edge-triggered
 - Input duty-cycle doesn't matter
- Frequency correction takes precedence over phase correction – no harmonic locking – 3 state operation
- Output pulse-widths proportional to phase error
- Reset delay to provide minWidth on output pulses to avoid “dead-zone”
- Symmetric NAND used to balance equalize delays from both inputs
- PFD fails as T_{reset} approaches $T_{\text{ref}} \rightarrow$ limit cycles
 - Challenge for Gb/sec IO links
 - Pulsed-flop designs can be faster

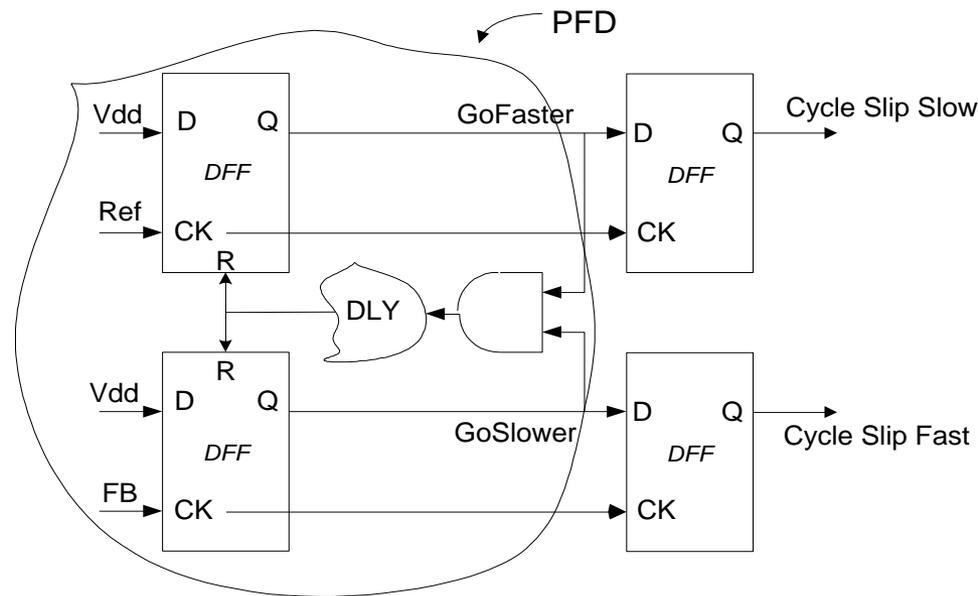


Example: PFD

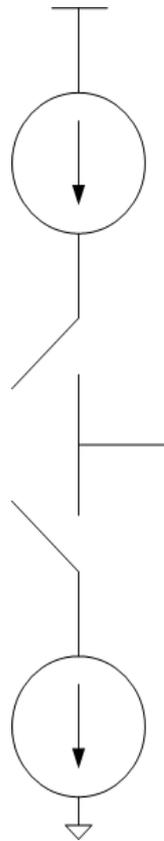


Frequency Lock Detector

- Sample PFD GoFaster signal with rising RefClk
- Sample PFD GoSlower signal with rising Fbclk
- If either sampled signal is TRUE, then PFD detected two consecutive RefClk's or FbClk's → cycle slip and loss of frequency lock
- May apply "sticky bit" to result to capture temporary loss of lock
- Sample GoFaster/GoSlower with falling edges of RefClk/Fbclk to detect 180 degrees phase error



Charge Pump(CP)



Charge-Pump Wish List

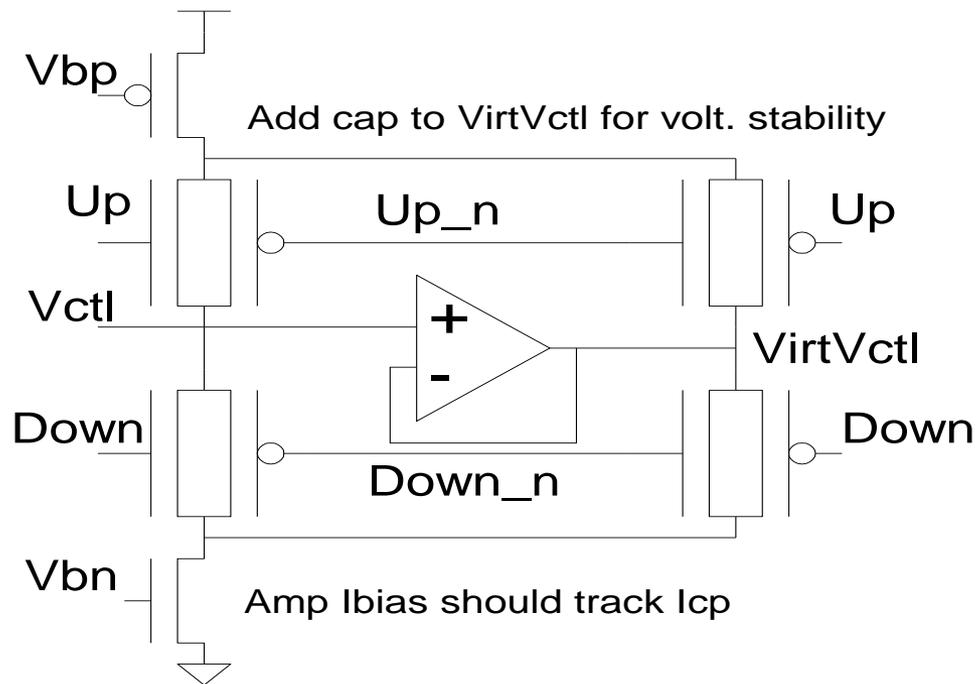
- Equal *UP/DOWN* currents over entire control voltage range - reduce static phase error
- Minimize mismatch caused by finite current sources g_{ds} and V_t mismatches
 - $\Delta V_t \sim 1 / \text{sqrt}(W*L)$
 - long L in current sources for higher r_{out}
 - Stacked (a.k.a. common) gates in $I_{sources}$ reduce mismatch
 - use replica-bias CP and feedback amplifier to balance I_{up}/I_{down}
 - beware of mismatch between two CP cells
 - increase in CP's phase noise due to finite BW of this feedback?
- Minimal coupling to control voltage during switching and leakage when off - reduce jitter and phase drift
- Insensitive to power-supply noise and process variations - loop stability

Charge-Pump Wish List

- Minimize coupling caused by “clock feedthrough” (C_{gd}) and charge-injection – big problem
 - 1/2 sized dummy switches to reduce charge-injection
 - $Q_{inj} \sim 1/2 * C_{ox} * (W * L) * (V_{gs} - V_t)$
 - Small (and/or limited swing) switches to reduce clock feedthrough – watch for leakage with limited-swing
 - Balance timing and slew rates of Up/Down inputs
- Reduce PFD pulse-width to minimize device noise while still avoiding dead-zone (< 100 ps possible in 65nm) – noise is band-pass filtered by PLL
- Typical I_{cp} : $5\mu A$ (mismatch) < I_{cp} < $300\mu A$ (headroom)

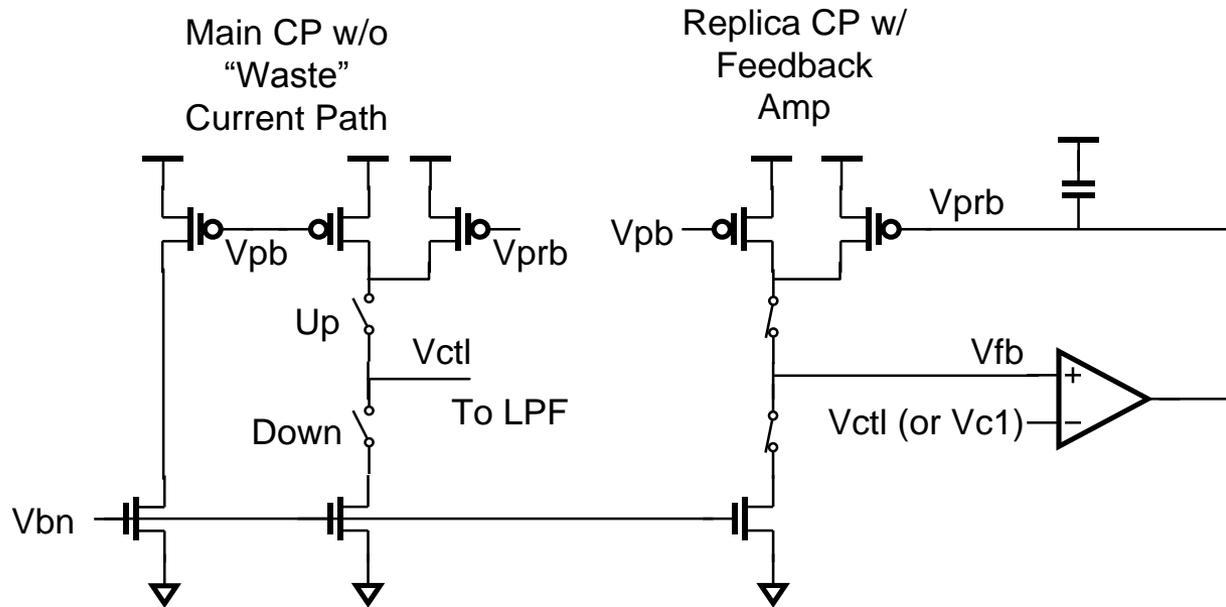
Charge Pump: const I with amp

- Amp keeps V_{ds} of current sources constant (Young '92), sinking "waste" current when UP and/or DOWN off
 - V_{offset} (off) \rightarrow need high-gain amp
 - V_{offset} (on) = $I_{cp}/g_m \rightarrow$ often $I_{amp} > 3-5X I_{cp}$ to reduce offset
 - Both PMOS and NMOS input pairs needed for wide input range



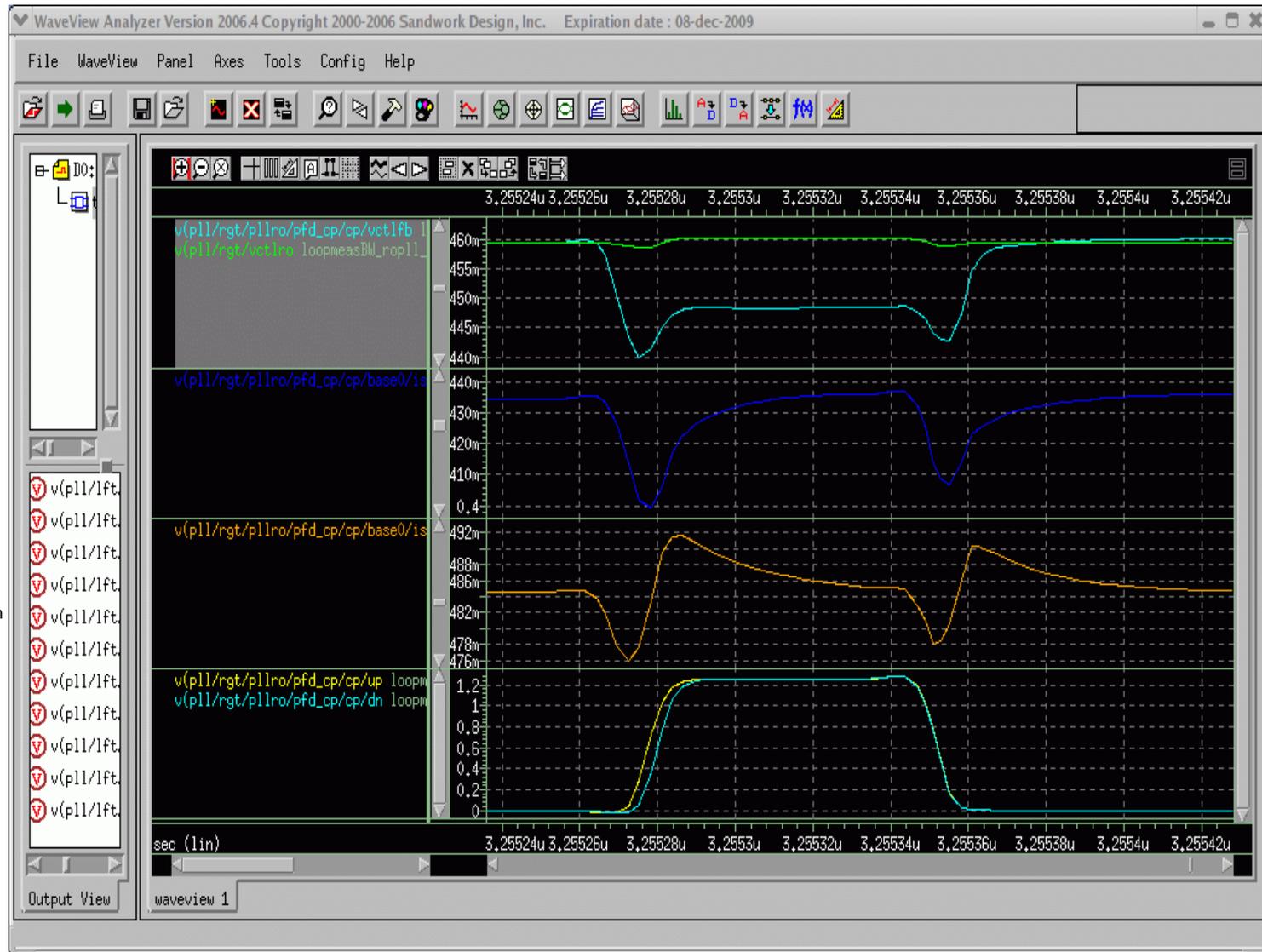
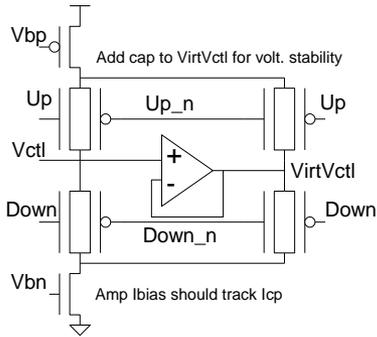
Charge Pump: replica-feedback

- Replica-bias CP and additional amp used to set bias V_{bp} , forcing $I_{up} = I_{dn}$ at low freq
 - Start-up may be needed. Stability a concern



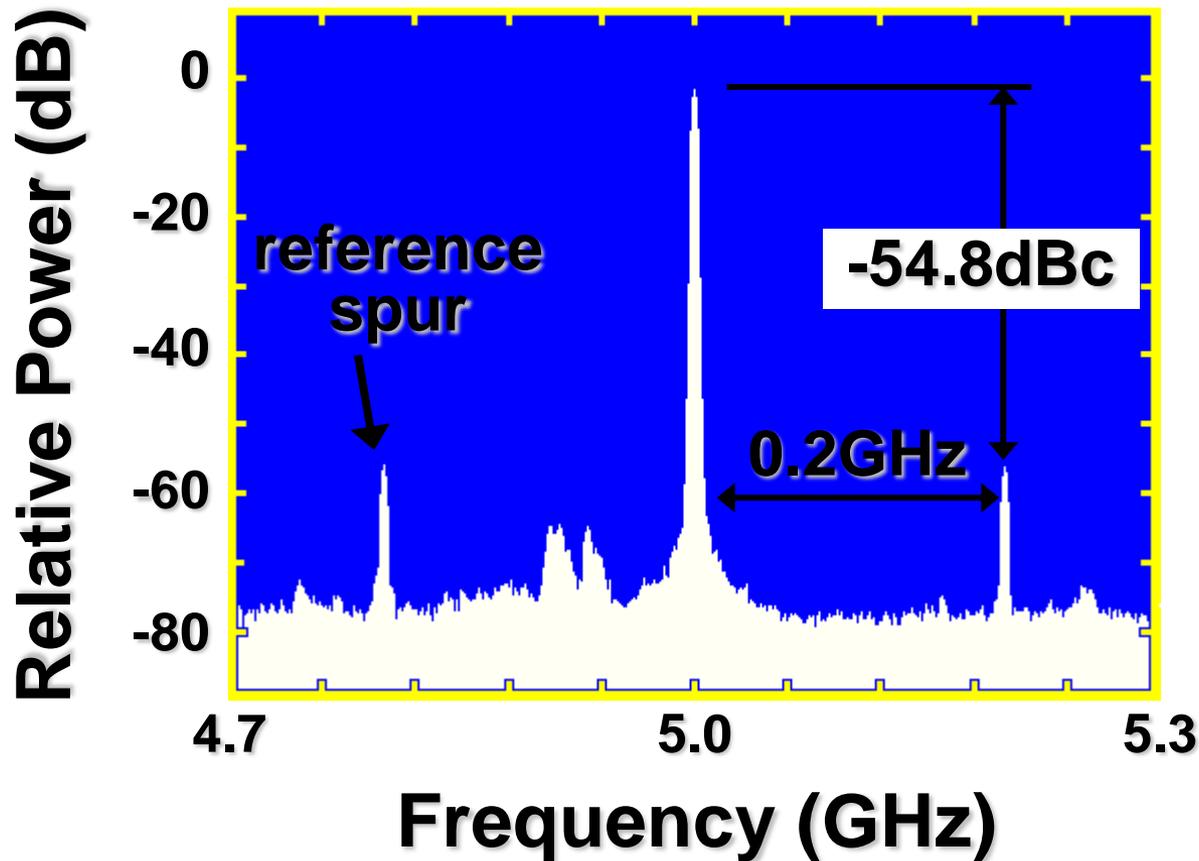
Charge-Pump Switching

- Panel1:
Vctl and
VirtVctl
- Panel2:
Idn drain
- Panel3:
Iup drain
- Panel4:
Up/Down



Spectral Analysis of VCO Clock

- 5GHz VCO clock with 200MHz reference clock

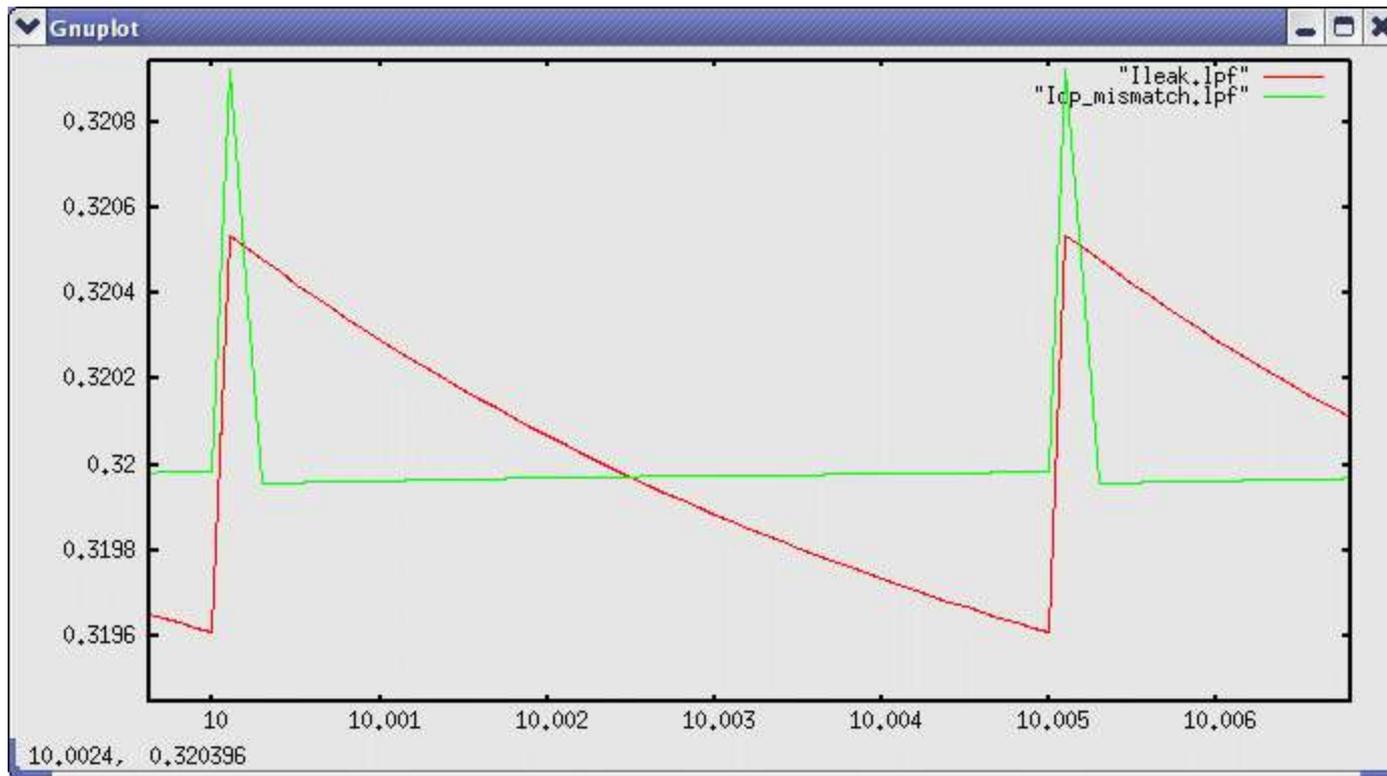


Static Phase Error

- Causes: CP Up/Dn mismatch and/or control voltage leakage
 - Jitter @ T_{ref} (reference spurs) – leakage more serious
- In lock, net control voltage currents must integrate to zero
 - Mismatch example: if *UP* current is 2× larger, then *DOWN* current source must be on 2× as long to compensate and so feedback clock must lead reference for *DOWN* to be on longer
 - $T_{err} = T_{dn} - T_{up} = T_{reset} * (I_{up}/I_{dn} - 1)$
 - Medium-narrow reset pulse → generally lower static error
 - Leakage example: if $T_{ref} = 10\text{ns}$, $I_{leak} = 0.1\mu\text{A}$, $I_{cp} = 10\mu\text{A}$
 - $T_{err} = T_{ref} * I_{leak} / I_{cp} = 100\text{ps}$
- Typical static phase error < 100ps

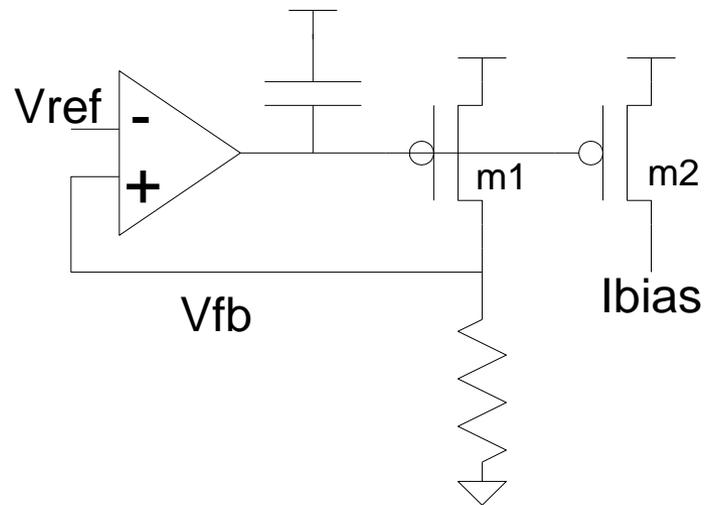
Static Phase Error

- “Green” – Up/Down Mismatch, “Red” – Leakage
- 100 ps static phase error in both cases

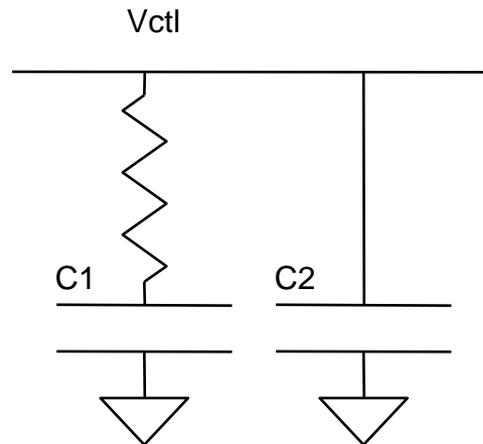


Bandgap-based I_{bias}

- $I_b \sim V_{ref} / R$
- V_{ref} generated from PVT-insensitive bandgap reference
- Con: feedback loop may oscillate
 - capacitor added to improve stability
 - resistor in series w/cap provides stabilizing zero (*not shown*)
- Pro: VDD-independent, mostly Temp independent
- Pro: $I_{cp} * R_{lpf} = \text{constant} \rightarrow$ less PVT-sensitive loop dynamics



Low-Pass Loop Filter (LPF)

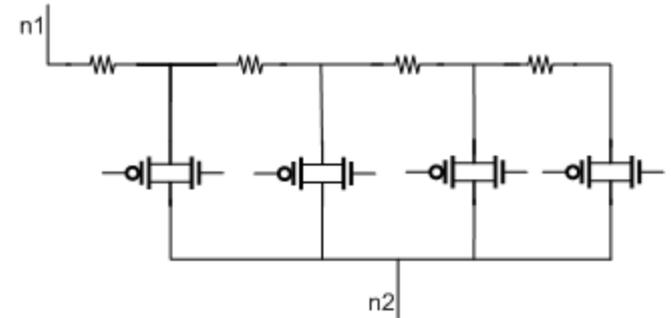


Loop Filter Basics

- Simplest and most commonly-used loop filter is continuous-time, passive filter (1 R, 2 C's) – affects stability and bandwidth
- Integrates low-frequency phase errors onto C1 cap to set avg. freq
- Resistor provides a means of isolating phase correction from frequency correction – $I_{cp} * R_{lpf}$ for stability but R adds thermal noise that is band-pass filtered by PLL
- C₂ cap filters high-freq noise spurs caused by sampling but adds parasitic pole at $1/RC_2$
- Other options include digital(FSM-based) filter, sampled-time filter (see Maneatis, Maxim) , and continuous-time active filter
- Differential designs can reduce sensitivity to VDD and substrate noise and often area by 2×. Requires common-mode feedback loop

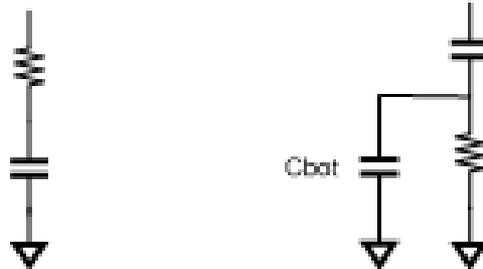
Loop Filter Resistor

- Resistance may be programmable using switches
- Parasitic switch resistance varies with control voltage
 - Usually lowest at V_{ctl} extremes if CMOS transmission gate
 - Large R_{switch} variation vs. V_{ctl} if NMOS or PMOS only
 - Usually $R_{switch} < 5-10\%$ of R_{lpf}
- Minimize gate leakage and noise coupling from switches
 - Coupling less of a problem if using voltage regulators
- Typical values: $500\Omega < R_{lpf} < 50k$
- Poly, Diffusion, Nwell R's most common
- MOSFET R's sometimes used if R placed "below" C1 cap
 - Constant V_{gs} needed



Integrating Cap Configuration

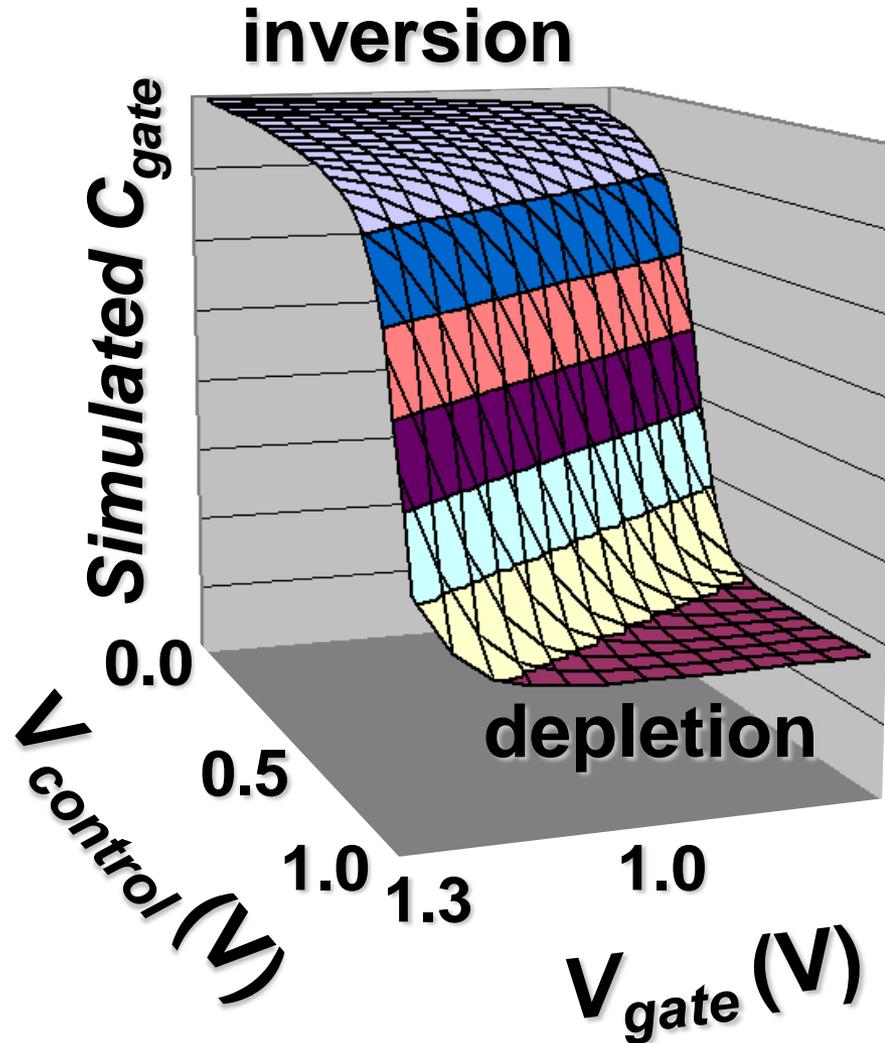
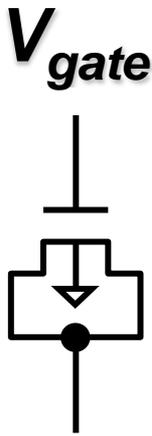
- Integrating cap (C1) may be placed “above” or “below” loop filter resistor
- Parasitic “bottom” capacitance for C1 “above” configuration
- Variable resistance if switches used in programmable resistor for C1 “below” configuration



Loop Filter Capacitors

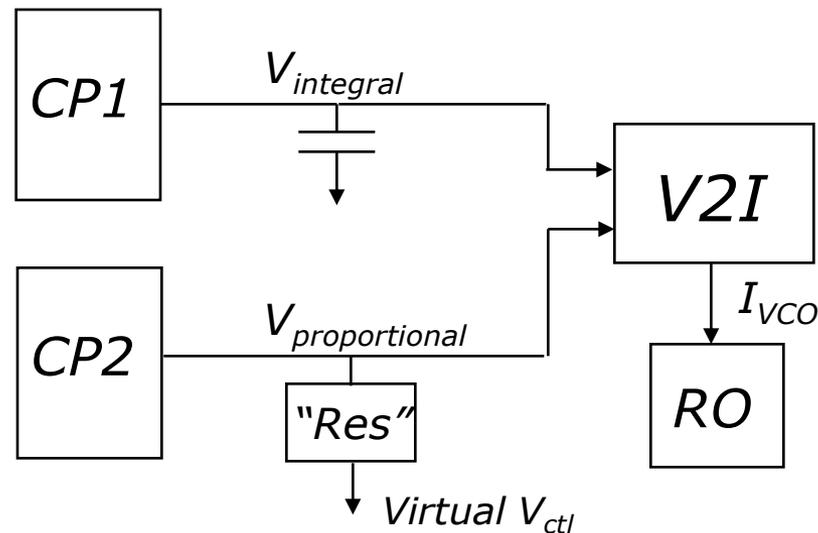
- Reference capacitor to same supply as VCO V-to-I reference → makes power supply noise common mode
- Gate Leakage in MOSFET caps can be a HUGE problem
 - Exponential I_{leak} vs. V : $I_{\text{leak}} \sim V_{\text{gate}}^4$ (approximate)
 - Weak temperature dependence
 - I_{leak} vs. $t_{\text{ox}} \rightarrow \sim 2\text{-}3\times$ per Angström
 - Use metal caps (2-10X larger) or thick-gate (IO) oxide caps to minimize leakage
 - If MOSFET caps, *accumulation* mode preferred – flatter C_{gate} vs. V
- I_{leak} causes large refclk spurs (jitter) and static phase error
- Typical values:
 - $5\text{pF} < C_1 < 200\text{ pF}$
 - $1\% \text{ (low phase error)} < C_2/C_1 < 10\% \text{ (low period jitter)}$
 - Smaller C_1 caps are becoming more common w/ higher reference frequencies and metal cap usage

Depletion-Mode MOSFET C_{gate} vs. V



Feed-Forward Zero: eliminate R

- Resistor in classic LPF provides an instantaneous IR on the control voltage causing the VCO V2I to generate a current bump on the oscillator input
- Alternative: eliminate R → Add parallel CP path into V2I.
 - requires parasitic cap (C_2 *not shown*) to the proportional loop to reduce reference spurs
 - see Maneatis '96 for continuous time or '03 for sampled loop filter
- Reduces LPF phase noise? Commonly used in low phase-noise I/O apps.

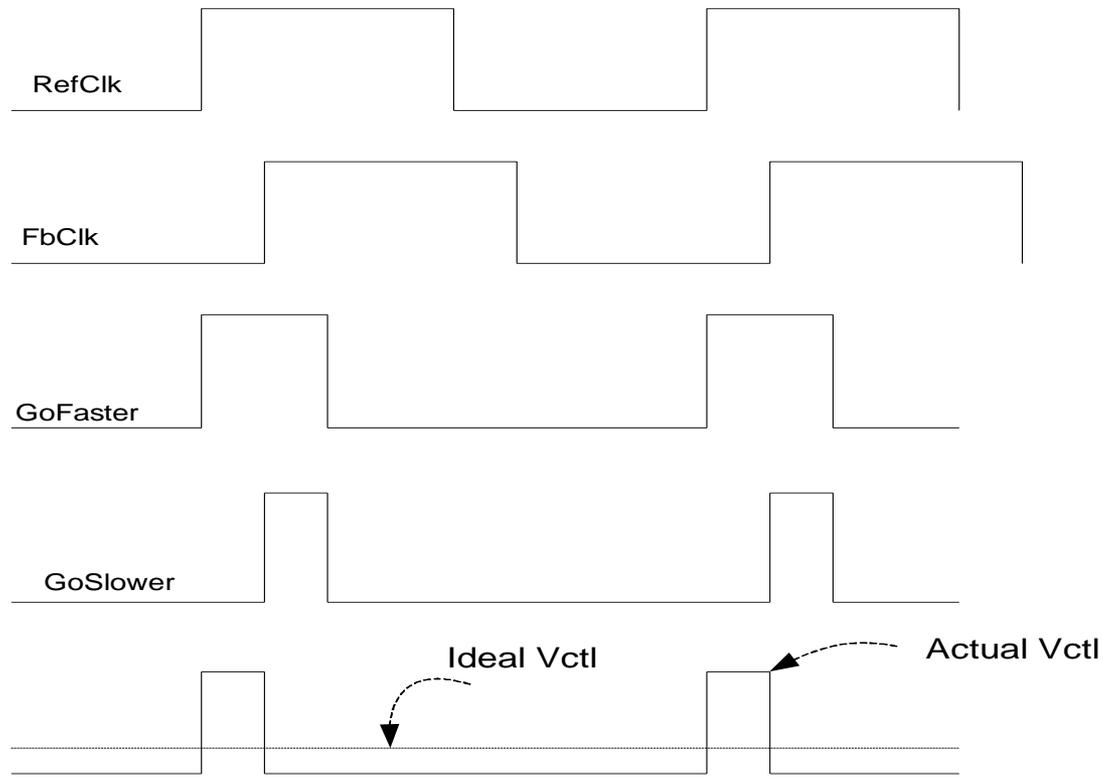


Dual-Loop Charge-Pump Mismatch

- I_{up}/I_{down} ratios in proportional and integral charge-pumps are partly uncorrelated due to random device mismatch
- Net charge from integral CP must integrate to zero for stable frequency – determines static phase error alone
- Net charge from proportional CP causes frequency kick every PFD cycle ($K_{vco} * I * R$) caused by static error and its own I_{up}/I_{down} mismatch
- Upshot: control voltage adjusts up or down from ideal level to achieve correct average frequency but f_{VCO} varies within PFD cycle (phase wander)– need well-matched CP's to avoid this effect

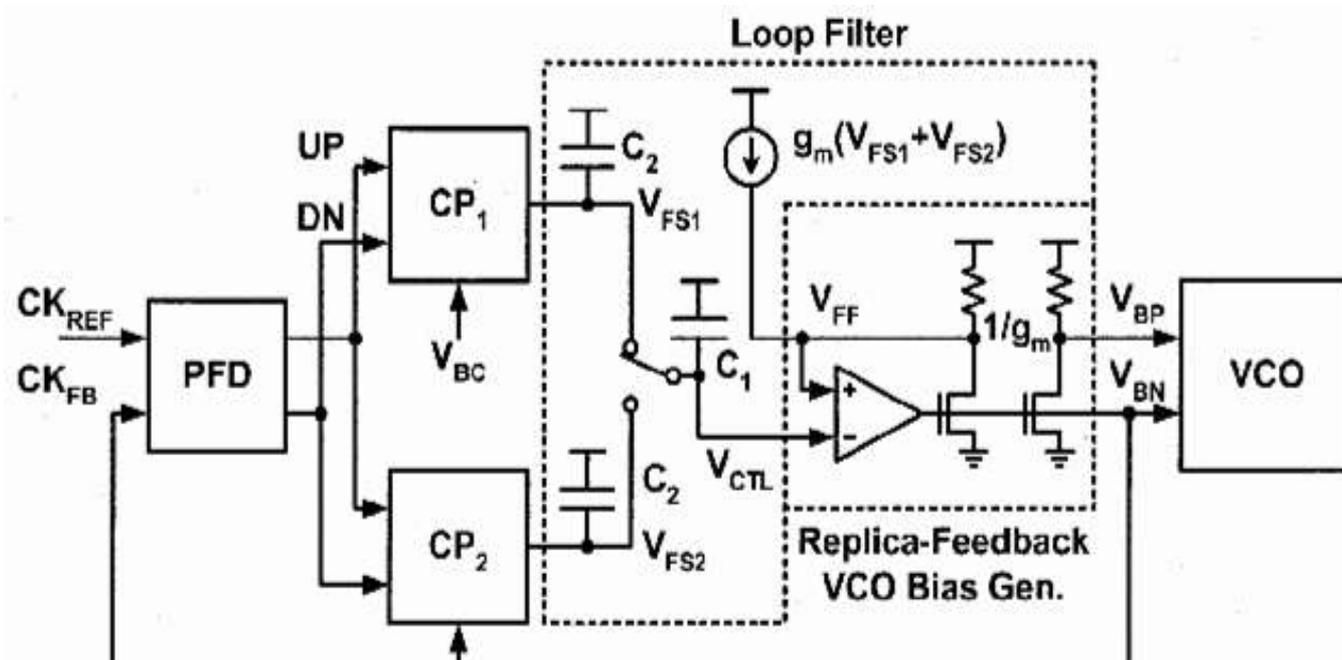
Dual-Loop Charge-Pump Mismatch

- Static error in integral charge-pump \rightarrow period jitter and phase wander

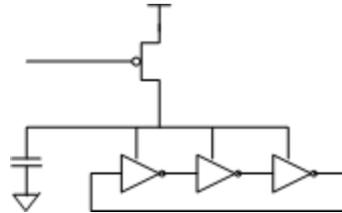


Sample-Reset Loop Filters

- Single charge-pump for I_{int} and I_{prop} – Zero $\sim \sqrt{C1/C2}$
 - e.g. Maneatis (JSSC '03)
- Two charge-pumps to allow for reset (discharge) delay
- Spreads phase correction over T_{ref} – can reduce ref spurs
- Mismatch between CP's \rightarrow significant VCO phase modulation at $f_{\text{ref}}/2$



Voltage-Controlled Oscillator (VCO)

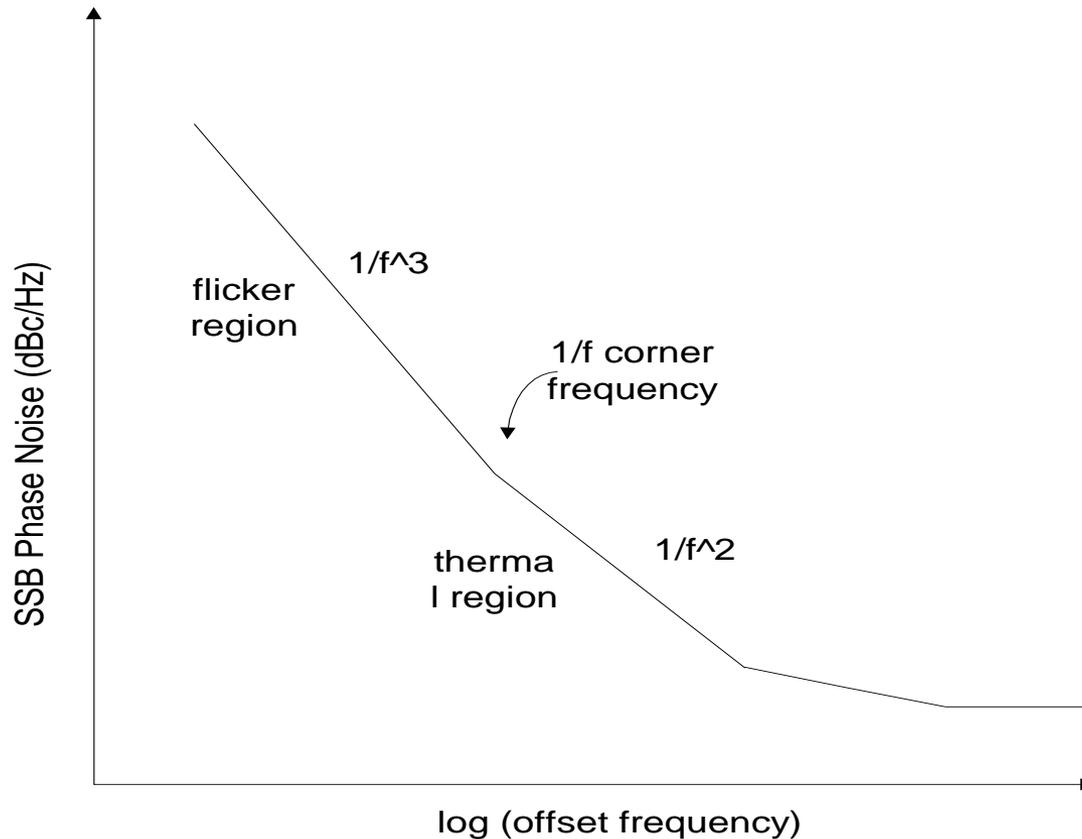


Voltage-Controlled Oscillator

- Ring-oscillator (RO)
 - Wide frequency range
 - Easy to design, integrate, and model
 - Easy to generate multi-phase outputs
 - Small area but high power for low jitter
 - Low Q – higher jitter
- LC-tank
 - Narrow frequency range
 - Need field-solver tools to model inductor and accurate varactor model
 - Hard to generate multi-phase outputs
 - Large area but low power
 - High Q – lower jitter

Single-Sideband Phase Noise Plot

- Open-loop VCO



Open-Loop VCO Phase Noise

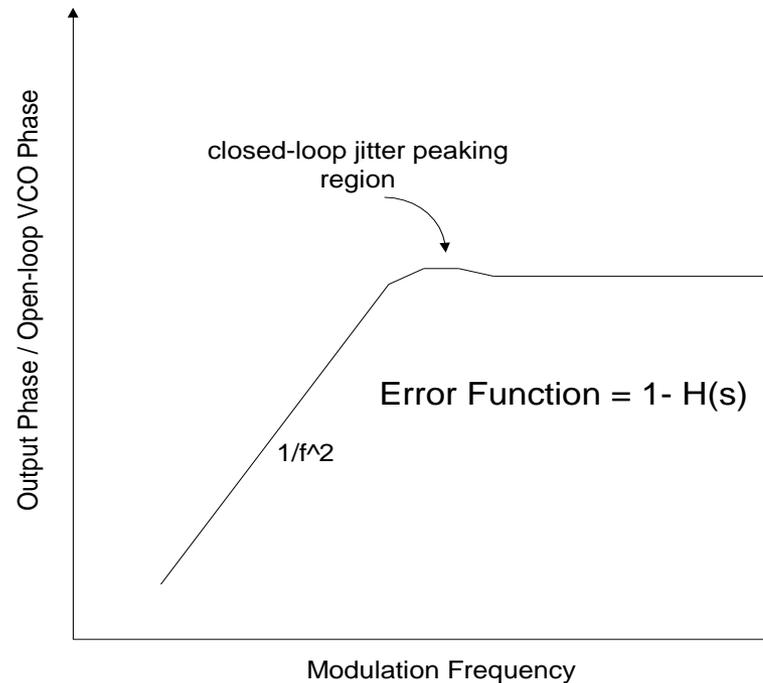
- Measured vs. offset frequency (f) from carrier
- Spectral Density of Phase Fluctuations ($S_{\phi}(f)$)
 - $S_{\phi}(f) = 2L(f)$
 - $L(f)$ is Single-Sideband Phase Noise (dBc/Hz)
 - Analogous to Power(sideband)/Power(carrier)
- $S_{\phi}(f) \sim 1 / f^2$
 - thermal region, mid-to-high freq
- $S_{\phi}(f) \sim 1 / f^3$
 - flicker region, low freq
 - Flicker noise mostly filtered by high BW PLL

VCO Phase Noise - Leeson

- $L(f) = 10 \log (FkT/A) * (1/8Q_L^2) * (f_{osc}/f)^2]$
 - F is the device noise factor at operating power level A
 - k is Boltzmann's constant, $1.38e^{-23}$ J/K
 - T is temperature (K)
 - A is oscillator output power (W)
 - Q_L is loaded Q (dimensionless)
 - f_{osc} is the oscillator carrier frequency
 - f is the frequency offset from the carrier
- Valid:
 - For offsets greater than the 1/f flicker corner frequency
 - the noise factor at the operating power level is known
 - the device operation is linear
 - Q includes the effects of component losses, device loading and buffer loading
- Source: Analog Devices: AnalogDialogue

Open-loop → Closed-Loop Phase Noise

- Goal: determine how much open-loop VCO phase noise remains after applying PLL feedback loop
- Method: multiply VCO's open-loop single-sideband phase noise by square of PLL's "error function" $\langle 1 - H(s) \rangle$ where $H(s)$ is closed-loop transfer function



VCO Noise Tracking: Phase Error vs. Bandwidth

- For random VCO noise (i.e. thermal):
- lower BW → more accumulated phase error
- Why? More jittery VCO cycles before feedback loop can correct:

$$\phi_{error} \propto J_{RMS,period} \cdot \sqrt{\frac{\omega_{vco}}{\zeta\omega_n}}$$

where J_{rms} = open-loop VCO RMS period jitter

PLL Suppression of VCO Noise

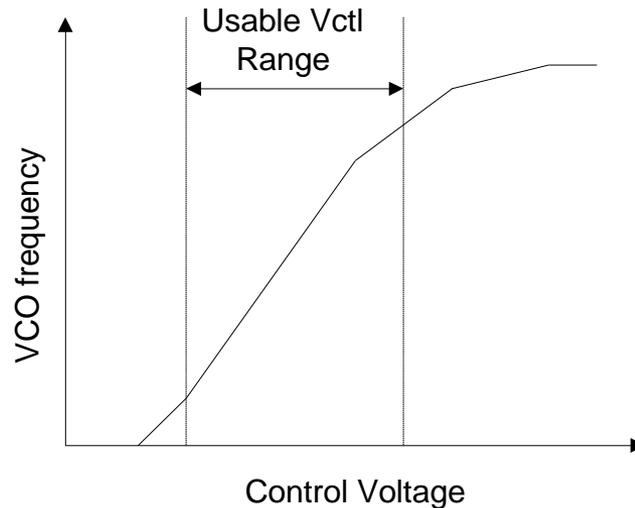
- PLL acts like a high-pass filter in allowing VCO noise to reach output
- Need noise-immune and low-intrinsic noise VCO to minimize jitter
 - Feedback loop cannot react quickly.
 - Tradeoff between tuning range & noise sensitivity
- Power-supply noise is usually largest source of VCO deterministic jitter(DJ) if no voltage regulator. Otherwise, largest jitter source is device noise (RJ).
- VCO power-supply sensitivity should be at least 10-20× less than inverter

PLL Suppression of VCO Noise

- For RO: high power, fast edges, large swing → lower device noise and lower random jitter (RJ)
 - J_{rms} (open-loop period) $\sim \sqrt{kT/2NC} / (f_{\text{vco}} * V_{\text{swing}})$
 - where $N = \#$ of stages, $C = \text{cap/stage}$
- Match rise/fall times, inter-stage delays to minimize phase noise (lowers ISF)
- RMS random jitter (kT) < 0.02% - 0.2% VCO period (typical)

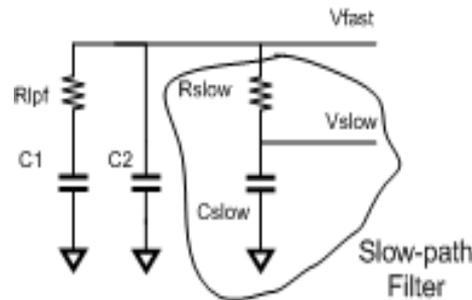
RO VCO Gain

- Typical VCO gain: $K_{VCO} \sim 1-3 \times * f_{max}$. May vary w/PVT by $> 2 \times$
 - need frequency range: $> 2 \times$ to allow for PVT
 - desire constant gain over most of usable control voltage range
 - use digital calibration to reduce : K_{VCO} variation



Achieving Low RO VCO Gain

- Goal: low gain and wide frequency range → allows for low PLL BW and/or can help filter charge-pump and resistor noise
- Make VCO frequency a function of TWO control paths
 - Fast-path: low K_{vco} – connect to normal loop filter path
 - Slow-path: high K_{vco} – connect to secondary control path with low BW ($\ll 1/10$ PLL BW) – requires stable refclk frequency
- Loop dynamics are determined mostly by fast-path – model in $H(s)$
- Slow-path RC filter added to normal loop filter
 - Can connect R_{slow} to C_1 cap instead of C_2 cap.
 - Add unity-gain buffer if V_{slow} leakage is high
 - Increases lock time w/o additional logic and switches
 - Techniques to reduce lock-time can cause instability

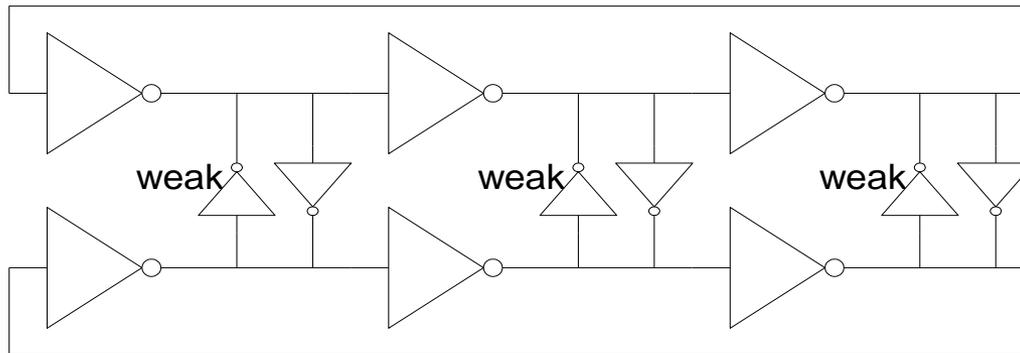
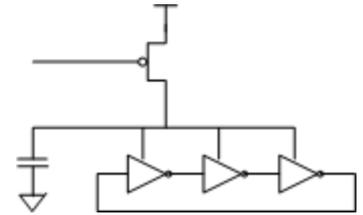


Voltage-Controlled Oscillator

- Barkhausen criteria for sustained oscillation
 - loop gain must exceed 1, loop phase must equal 360°
 - more RO delay stages \rightarrow easier to initiate oscillation
 - gain(DC) > 2 for 3 stages, gain $> \sqrt{2}$ for 4 stages

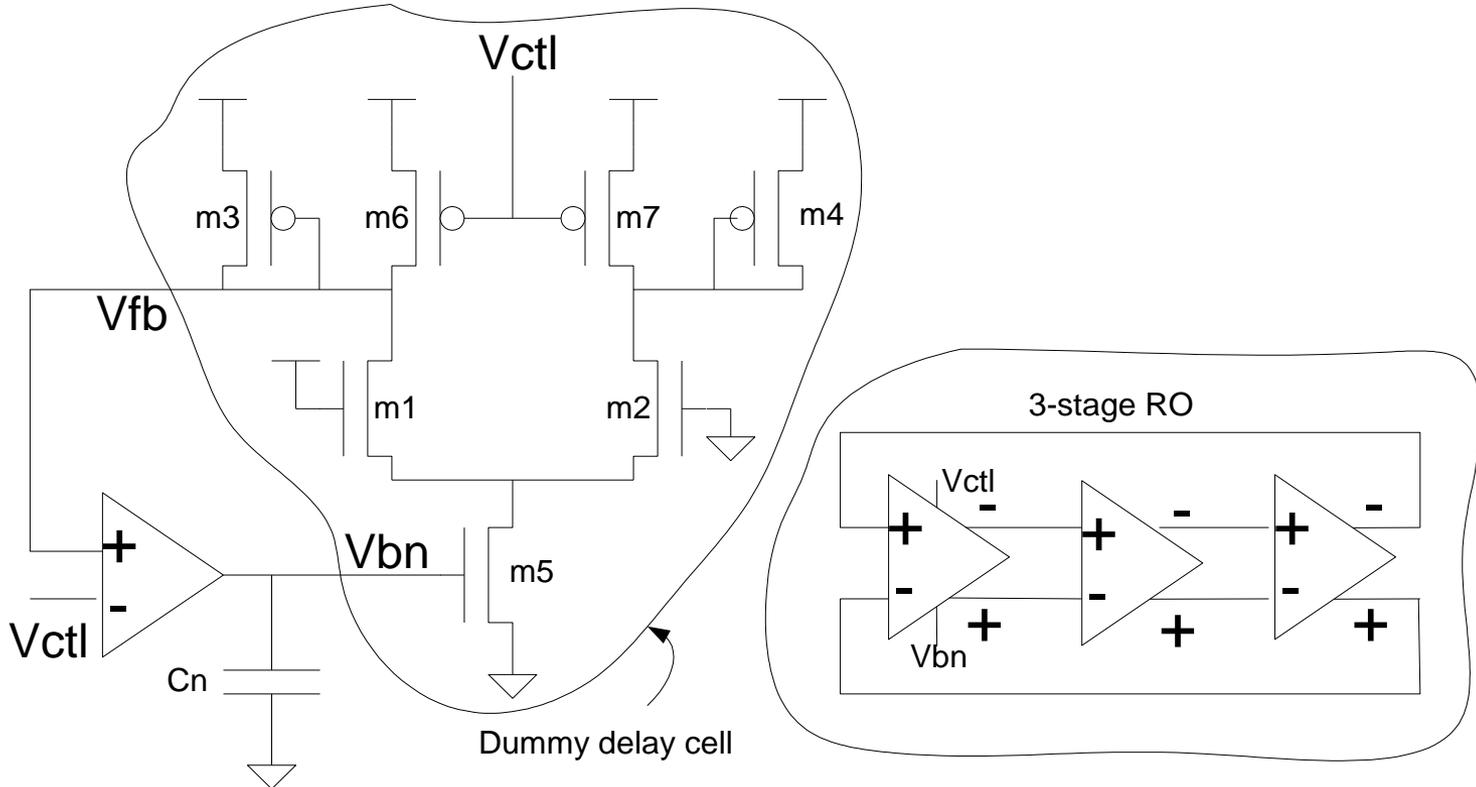
VCO w/current-starved inverters(CSI)

- RO VCO usually consists of two circuits
 - bias generator (e.g. V_{ctl} to I_{ctl})
 - voltage or current controlled ring oscillator (RO)
- Usually odd # of stages (usually 5+). Even # ok if differential RO
- Feedback INV \rightarrow usually weaker by $> \sim 3-4\times$
- Tune frequency by adjusting "VDD" of inverters – changes delay
- "Vdd" for inverters is regulated output of VCO V2I



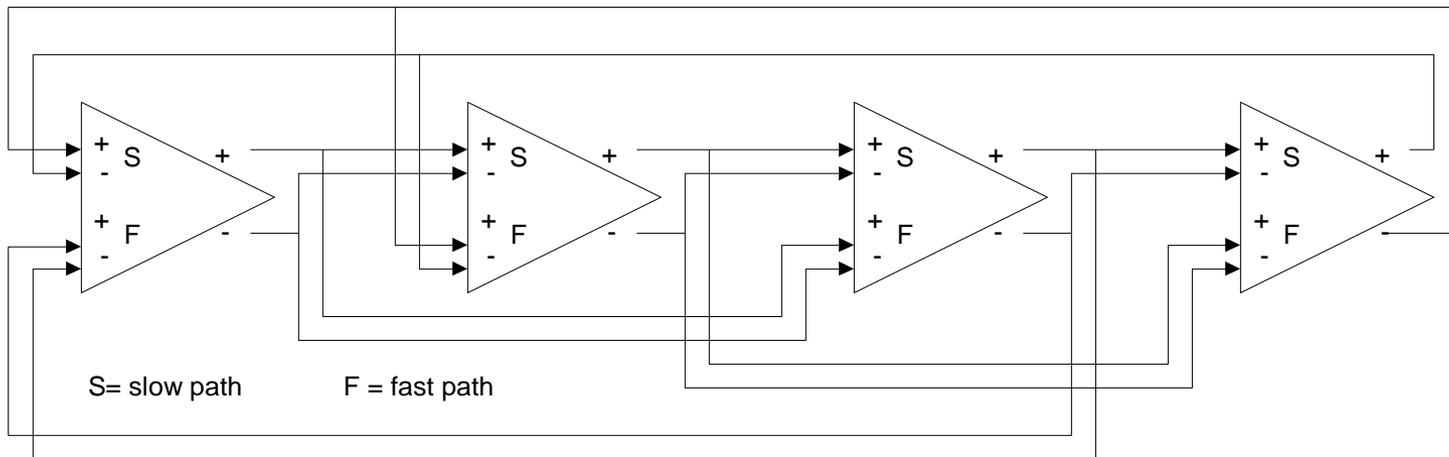
Diff-Amp VCO w/Replica-Bias V2I

- $V_{\text{swing}} = V_{\text{ctl}}$ (Maneatis '96)
- Amp provides DC power-supply rejection
- Stable, but getting high BW and good PSRR tricky
- Start-up necessary



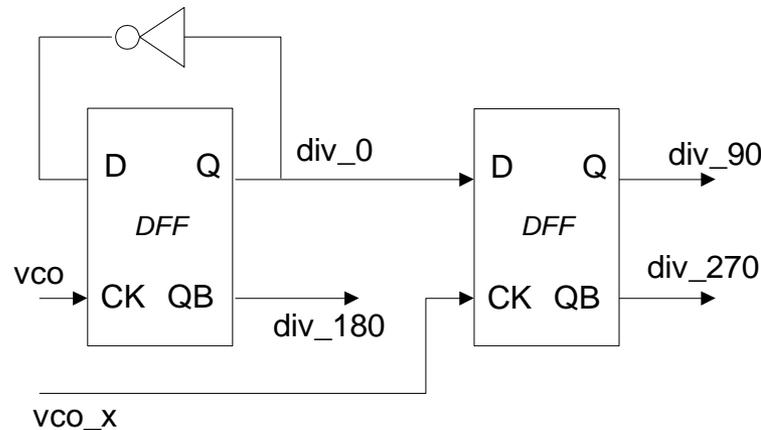
VCO w/Feed-Forward Path

- RO delay stage may receive inputs from multiple prior stages (e.g. N-1 and N-2)
 - allows N-stage VCO to oscillate at speeds otherwise attainable only by reducing # of stages
 - easier to implement with differential signals
 - extra care must be taken to ensure that RO will safely oscillate



Quadrature Output Clocks

- Quadrature clocks (0°, 90°, 180°, 270°)
 - requires 4 delay stages or
 - divide “differential” VCO outputs by 2, then delay one set of divided outputs by $\frac{1}{2} T_{VCO}$ to generate quadratures. Allows any # of delay stages

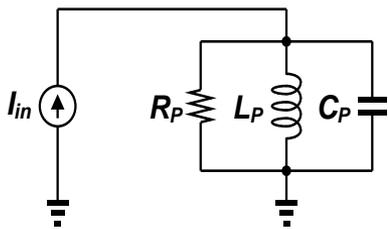
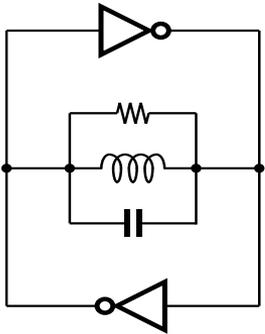


LC VCO

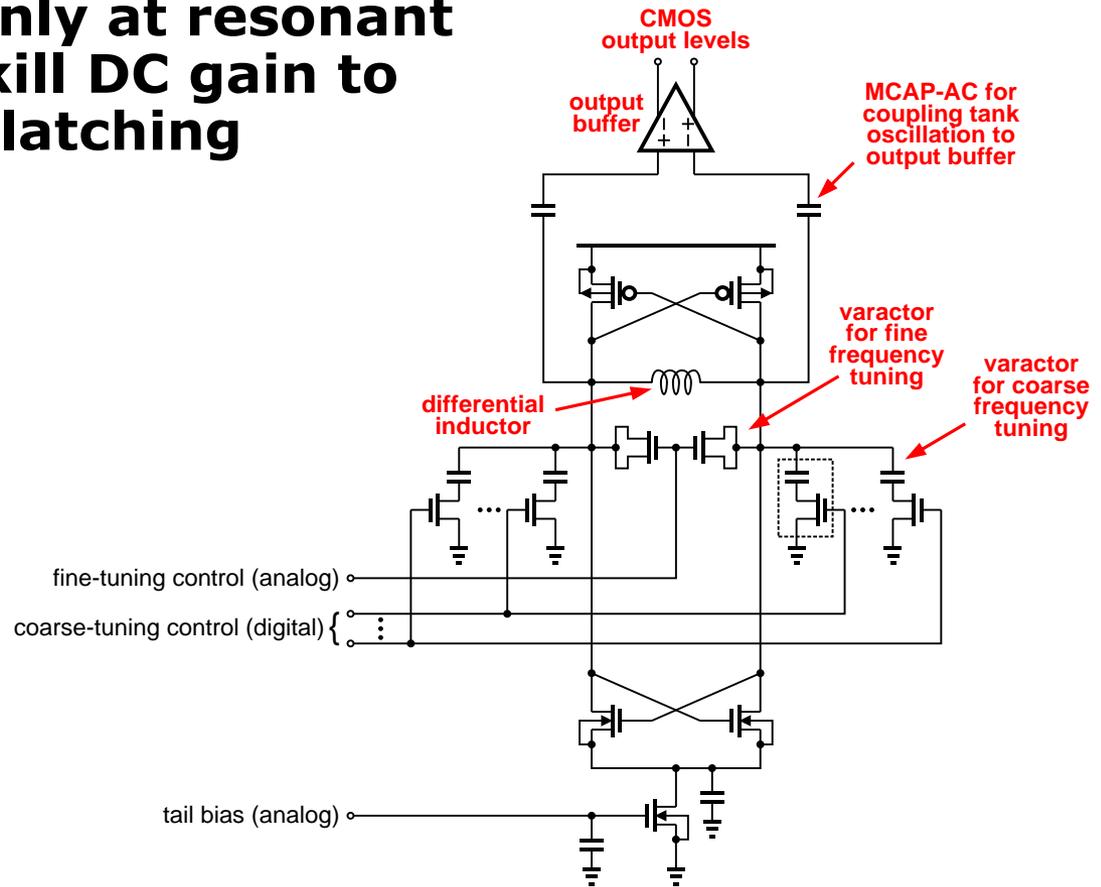
- Pros
 - Low jitter / phase noise performance
 - If L & C are modeled correctly, frequency prediction is good
- Cons
 - Limited tuning range
 - Area (inductor)
 - Inductor is not supported at many companies
 - Accurate varactor model is challenging
- Key design considerations
 - Keeping noise sources quiet
 - Varactor choices
 - Tuning range vs. noise performance
 - Oscillation amplitude control

LC VCO Schematic

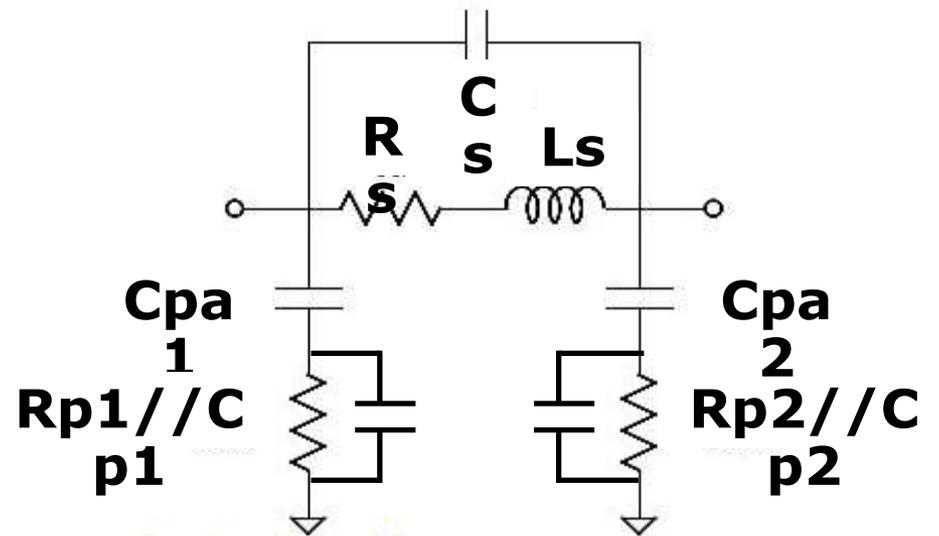
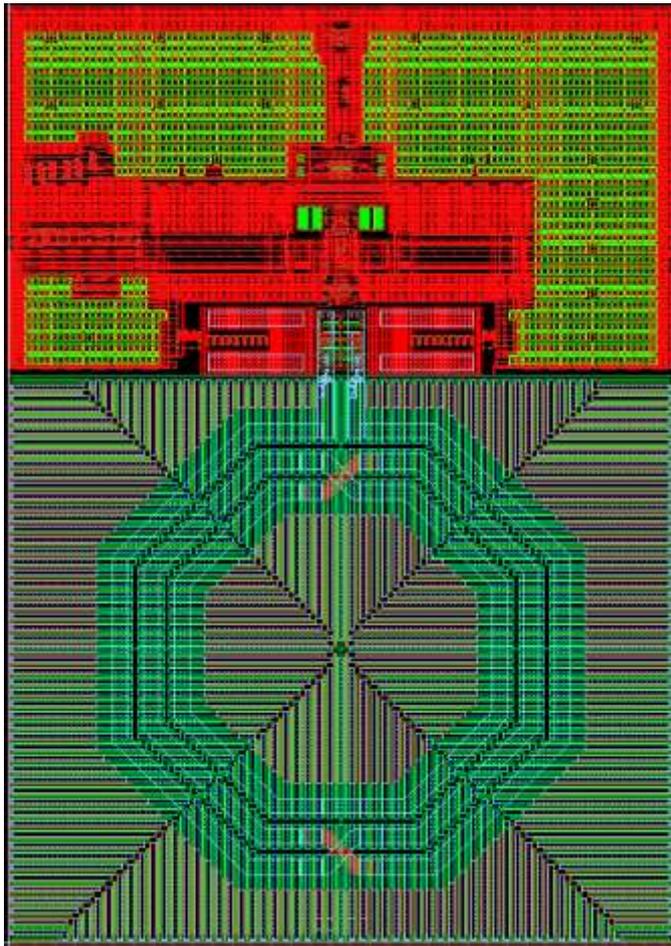
Two back-to-back inverting stages with LC filtering to amplify noise only at resonant frequency & kill DC gain to prevent latching



$$\omega_P = \frac{1}{\sqrt{L_P C_P}}$$



LC VCO



LC VCO Design Concerns

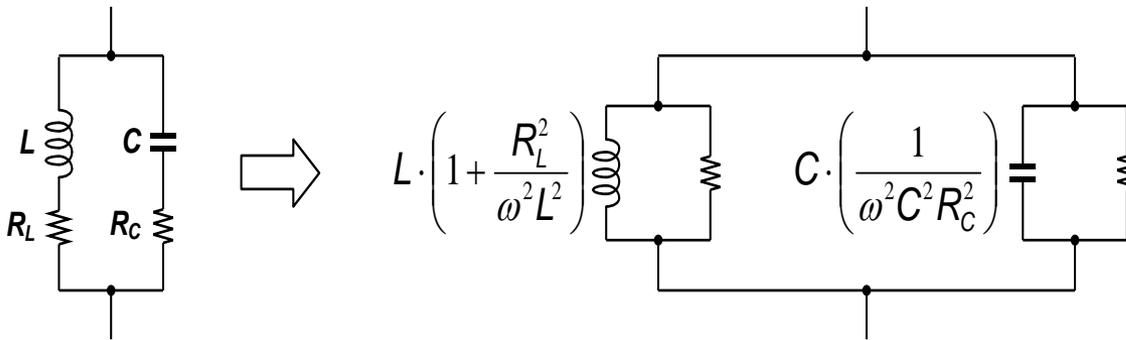
- Thermal noise of parasitics tuning L & C parasitics
- Device noise of cross-coupled $-gm$ devices (mostly thermal noise)
- $1/f$ noise of tail (upconverted to fundamental via mixer action)
- L needs to add dummy fingers to pass metal density rules
- Fingers oriented orthogonally to inductor turns to minimize parasitic eddy currents from magnetic coupling
- Fingers staggered between M_n & M_{n+1} to reduce CMP topography
- Need symmetry in inductor underpass connections
- Need to account for high-frequency effects (proximity/skin effects, dielectric loss, etc.) in inductor

Setting LC VCO Tailbias

- Tail biasing sets oscillator current
- Need enough current to create enough g_m in cross-coupled devices to overcome resistive losses in tank in order to start up initial oscillation and sustain oscillation
- Can set with static control or local amplitude-control loop
- Ramp *tailbias* down, i.e., slowly kill oscillator gain & check when oscillations die out (defined when peak swing falls below 0.1V)

LC VCO Temperature Effects

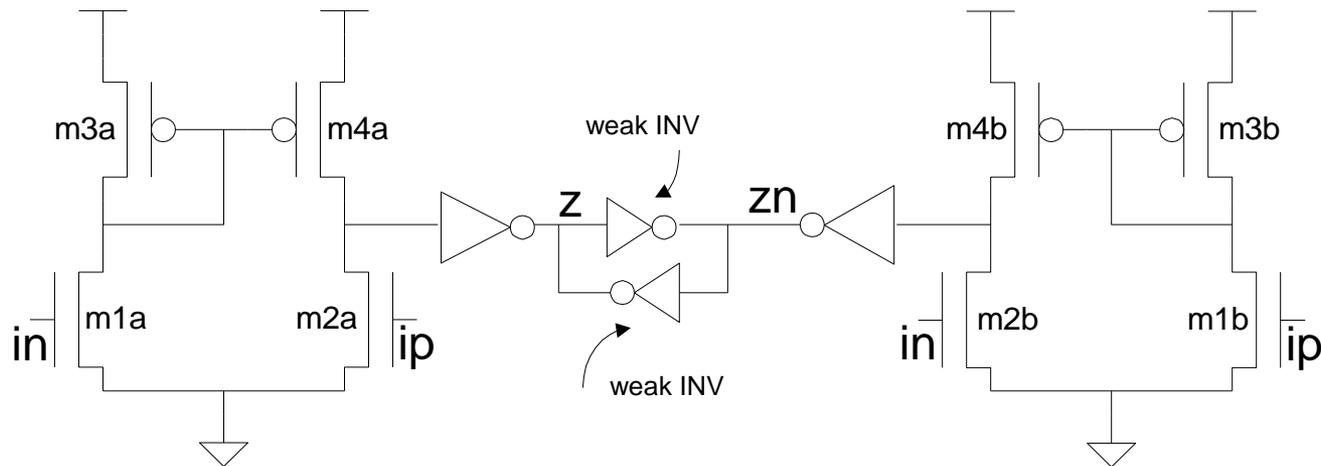
Metal TCR affects oscillation frequency when inductor Q is limited



$$\omega_{res} = \frac{1}{\sqrt{LC}} \cdot \sqrt{\frac{1 - \frac{C}{L} R_L^2}{1 - \frac{C}{L} R_C^2}} \neq \frac{1}{\sqrt{LC}}$$

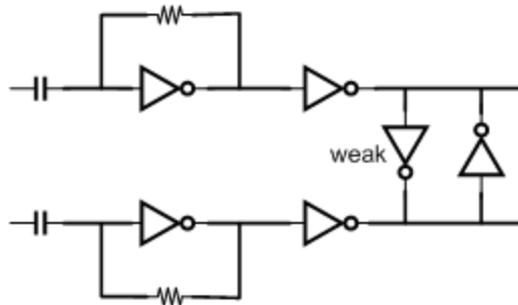
VCO Level-Shifter

- Differential-pair without tail current
- Need sufficient gain at low VCO frequency – use low- V_t NMOS
- Use NMOS input pair if VCO swing referenced to VSS for better power-supply rejection – often low V_t for wider input range
- For best duty-cycle, use two instances of level-shifter (swap inputs), and couple complementary outputs with weak inverters
- Typical duty cycle: $50 \pm 3\%$ with random mismatch



AC-Coupled VCO Level-Shifter

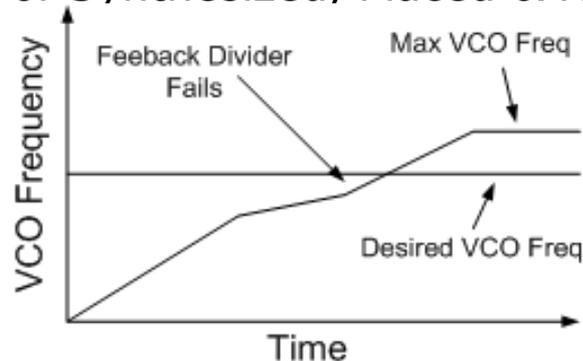
- Can't pass low-frequency clock due to AC-coupling
- Caps decouple VCO common-mode from level-shifter input common-mode
- Large resistors bias input inverters at trip-point w/o attenuating gain
- Parasitic capacitance at input of first inverters attenuates AC signal
- Typical duty cycle: $50 \pm 3\%$ with random mismatch



Feedback Divider

Feedback Divider (FBDIV)

- Typical Implementation: programmable, synchronous digital counter
- Max FBDIV frequency should be greater than max VCO frequency to avoid “run-away” - beware of Synthesized, Placed & Routed designs



- Counter output may glitch → re-sample with VCO output to clean up glitch, reduce latency and phase noise
- Loop Phase Margin Degradation $\sim \omega_c * T_{fbdiv}$
 - usually insignificant (a few degrees)
- Divider may be internal to PLL or after clock tree to cancel clock tree skew
- May provide additional output signals used to deterministically synchronize tester controls to VCO clock and/or walk signals between various on-chip clock domains

Fractional-N Dividers

- Divide VCO clock by non-integer value to allow for finer frequency resolution
- Dual modulus: $N, N+1$
 - Vary divisor from N to $N+1$ at various rates, duty-cycles to achieve intermediate value
 - Requires delta-sigma modulation to reduce/re-shape noise spurs (move to higher frequency)
 - PLL feedback loop filters high-frequency spurs
- Complementary Approach: multi-phase VCO outputs
 - e.g. 8 or 10 output phases
 - Feedback clock period can be adjusted by less than one VCO clock
 - More power, lower f_{max} for multi-phase VCO

Voltage Regulator

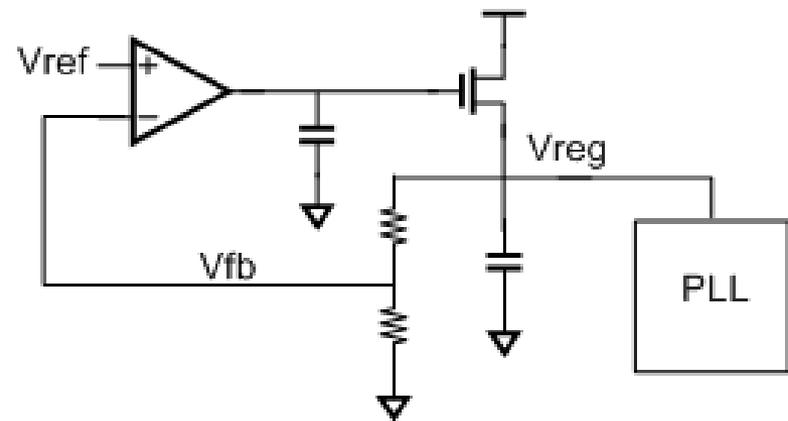
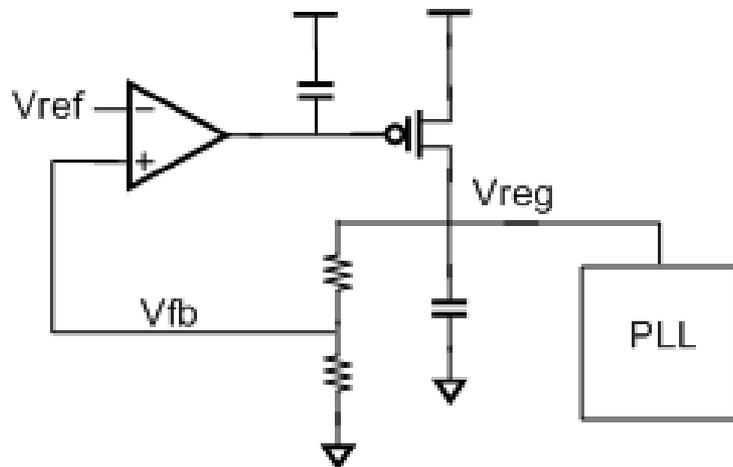
- Provides stable, PVT-insensitive, clean power-supply for PLL
 - lower jitter, phase noise
 - more stable loop dynamics, VCO range, etc.
 - aim for $> 30\text{dB}$ PSRR, definitely $> 20\text{dB}$
- Uses bandgap reference to set voltage and bias current levels
- Two voltage regulators sometimes used
 - High VDD for charge-pump (analog) and lower VDD for VCO
 - “Quiet” for analog (CP, VCO bias) and “Dirty” for digital (PFD, FBDIV)

Voltage Regulator

- Requires higher power-supply (e.g., 1.8V \rightarrow 1.2V)
- Wastes current
 - higher VDDA and bandgap/regulator over-head (0.5-3mA).
 - aim for current overhead $< 20\%$. $< 5\%$ is achievable in some apps
- Regulator area (inc. bandgap) is small compared to decoupling cap area
 - Area (MOSFETs, Rpoly, diodes) $\sim 70 \times 70 \mu\text{m}^2$ (65nm)
 - Area (DECAPs) $\sim 125\mu\text{m} \times 125\mu\text{m}$ for 100pF (65nm)
 - Typical cap $\sim 30\text{-}300\text{pF}$
- V_t -mismatch in bandgap amplifier input pair dominates overall regulator mismatch
 - 3mV offset at amp $\rightarrow \sim 20\text{mV}$ variation at output
 - Goal $< 25\text{mV}$ 1- σ variation from device mismatch
 - Goal $< \pm 5\text{mV}$ PVT variation (due mostly to diodes)

Voltage Regulator

- Hard to stabilize over wide Iload and Cload ranges
- NMOS source-follower output stage
 - Requires more headroom
 - Faster response and easier to stabilize
- PMOS common-source output stage
 - Can handle larger current loads \rightarrow larger V_{gs}



Digital PLL's

What is a Digital PLL?

- Replace charge-pump (time error-to-charge) with TimeError-to-Digital Converter
- Replace loop filter with discrete-time digital filter (usually 2nd or 3rd order sigma-delta)
- Replace voltage-controlled VCO with digital-control (vary cap load, interpolation, etc.)
- Are analog components “allowed”? Voltage regulator? Analog current-steering DAC for VCO?
- Sampled-system modeled in the Z-domain

Why a Digital PLL?

- Replaces process and noise-sensitive analog circuits with digital equivalents – advances on work with digital DLL's
- Increases PLL design portability and testability
- Takes advantage of area scaling with nm devices
- Greater flexibility in loop bandwidth – don't need huge capacitors for low BW
- Increases ability to test and observe. e.g. open-loop, disturb loop
- Fast behavioral simulation
- "Good-enough" for frequency synthesis applications
- ISSCC presentations: TI('04) and IBM ('07)

Why NOT a Digital PLL?

- Often not “good enough” for phase-tracking applications
- VCO frequency has finite frequency resolution (e.g. 10-14 bits). May use coarse DAC if high-frequency dithering available
- VCO has limited range – requires range control and/or calibration
- VCO may have poor noise rejection if purely digital frequency control and no voltage regulator (usually analog)

Why NOT a Digital PLL?

- Need high-frequency over-sampling clock for sigma-delta loop filter – VCO? Refclk? Start-up problem?
- TimeError-to-Digital Converter is hard – poor resolution, high power – usually < 5 bits
 - Bang-bang is an alternative (IBM)
 - FbDiv internal state contains phase error information
- Digital filter generates large noise spurs, possibly inducing jitter, and dissipates more power than passive loop filter
 - Requires delta-sigma modulation to reduce spurs
- Generating proportional correction can be tricky

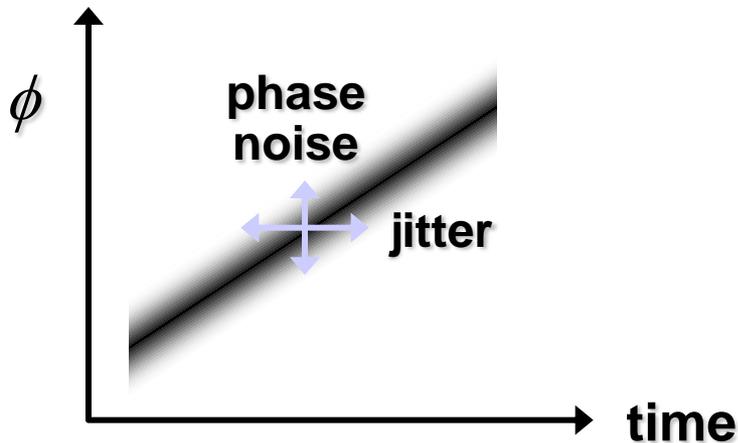
Phase Noise to Jitter

Phase Noise and Timing Jitter

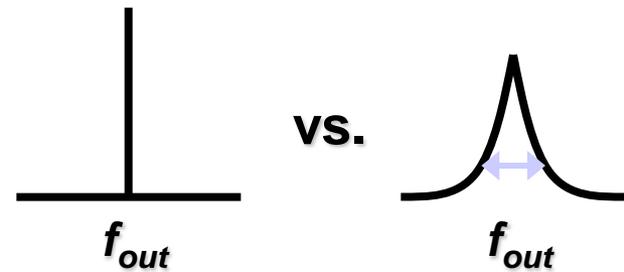
- **Phase Noise (frequency domain) ↔ Jitter (time domain)**
- **Noise is frequency-dependent with random & deterministic components**
- **VCO and loop filter resistor often largest sources of noise**

PLL Output

$$V_{out}(t) \propto \sin(2\pi f_{out} t + \phi_n(t))$$



Frequency Domain

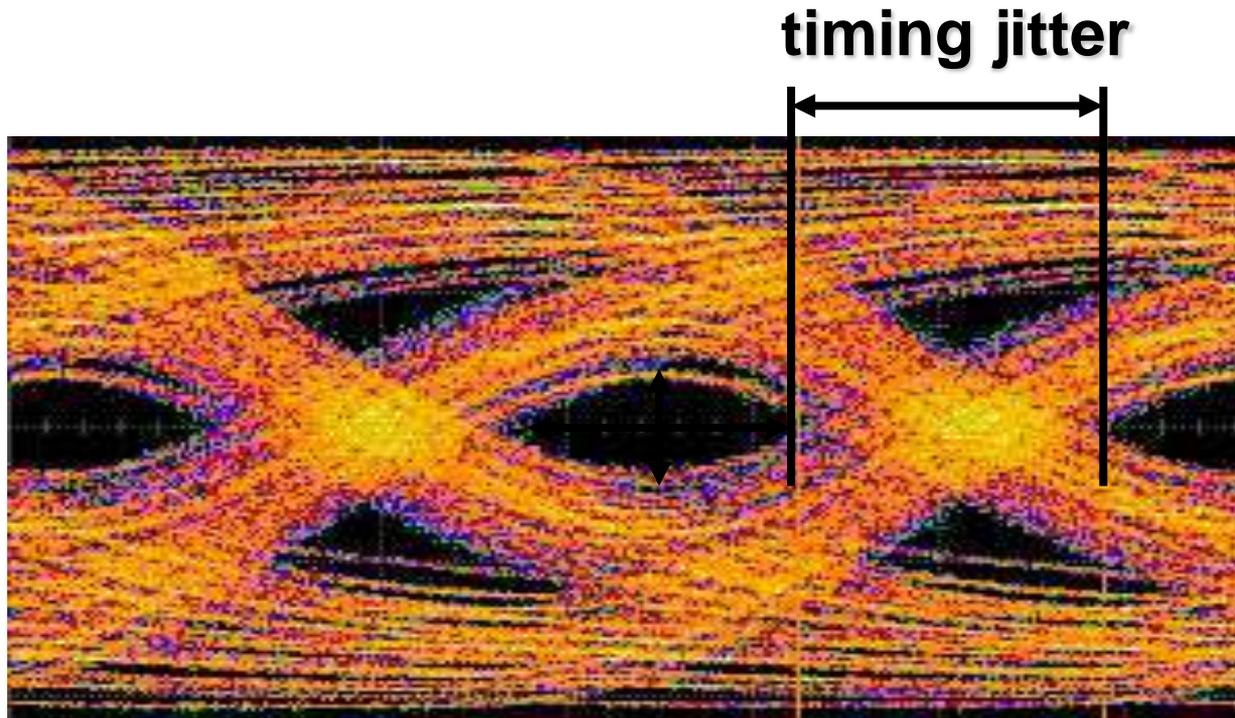


Time Domain



Timing Jitter: Eye Diagram

- Example of timing jitter in serial link.
- Overlay scope traces of several bits on top of each other



Jitter Definitions

- Phase Jitter (sec)
 - **deviation of VCO output edges from ideal placement in time.**
 - specified over a time interval or frequency range.
 - important for I/O apps (e.g. PCI-Express < ± 1.5 ps RMS)
 - measure with spectrum analyzer or scope with jitter package
- Period Jitter (sec)
 - **deviation of VCO period from ideal period**
 - **derivative of Phase Jitter with respect to time**
 - peak-to-peak period jitter (J_{pp}) is max VCO period – min VCO period
 - most important for CPU-like apps
 - e.g. 10-20ps for 2GHz CPU clock
 - easily measured on scope – self-triggered infinite-persistence or jitter package
- Cycle-to-Cycle Jitter (sec)
 - change in VCO period from cycle N to cycle N+1
 - **derivative of Period Jitter with respect to time**
 - not important for CPU-like apps

Jitter Definitions

- TIE (sec)
 - time difference between total of N-consecutive actual VCO cycles and N ideal cycles
 - easily measured on oscilloscope with jitter package – self-triggered measurement
 - TIE – “time-interval error”

Noise Sources

- Major internal PLL Noise Sources
 - VCO oscillator (mostly thermal) – very significant
 - VCO bias (flicker and thermal) – very significant
 - Loop filter resistor (thermal)
 - Charge-pump (flicker (1/f) and thermal)
 - Flicker Noise
 - V_n^2 (V²/Hz) = $K_f / (C_{ox} * W * L * f)$
 - $K_f \sim 10e^{-24}$ – PMOS often lower than NMOS
 - Thermal Noise
 - I_n^2 (Amp²/Hz) = $4kT * g_m * \gamma$
 - $\gamma \sim 2/3$ for older CMOS technologies, much higher in deep submicron
- PLL feedback loop
 - Low-pass filters ref and charge-pump noise
 - Band-pass filters loop-filter resistor noise
 - High-pass filters VCO noise (1-H(s))

Converting Phase Noise to Jitter

- RMS Phase Jitter

$$J_{phase} = \frac{1}{2\pi f_{vco}} \sqrt{\int S_{\phi}(f) df}$$

- $S(f) \rightarrow 2 * L(f)$ where $L(f)$ is single-sideband phase noise
 - To convert to dBc/Hz, use $10\log_{10}(L(f))$
- Easily measured using spectrum analyzer – low noise floor
- Ideal reference is measurement trigger
- Integration range depends on application (e.g. PCIe: $f_{min} = 1.5\text{MHz}$)
 - usually stop integration at $f_0/2$ to avoid capturing carrier and harmonics
 - e.g., 5ps from 1MHz to $f_0/2$ with BW=15MHz and 2.5GHz clock (SOI bad for phase jitter)

Converting Phase Noise to Jitter

- RMS Period Jitter

$$J_{period} = \frac{1}{2\pi f_{vco}} \sqrt{8 \int L(f) \sin^2\left(\frac{\pi f}{f_{vco}}\right) df}$$

- Spectrum analyzer can't do this integral. Post-process phase noise
 - e.g., $J_{per} \sim 300\text{fs}$ w/2.5GHz clock
- Usually dominated by VCO bias and VCO?
- Spectrum analyzer usually has lower noise floor than scope (scope floor $\sim 800\text{fs}$ @ 40Gsample/sec)

Converting Phase Noise to TIE

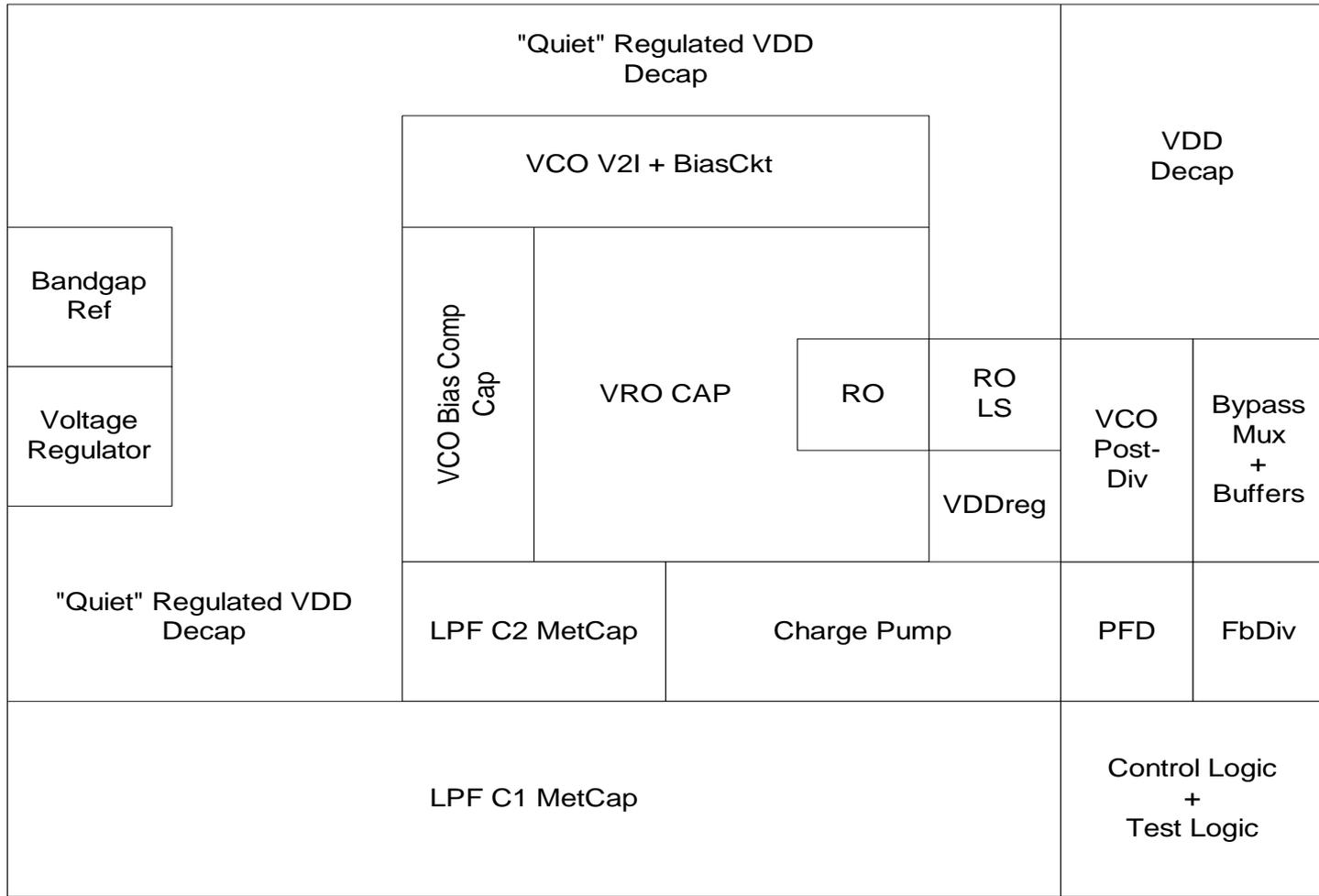
- Time-Interval Error (TIE)

$$J_{TIE} = \frac{1}{2\pi f_{vco}} \sqrt{8 \int L(f) \sin^2(\pi f \tau) df}$$

- “*Tau*” is time interval over which phase drift is measured
- Spectrum analyzer can’t do this integral. Post-process phase noise
- $J_{TIE}(Tau) = \text{sqrt}(2) * J_{\text{phase}}$ where $Tau = 1/f_{\text{start}}$ and f_{start} is the starting frequency for both integrations

Circuit Verification

PLL Floorplan



Noise Isolation

- Check extracted netlist for coupling of switching signals onto sensitive analog signals (e.g. REFCLK \rightarrow V_{ctl})
- Check that LPF metal caps are present and well-connected to correct power supplies
- Check that VSS of LPF metal caps and VSS of VCO bias circuits are well-connected and at same potential
- Check that correct shields for sensitive signals are in place and well-tied to correct power supplies

Noise Isolation

- Account for parasitic capacitance to substrate in “NWELL” decaps, diodes, and well/diffusion resistors
- Add guard rings as applicable
- Buffer control signals and programmable inputs locally before use
 - avoids problem where VSS of control signal doesn't match local VSS where signal is used
 - filters coupling/glitches on long routes

Signal EM / ESD

- Inspect wires that conduct DC current and wires that drive large switching output loads for EM violations (e.g. charge-pump bias, output clocks)
- Check that signal ESD and/or power supply clamps are well-connected to power supplies ($< 1-2 \Omega$)
 - extract power grids and ESD
 - simulate for voltage peaks and diodes wired-backward

Power-Grid IR

- Aim for avg IR drops $< 5\text{mV}$ over entire PLL, less within and between related analog blocks
- Decoupling capacitors surround large, switching buffers to reduce IR drops and are well-connected to grid
- Check for isolated power domain islands
- Plan power domains and level-shifter placement up-front

Switching Signals

- Match differential signals – total capacitance and coupling (e.g. up, up_x, dn, dn_x, clk, clk_x)
 - try to match total capacitance < 1-2%
- Maintain fanout (incl. Wires) < ~6 on high-speed paths, < ~10 on DC paths (e.g. encode/decoders)
 - reduces crow-bar current and noise glitches
- Setup/Hold checks in PFD, Feedback Divider, and Post-VCO divider. Needs lots of margin for FBDIV to account for overshoot, aging, etc.
 - strive for FBDIV faster than VCO(max)

PLL Instantiation – Checks

- Mismatch on differential signals
- Coupling into refclk, output clocks
- Possible glitches on control inputs
- Signal routes over sensitive areas of PLL (VCO, loop filter, charge-pump)
- Large buffers on edge of PLL that may inject noise in substrate (keep-out requirement?)

PLL Instantiation – Checks

- Output wires wide enough to handle current load (EM)
- Rise/fall times on inputs/outputs – add maxcap limit into timing file to flag heavy loads - RC delays
- VDDA/test signal routes to bumps and/or ESD
- VDD/ VSS power supply connections

Functional Modes

- Power-Down/Reset/Test Modes
 - chicken-and-egg start-up problems – esp. level-shifters, bootstrapped regulators
 - Contention?
 - measure current in every device in these modes
- SLOW clock mode
 - drive slow output clock at power-on to remove contentious states in downstream logic
 - disable any clock gaters
 - mux in separate ring oscillator or force VCO/post-VCO div to produce low frequency clock in open-loop mode
 - avoid glitches when entering/leaving SLOW mode
- Frequency Hopping
 - Ensure that FBDIV can't fail during frequency transition if RESET not applied

Power/Clocking Domains

- Level-shifters are present when crossing power domains and are connected to correct supplies
 - apply writability analysis with mismatch
 - check for overstress
 - easy to miss
- Add synchronizers or “walk clocks” when crossing clock domains – easy to miss
- Check metastability on flops, comparators – is there a failure mechanism? Calculate MTBF.
- Insert bypass mode mux, preferably such that if the regulator fails, bypass clock still propagates to output

RTL vs. Circuit

- Add assertions to RTL model to flag illegal input states
- Verify that RTL and tester don't assume that dividers, etc. are initialized to known states upon power-on, frequency-changes, etc. – add logic to establish determinism if needed
- Model/verify all digital logic in RTL
- Specify expected input states at boundaries of all analog blocks in various operating modes
- Take special care with calibration algorithms outside PLL
- Simulate PLL exhaustively in VerilogA, Nanosim, etc, if possible

RTL vs. Circuit

- Look for incorrect polarity on input control signals (e.g., reset, powerDown) and REFCLK
- Look for glitches on feedback clock and other dividers
- Exercise all divider/counter states
- Check for possible VCO run-away conditions during power-on and frequency changes (e.g., no reset or feedback divider is halted)
- Verify that unselected inputs of muxes in critical signal paths are gated (e.g., VCO post-divider muxes)

Behavioral Simulations

- Behavioral simulation –before detailed circuit design define requirements for each block – e.g. PLLUS, Simulink
- Develop/verify jitter budget – e.g. PCI-Express
- Estimate VCO frequency overshoot
- Loop bandwidth vs. reference noise suppression
- Simulate effects of VCO gain variation, loop filter leakage, charge-pump mismatch, feedback delays, OSR, spread-spectrum tracking, Vctl-sensitive loop parameters, PFD dead-zone, parasitic poles

Circuit Simulations

- Start-up circuit safety margin - bandgap, VCO, regulators
- Stability of all internal feedback loops
 - AC and transient impulse response (ringing)
 - e.g., bandgap, regulator, charge-pump bias, VCO bias
 - Phase margin, gain margin, # of rings
- VCO - RO stage delays rise vs. fall, stage-to-stage – lower ISF
- Level-shifters' possible corruption of duty-cycle
- Switching-induced noise spikes on regulated power supplies
- Current dissipation in power

Circuit Simulations

- PSRR of voltage regulators, ability of regulators to meet fast-changing current load
- Step reference phase, observe PLL re-lock
 - overshoot, relock time
- Simulate entire sequence from power-on to lock
 - sanity check

Devices/Circuits

- Estimate effects of V_t mismatch BEFORE starting layout (monte carlo, $dV_t \sim 1/\sqrt{W*L}$)
 - most sensitive: bandgap, charge-pump, other low I ckts
- Estimate loop parameter variations, static error, reference spurs due to PVT and mismatch before starting layout
 - K_{vco} , I_{cp} , R , $C1$ (also vs. V_{ctl}) – esp. dual- charge-pump designs
 - circuit techniques to minimize effects: self-bias, $I_{cp}*R_{lpf}=\text{const}$
 - self-bias not as effective if not all devices the same L_{eff}
- Diode current density (bandgap) – ideality factor may be sensitive to current density – stay away from cliff

Device Reliability

- Gate Overstress
 - especially likely during power-down, reset, test
 - hspice .biaschk is useful
- Gate Leakage
 - LPF especially, $I_{\text{leak}}(\text{LPF}) < \text{a few nA}$
 - Switches used for test modes
 - Gate loads of high-impedance nodes (e.g. bandgap)
 - Large op-amp inputs

Device Reliability

- Check PMOS devices for NBTI-sensitivity and NMOS devices for PBTI-sensitivity
 - V_{gs} of matched devices should be the same at all times, even when not selected (e.g. current-steering DAC) – don't place switches closest to supply rails
 - switching circuits such as VCO and FBDIV should have enough frequency headroom to allow for aging. High V_{gs} is bad! 10-20% margin?
 - effects worse at sub-90nm and may not be well-modeled

Lithography/Devices

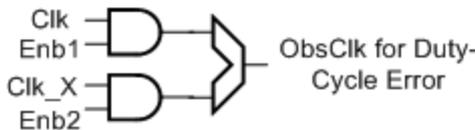
- Add dummy poly to reduce ACLV (across chip linewidth variation), esp. in L_{\min} devices
- Maintain gate poly on fixed pitch in same orientation to reduce ACLV (esp. in L_{\min} devices)
- Try to maintain constant poly density – e.g. no large caps next to sensitive L_{\min} devices)
- Add dummy devices if stress/strain is applied and matching is required (e.g., charge-pump)

Tips for Design for Test

- Measuring Jitter and Phase Error
- Measuring Loop Dynamics
- Analog Measurements
- Probing

Getting Clocks from PLL to Board

- Differential I/O outputs highly desirable to reject common-mode noise – use fastest, lowest-latency I/O available
- Divide VCO to reduce board attenuation only if necessary
→ make divider programmable
- Measuring duty-cycle
 - add mux to select either true or inverted VCO clock
 - Duty-cycle error = $(\text{Duty}+ - \text{Duty}-) / 2$
 - E.g. $\text{Duty}(\text{true}) = 56\%$, $\text{Duty}(\text{inv}) = 54\% \rightarrow \text{Error} = 1\%$



Getting Clocks from PLL to Board

- Ability to disable neighboring I/O when measuring jitter
- Observe REF, VCO, and FBCLK. Gate all but the observed clock at the inputs of the clock observation mux to minimize coupling between clocks



- Phase error measurement: trigger scope on REFCLK on board. Capture internal REFCLK and FBCLK in infinite persistence. Measure difference between internal REFCLK and FBCLK on *same* pin.

Measuring Loop Dynamics

- Modulate reference phase at various modulation frequencies and measure VCO phase using TIE
 - used to construct closed-loop transfer function
- On-chip state-machines
 - range from simple to sophisticated
 - disturb locked PLL in some way and observe re-lock behavior

Analog Measurements

- Need ability to measure key internal analog signals without injecting noise
 - Loop filter control voltage
 - Ring Oscillator regulated supply
 - Bandgap reference
 - Regulated power supplies
 - Charge-pump bias voltages and currents
- Metrics
 - Measurement BW \sim PLL Bandwidth or less
 - Accuracy \sim 5mV?
 - Programmable via JTAG

Analog Measurements

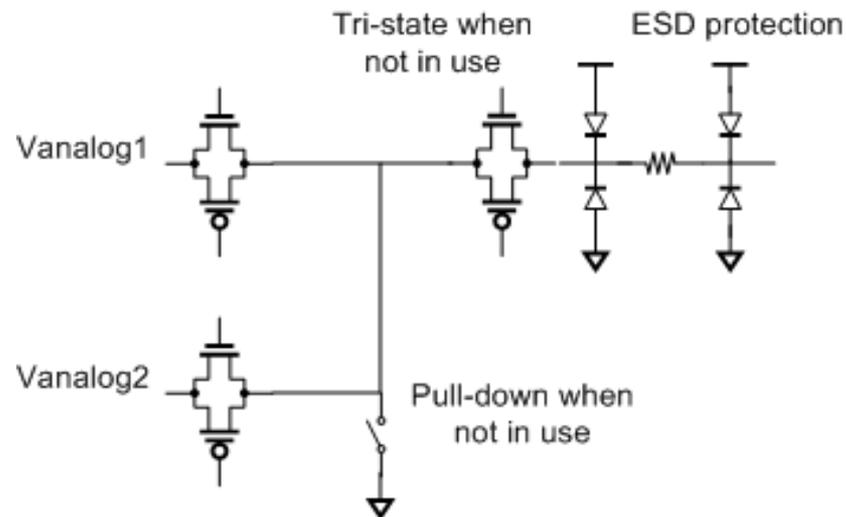
- Internal A/D
 - Can be fairly slow
 - Minimize mux switch leakage into A/D front-end
 - Minimize coupling to sensitive signals
 - May require external analog pin for calibration
 - Compare analog voltage to internally-generated voltage reference
 - Use state-machine to minimize # of comparators to save area
 - Disable when not in use to save power

Analog Measurements

- Analog Observation Pins
- Force or sense voltage/current
- Low BW – high impedance analog signals and high parasitics
- Need ESD (HBM,CDM) to protect signals –watch for leakage
- Can wire-OR analog observation pins from several PLL's but watch for increased pin leakage causing IR drops across pass-gates (e.g., 3-6k Ω) or causing high-impedance analog signals to droop
- Buffer control voltage before sending off-chip to prevent leakage and extra load from upsetting feedback loop – watch for gate leakage in unity-gain buffer

Analog Measurements

- Two-level transmission-gate analog mux connects analog signals to outside world
- Pull-down to VSS middle node of two-level mux when not in use to minimize coupling of noisy pin to analog signals (at expense of increased leakage).



Probing On-chip (last resort!)

- If not flip-chip, then put probe pads on top-layer metal
- Probe pad size $> 1\mu\text{m} \times 1\mu\text{m}$. Prefer $> 2\mu\text{m} \times 2\mu\text{m}$
- Place probe pad on a side-branch of analog net to avoid breaking wire with probe
- Separate probe pads to allow room for multiple probes
- FIB: can add probe pad, add or remove wires
 - need room and luck

Summary: Uncle D's PLL Top 5 List

1. Maintain damping factor ~ 1 for low period jitter apps
2. VDD-induced and intrinsic VCO noise – loop can't do the work for you
3. Leaky loop filter gate caps will cost you your job
4. Make FBDIV run faster than VCO
5. Observe VCO, FBCLK, REF, clkTree on differential I/O pins – you can't fix what you can't see!

Special thanks to Alvin Loke for allowing to me “borrow” some of his diagrams and ideas for this talk...which ones? The good ones

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PLL Failures

PLL Failures

- Observation is that VCO frequency is pinned at max value. Can't observe Vctl or feedback clock. VCO fails to oscillate at low frequency because of insufficient gain in 3-stage VCO. When VCO finally starts, FBDIV can't keep up, causing "run-away" Solution: increase gain of delay stage and FBDIV speed.
- VCO "run-away" when re-locking to higher frequency due to VCO overshoot and slow FBDIV.
- VCO loses lock occasionally at low frequencies. Due to insufficient VCO level-shifter gain. Dropped VCO edges. Required real-time scope for debug
- High jitter at low VCO frequencies due to Vctl approaching V_t of V2I current source. Solution: operate VCO at 2X.

PLL Failures

- Occasional high deterministic jitter caused by coupling into PLL's VDDA bondwire.
- Extremely high period jitter – caused by incorrect wiring of 8-bit charge-pump setting. Bandwidth much too high. Verilog model did not check for legal input settings.
- PLL won't start-up at low temp due to weak start-up circuit in voltage regulator and lack of simulation at corners with slow VDDA ramp-rate.
- PLL period modulated strongly by 400MHz signal, resulting from oscillating internal feedback loop in VCO bias ckts. Ultimate cause, fab misprocessing of compensation cap and insufficient margin in ckt.

PLL Failures

- Metastability condition corrupted digital loop filter due to slow devices, low V_{dd} , and insufficient design margin.
- Digital VCO out-of-range due to resistor mis-processing. Solution: fusible chicken-bits to adjust frequency range.
- Race condition in digital loop filter caused by missing synchronizers in clock domain crossing.

PLL Failures

- CDM ESD failures of analog measurement pins – no visual inspection and no extraction/simulation of connection to VSS.
- Duty-cycle corruption ($> 57\%$) – caused by unbalanced fanouts in delay stages after VCO – exacerbated by single-ended clocking.
- Contention in analog observation signals due to ESD diodes wired backward and control logic bugs.
- Inconsistent duty cycle. Failure to initialize state in post-VCO divider exposed VCO duty-cycle error.