A Cascade Multilevel Inverter Using a Single DC Source

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***Abstract*— A method is presented showing that a cascade multilevel inverter can be implemented using only a single DC power source and capacitors. A standard cascade multilevel inverter requires n DC sources for $2n + 1$ levels. Without requiring transformers, the scheme proposed here allows the use of a single DC power source (e.g., a battery or a fuel cell stack) with the remaining $n-1$ DC sources being capacitors. It is shown that one can simultaneously maintain the DC voltage level of the capacitors and choose a fundamental frequency switching pattern to produce a nearly sinusoidal output.**

***Index Terms*— Multilevel Inverter, Fuel Cell**

I. Introduction

A cascade multilevel inverter is a power electronic device built to synthesize a desired AC voltage from several levels of DC voltages. Such inverters have been the subject of research in the last several years [1][2][3][4][5], where the DC levels were considered to be identical in that all of them were either batteries, solar cells, etc. In [6], a multilevel converter was presented in which the two separate DC sources were the secondaries of two transformers coupled to the utility AC power. In contrast, in this paper, only one source is used without the use of transformers. The interest here is interfacing a single DC power source with a cascade multilevel inverter where the other DC sources are capacitors. Currently, each phase of a cascade multilevel inverter requires n DC sources for $2n+1$ levels in applications that involve real power transfer. In this work, a scheme is proposed that allows the use of a single DC power source (e.g., battery or fuel cell stack) with the remaining $n-1$ DC sources being capacitors. It is shown that one can simultaneously maintain the DC voltage level of the capacitors and choose a fundamental frequency switching pattern to produce a nearly sinusoidal output.

II. Multilevel Inverter Architecture

To operate a cascade multilevel inverter using a single DC source, it is proposed to use capacitors as the DC sources for all but the first source. Consider a simple cascade multilevel inverter with two H-bridges as shown in Fig. 1.

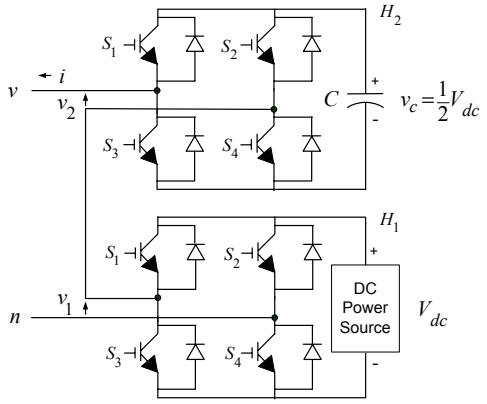

Fig. 1. Single-phase structure of a multilevel cascaded H-bridges inverter.

The DC source for the first H-bridge (H_1) is a DC power source with an output voltage of V_{dc}, while the DC source

for the second H-bridge (H_2) is a capacitor voltage to be held at $V_{dc}/2$. The output voltage of the first H-bridge is denoted by v_1 and the output of the second H-bridge is denoted by v_2 so that the output of this two DC source cascade multilevel inverter is $v(t) = v_1(t)+v_2(t)$. By opening and closing the switches of H_1 appropriately, the output voltage v_1 can be made equal to $-V_{dc}$, 0, or V_{dc} while the output voltage of H_2 can be made equal to $-V_{dc}/2$, 0, or $V_{dc}/2$ by opening and closing its switches appropriately. Therefore, the output voltage of the inverter can have the values $-3V_{dc}/2, -V_{dc}, -V_{dc}/2, 0, V_{dc}/2, V_{dc}, 3V_{dc}/2$, which is seven levels and is illustrated in Fig. 2(a). Table I shows how a waveform can be generated using the topology of Fig. 1.

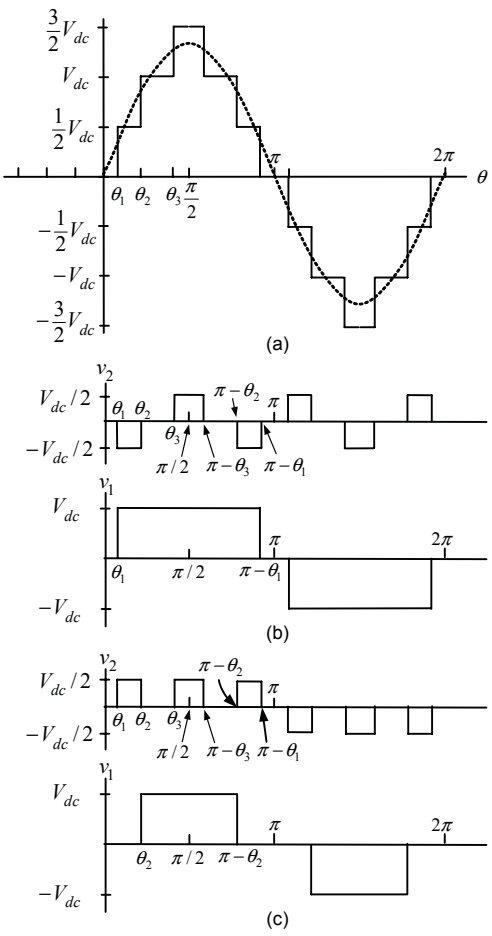

Fig. 2. (a) Output waveform of an 7-level cascade multilevel inverter. (b) and (c) H-bridge voltages v_1 and v_2 which achieve the same output voltage waveform $v = v_1 + v_2$.

TABLE I. OUTPUT VOLTAGES FOR A 7-LEVEL INVERTER

θ	v_1	v_2	$v = v_1 + v_2$
$0 \le \theta \le \theta_1$	0	0	0
$\theta_1 \le \theta \le \theta_2$	0	$V_{dc}/2$	$V_{dc}/2$
$\theta_1 \le \theta \le \theta_2$	V_{dc}	$-V_{dc}/2$	$V_{dc}/2$
$\theta_2 \le \theta \le \theta_3$	V_{dc}	0	V_{dc}
$\theta_3 \le \theta \le \pi/2$	V_{dc}	$V_{dc}/2$	$3V_{dc}/2$

Fig. 2(b) shows how the waveform of Fig. 2(a) is generated if, for $\theta_1 \le \theta \le \theta_2$, $v_1 = V_{dc}$ and $v_2 = -V_{dc}/2$ is chosen. Similarly, Fig. 2(c) shows how the waveform of Fig. 2(a) is generated if, for $\theta_1 \le \theta \le \theta_2$, $v_1 = 0$ and $v_2 = V_{dc}/2$ is chosen. The fact that the output voltage level $V_{dc}/2$ can be achieved in two different ways is exploited to keep the capacitor voltage regulated. Specifically, one measures the capacitor voltage v_c and the inverter current i. Then, if $v_c < V_{dc}/2$ and $i > 0$, one sets $v_1 = V_{dc}$ and $v_2 = -V_{dc}/2$ and the capacitor is being charged. Table II summarizes this case along with the discharge case $v_c > V_{dc}/2$.

TABLE II. CONTROLLER FOR CAPACITOR VOLTAGE LEVEL

System State	v_1	v_2	$v = v_1 + v_2$
$v_c < V_{dc}/2, i > 0$	V_{dc}	$-V_{dc}/2$	$V_{dc}/2$
$v_c < V_{dc}/2, i < 0$	0	$V_{dc}/2$	$V_{dc}/2$
$v_c > V_{dc}/2, i > 0$	0	$V_{dc}/2$	$V_{dc}/2$
$v_c > V_{dc}/2, i < 0$	V_{dc}	$-V_{dc}/2$	$V_{dc}/2$

By choosing the nominal value of the capacitor voltage to be one half that of the DC power source, the nominal values of the levels are equally spaced. However, this is not required. The criteria required for this capacitor regulating scheme is that (1) the desired capacitor voltage is less than the DC power source voltage, (2) the capacitance value is chosen large enough so that the variation of its voltage around its nominal value is small, and (3) the capacitor charging cycle is greater than the capacitor discharge cycle.

III. SWITCHING ANGLES

If the nominal capacitor voltage is chosen as $V_{dc}/2$, then one can compute the switching angles θ_1, θ_2, and θ_3 as in [7]. Following the development in [7] (see also [8]), the Fourier series expansion of the (staircase) output voltage waveform of the multilevel inverter as shown in Fig. 2(a) is

$$V(\omega t) = \frac{4}{\pi}\frac{V_{dc}}{2} \times \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n}\Big(\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)\Big)\sin(n\omega t). \quad (1)$$

Ideally, given a desired fundamental voltage V_1, one wants to determine the switching angles θ_1, θ_2, and θ_3 so that (1) becomes $V(\omega t) = V_1 \sin(\omega t)$. In practice, one is left with trying to do this approximately. For three-phase systems, the triplen harmonics in each phase need not be canceled as they automatically cancel in the line-to-line voltages. In this case where there are 3 DC sources, the desire is to cancel the 5^{th} and 7^{th} order harmonics as they tend to dominate the total harmonic distortion. The mathematical statement of these conditions is then

$$\begin{aligned} \frac{4}{\pi}\frac{V_{dc}}{2}\Big(\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3)\Big) &= V_1 \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) &= 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) &= 0. \end{aligned} \quad (2)$$

This is a system of three transcendental equations in the three unknowns θ_1, θ_2, and θ_3. There are many ways one can solve for the angles (see, for example, [9], [10], and [11]). Here the approach in [7] and [12] is used.

IV. Experimental Results

A three-phase wye-connected cascaded multilevel inverter using 100 V, 70 A MOSFETs as the switching devices [13] was used to carry out the experiments. A power supply was used as the DC power source with $V_{dc} = 25$ V and a 8 mF capacitor was used as the second DC source. The real-time controller was implemented on an FPGA chip with an 8 μsec time step where the switching angles as a function of the modulation index were stored in a lookup table. The multilevel converter was connected to a three phase induction motor whose nameplate data is 1/3 hp, 1.5 A, 1725 rpm and 208 V (RMS line-to-line at 60 Hz).

With $m \triangleq V_1 / \left(\frac{4}{\pi}\frac{V_{dc}}{2}\right)$ [see equation (2)], Fig. 3 shows the inverter voltage waveforms of the three phases for $m = 1.32$ and $f = 60$ Hz. (Note that the modulation index is m/s where s is the number of DC sources, which in this experiment is $s = 2$).

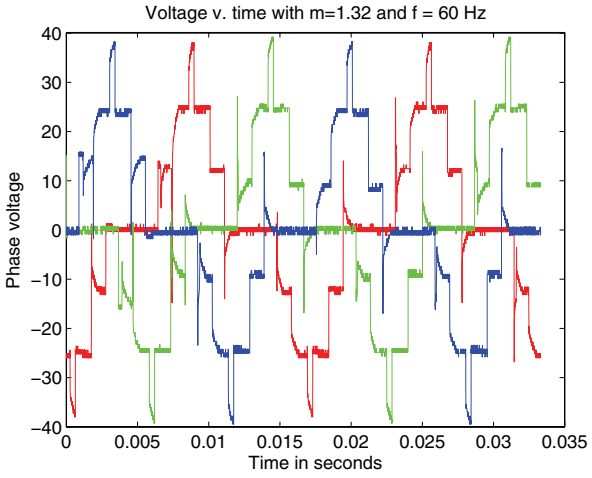

Fig. 3. Three-phase output waveforms of the seven-level multilevel inverter.

Note that the second level in Fig. 3 is constant at 25 V because this level is due to only the power supply source with the capacitor voltage not being used. However, the first level and the third level both require using the capacitor voltage, and note that they are not constant. In particular, note that the first level varies considerably, but the capacitor voltage controller pushes back in the right direction. The fact that the capacitor voltage varies so much is due to the low value of capacitance used (8 mF).

Also, voltage spikes are seen in Fig. 3. These occur at those times when both of the sources (power supply and capacitor) are being switched in or out simultaneously. This is due to the differences in dead time of the H-bridge switches as well as the timing of turning the switches on and off not being exactly the same between the two H-bridges.

The FFT plot of a line-line voltage waveform is shown in Fig. 4. The 5th and 7th harmonics are not quite zero due to the varying capacitor voltage.

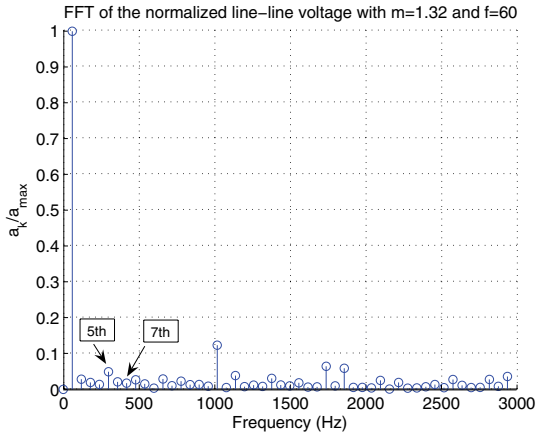

Fig. 4. FFT of the line-line voltage for $m = 1.32$ and $f = 60$ Hz.

Fig. 5 is the current in one of the phases of the induction machine, and its corresponding FFT is shown in Fig. 6.

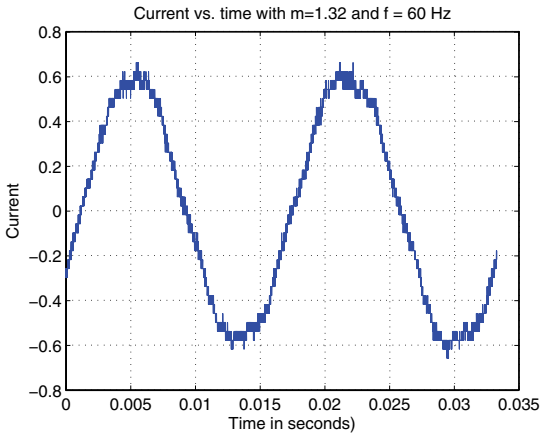

Fig. 5. Phase current waveform with $m = 1.32$ and $f = 60$ Hz.

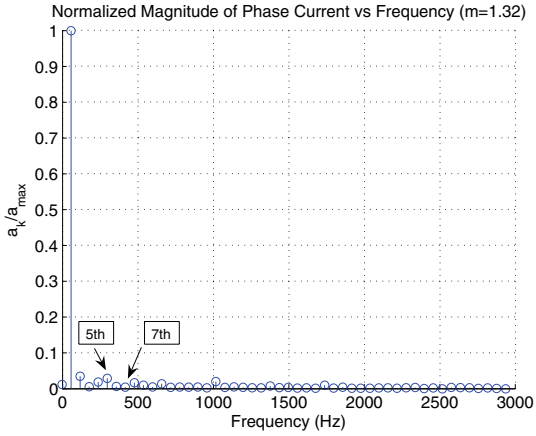

Fig. 6. FFT of the phase current for $m = 1.32$ and $f = 60$ Hz.

V. 15-Level Inverter

Consider now a 15-level inverter with three H-bridges as shown in Fig. 7. The corresponding waveform is shown in Fig. 8.

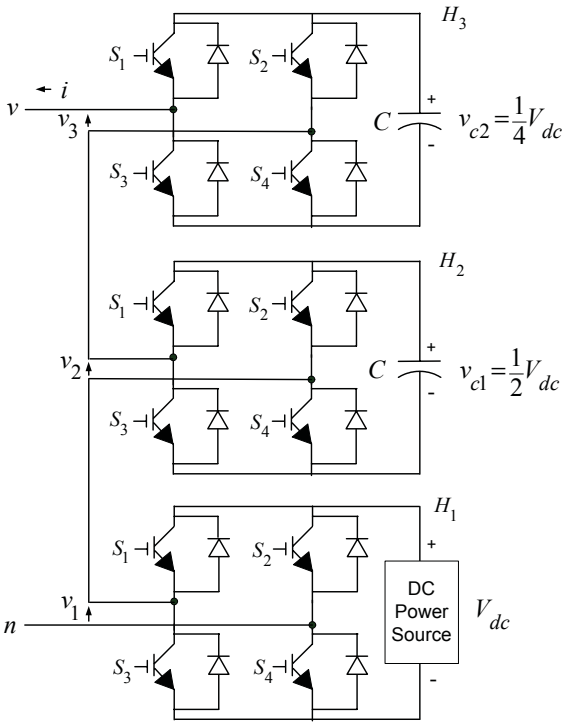

Fig. 7. Hardware architecture for a 15-level (3 DC sources) inverter.

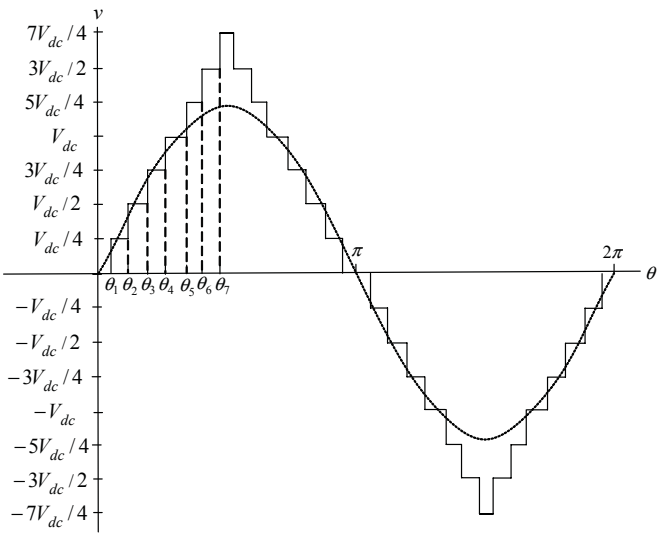

Fig. 8. Hardware architecture and output voltage waveform for a 15-level inverter.

The DC source for the first H-bridge (H_1) is a DC power source with an output voltage of V_{dc}, the DC source for the second H-bridge (H_2) is a capacitor voltage to be held at $V_{dc}/2$, and the DC source for the third H-bridge (H_3) is a second capacitor voltage held at $V_{dc}/4$. As in the 7-level inverter, the capacitor voltages are chosen in this way so that the difference between levels is the same. However, this is not essential. The output voltages of each of the H-bridges are denoted v_1, v_2, and v_3, respectively, so the output voltage of the 15-level inverter is given by $v(t) = v_1(t) + v_2(t) + v_3(t)$. The possible ways in which the voltage waveform of Fig. 8(b) can be achieved are given in Table III.

Table III. Output Voltages for a 15-Level Inverter

θ	v_1	v_2	v_3	$v_1 + v_2 + v_3$
$0 \le \theta \le \theta_1$	0	0	0	0
$\theta_1 \le \theta \le \theta_2$	0		$V_{dc}/4$	$V_{dc}/4$
$\theta_1 \le \theta \le \theta_2$	0	$V_{dc}/2$	$-V_{dc}/4$	$V_{dc}/4$
$\theta_1 \le \theta \le \theta_2$	V_{dc}	$-V_{dc}/2$	$-V_{dc}/4$	$V_{dc}/4$
$\theta_2 \le \theta \le \theta_3$	0	$V_{dc}/2$	0	$V_{dc}/2$
$\theta_2 \le \theta \le \theta_3$	V_{dc}	$-V_{dc}/2$	0	$V_{dc}/2$
$\theta_3 \le \theta \le \theta_4$	0	$V_{dc}/2$	$V_{dc}/4$	$3V_{dc}/4$
$\theta_3 \le \theta \le \theta_4$	V_{dc}	0	$-V_{dc}/4$	$3V_{dc}/4$
$\theta_3 \le \theta \le \theta_4$	V_{dc}	$-V_{dc}/2$	$V_{dc}/4$	$3V_{dc}/4$
$\theta_4 \le \theta \le \theta_5$	V_{dc}	0	0	V_{dc}
$\theta_5 \le \theta \le \theta_6$	V_{dc}	0	$V_{dc}/4$	$5V_{dc}/4$
$\theta_5 \le \theta \le \theta_6$	V_{dc}	$V_{dc}/2$	$-V_{dc}/4$	$5V_{dc}/4$
$\theta_6 \le \theta \le \theta_7$	V_{dc}	$V_{dc}/2$	0	$6V_{dc}/4$
$\theta_7 \le \theta \le \pi/2$	V_{dc}	$V_{dc}/2$	$V_{dc}/4$	$7V_{dc}/4$

VI. Conclusions

A cascade multilevel inverter topology has been proposed that requires only a single DC power source. Subject to specified constraints, it was shown that the voltage level of the capacitors can be controlled while at the same time choosing the switching angles to achieve a specified modulation index and eliminate harmonics in the output waveform.

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