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Study of CAN Protocol for Area and Power Optimization using XILINX and Cadence Software

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Abstract: In this paper we focus on the communication technology in industrial automation and automotive applications for robust network. The CAN Protocol was developed for use in industrial environments and for in-vehicle networks. Some of the CAN features are its multi-master capability, its built-in error detection and correction capability, as well as its unique fault confinement. In this work we design hardware for CAN Top Module based on CAN Architecture using the Xilinx software which are used to improving various functions of CAN protocol parameters such as optimization of area and power, in industrial and different communication system.

I. INTRODUCTION

Robert Bosch introduced the Controller Area Network (CAN) serial bus system at the Society of Automotive Engineers (SAE) congress in Detroitin1986. It was called the "Automotive Serial Controller Area Network" because CAN systems were developed first for the automotive industry.

The goal of this paper is to make automobiles more reliable, safe and fuel-efficient while decreasing wiring harness weight and complexity. Since its inception, the CAN protocol has gained widespread popularity in industrial automation and automotive applications. Other markets where networked solutions can bring attractive benefits like medical equipment, test equipment and mobile machines are also starting to utilize the benefits of CAN. The goal of this application note is to explain some of the basics of CAN and show the benefits of choosing CAN for embedded systems networked applications.

II. BASIC CONCEPT OF CAN PROTOCOL

The CAN bus is a serial communication protocol level supporting real time systems with a high reliable communication. It handles the detection of collisions, errors, the re-transmission of corrupted messages and the priority of sent and received messages.

The CAN protocol has configuration flexibility and prioritization of messages (bit wise arbitration using the identifier). It also have simultaneous reception by multiple nodes with time synchronization for multi-master system. It also has error detection and signalling by each node if automatic retransmission of corrupted messages once the bus is idle again. The CAN protocol have error distinction between temporary errors and a permanent failure of a node with fault confinement if automatic switch off of defective nodes.

III. CAN PROTOCOL PHYSICAL CHARACTERISTICS

The CAN specification does not explain how the single channel which carries bits is implemented. A common way to implement a CAN bus is by using a single wire and a ground. However, the most typical implementation and the main focus of this work is using 2 twisted differential wires, CAN high and CAN low, with 2 termination resistors of 120 ohms each. A typical CAN bus topology when two differential wires are used, based on reference shown in figure-1, the Sr. no. 1 is CAN High Wire (CANH), Sr. no. 2 is CAN Low Wire(CANL) , Sr. no. 3 is Voltage between CANH and CANL, Sr.no.4 is Termination resister(120Ω) and Sr. no. 5,6,7 are nodes.

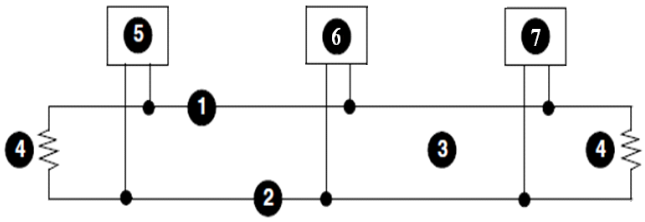

Figure 1 CAN Protocol Topology

Depending on the configuration of the network and the environment, the transmission distance can reach up to 1 km. The bus load related with CAN transceivers, resistors and

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capacitors, but the maximum speed and length are dependent on the acknowledgment bit.

The CAN Architecture
BSP(Bit Stream Processor)
BTL(Bit Timing Logic)

Shift Register
The basic building block CAN Architecture shown in below mention figure 2.

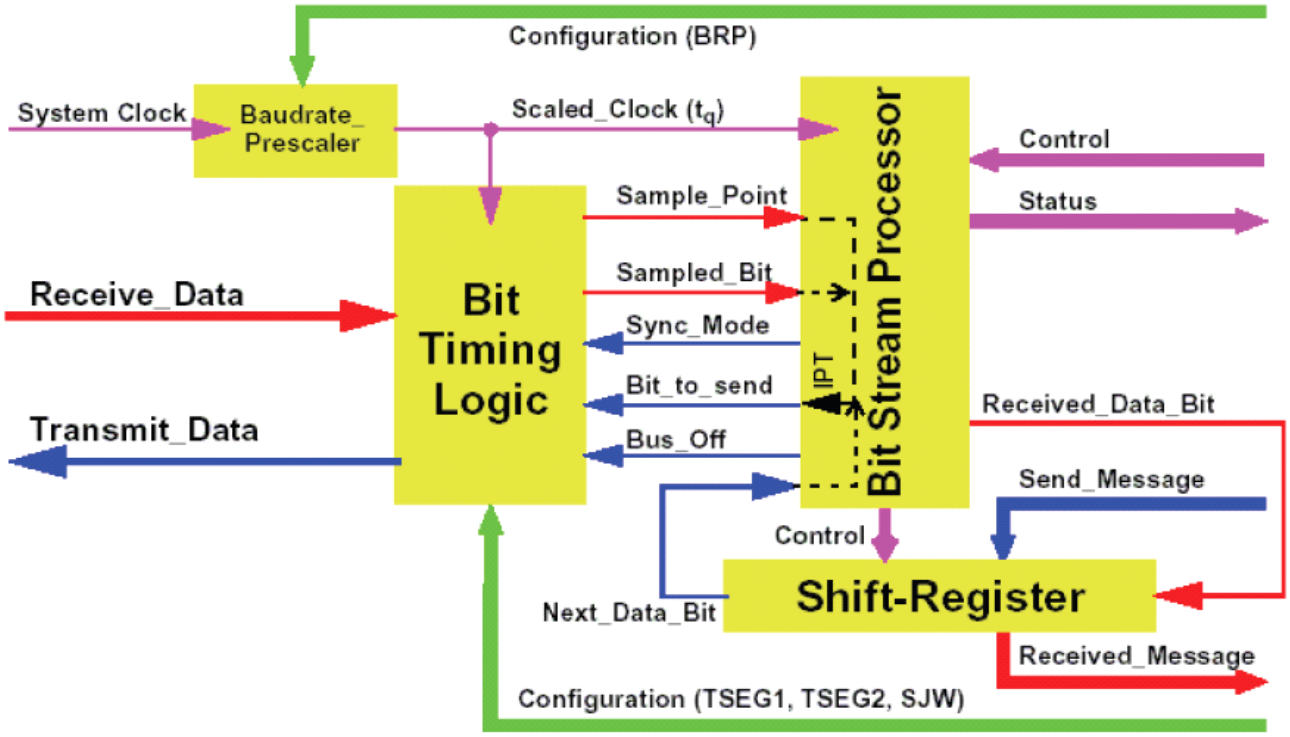

Figure 2 Basic Building Block of CAN Architecture

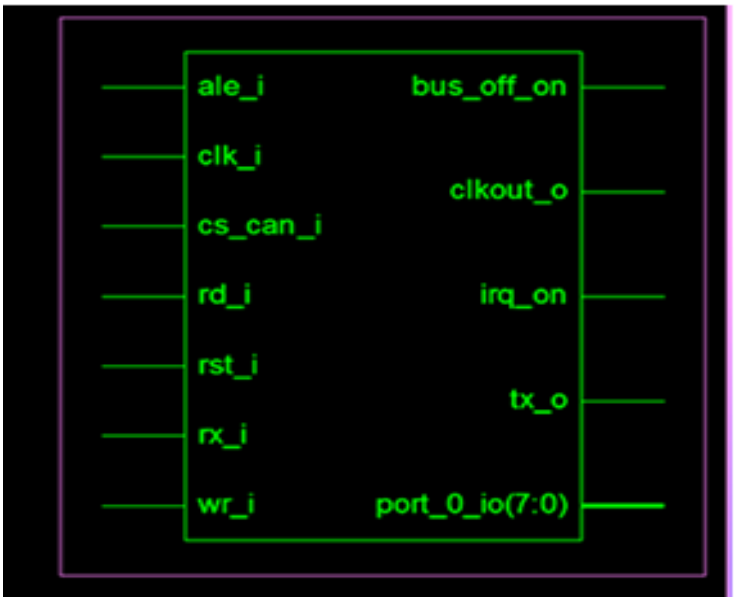

Figure 3 CAN Top Module of Master Controller

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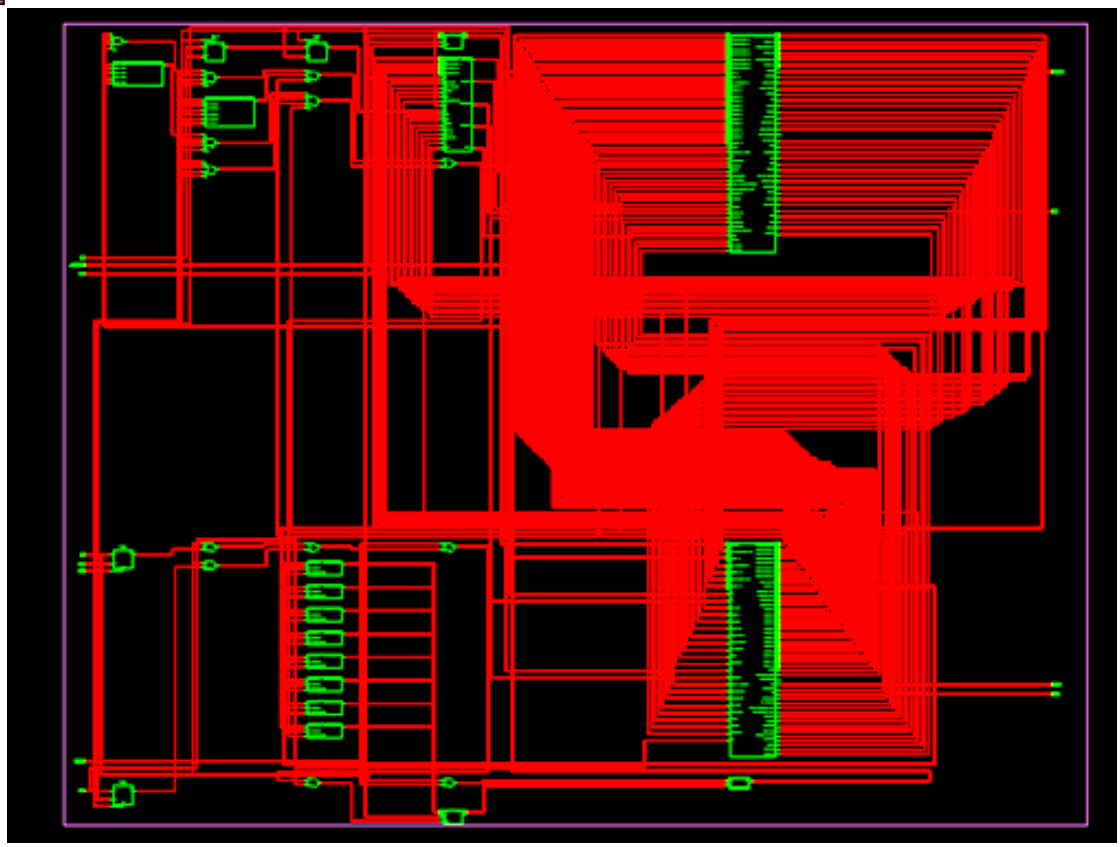

Figure 4 CAN Top Module RTL Diagram

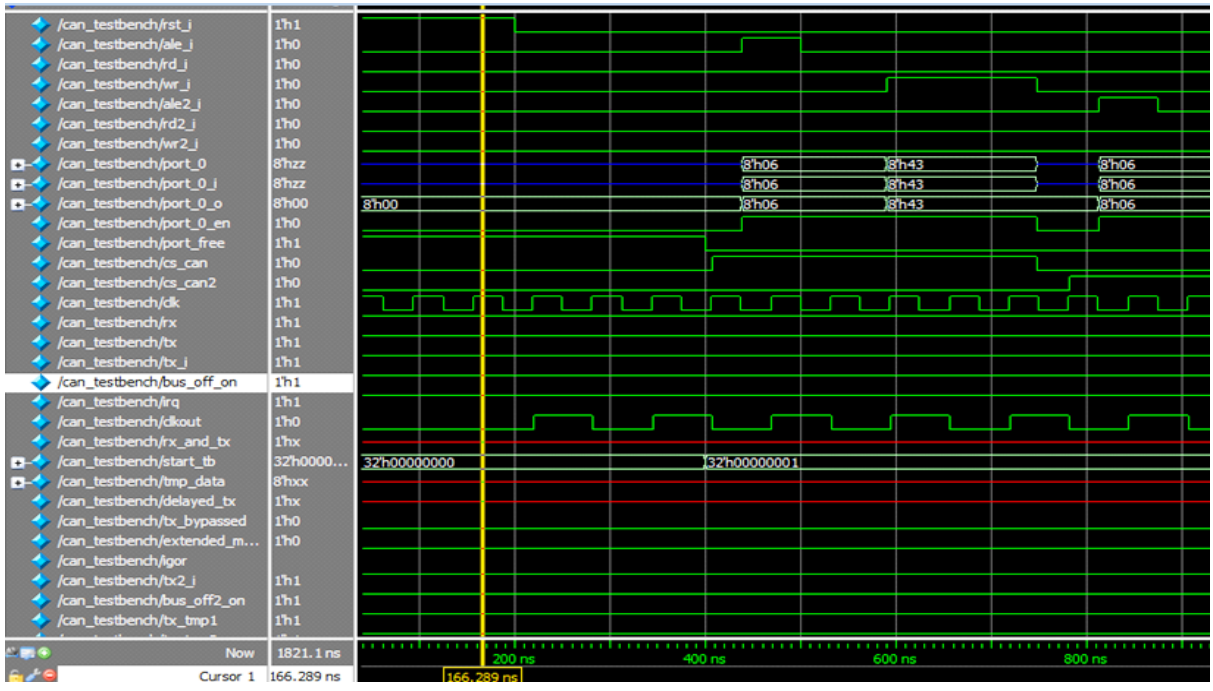

Figure 5 CAN Top Module Bit Timing Diagram

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IV. DESIGN OF CAN ARCHITECTURE

The CAN Architecture used to design hardware CAN Top Module in the Xilinx (Verilog) software which are used to transmit CAN Frames like Data Frame, Error Frame, Repeating Frame, Extended Data Frame etc. In this top module bus ON-OFF signal is used for buses & port is used to transmit frames. The Bit Timing Logic Unit is helpful for meet the timing constrains. It is also responsible to load error frames, overload frames, data sampling etc. The BTL are receive data from baud rate prescaler which is help full to provide timing constrains. It having some timing segment error frames, overload frame data transmission point sample etc.

The Bit timing diagram of CAN Master Controller is show that the generation of data frame, CRC bits, overload frame, error frame, retransmitted frame etc.

In this architecture, we are using same register configuration for different purpose. The CRC is used to generate cycle redundancy code, according to input data. Moderate prescaler are used to divide system clock, according to its external command signal. The baud rate prescaler are provide scanned clock to bit timing logic unit and bit stream processor unit. The shift register are controlled by bit stream processor.

V.CONCLUSION

The CAN protocol goal was to make automobiles more reliable, safe and fuel-efficient while decreasing wiring harness weight and complexity. The CAN user's group estimates that the TTCAN extension will allow Controller Area Network to continue its rapid growth for another ten to fifteen years into a variety of other embedded systems applications. In years to come, CAN systems may be working in just about every type of machine or process. Current systems are proprietary ones and there has been a great problem to find an approach that enables systems to be constructed of standalone units from different suppliers without losing the real-time performance of CAN.

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