Preventing Glitches Circuit in Flash ADC

Jih-Fu Tu

Department Electronic Engineering, St. John's University, Taiwan

tu@mail.sju.edu.tw

Abstract: The purpose of this paper is to design a prevented glitch circuit (PGC) to avoid the destroyed that is caused to glitch in the paralleling comparator Flash ADC. The advantages of this prevented glitch circuit are high-speed, lower power consumption, and size effective, furthermore, it also reduce the faults. We used the TSPC's D flip-flop to achieve this prevented glitch circuit where reduces and improves the glitches and faults, respectively. The PGC is simulated by the Tanner Pro. 13.0 with Generic0_25μm techniques in 0.25-μm. Summarizing the features of this implemented circuit is lower power of 3.3V at 333.3MHz, higher area density is 89.6%, and lower area size is $1221.16 \times 721.793 \mu m^2$.

Keywords: Prevented glitch circuit, ADC, Tranconductance latched comparator.

1. Introduction

In the recent, many papers for ADC were published. In 2000's, [12] issued the Transconductance Latched Comparator circuit and based-on that to implement a switching ADC, but a fault caused by the glitch from decoder. In order to eliminate this glitch and remove it from the DAC, we exploited the TSPC (Technological systems for protective coatings) D-type flip-flop [1, 3, 4, 7, 13] to improve the glitch problems in conventional ADC, to obtain a well waveform in output.

The focus of this paper was using the techniques of parallel comparator [6] to achieve a high-speed A-to-D transfer and lower noise interference, and then improve the glitches from Transconductance Latched Comparator. The ADC circuit derived from Terada et al. [12] that were shown in Figure 1, which is combined of FLASH A/D, sorter, and encoder.

This proposed prevented-glitch circuit aims at reducing the noise glitches to be generated from the output port of Transconductance Latched Comparator then to destroy the fine digital-signal. For an imprecise digital signal is delivered to the decoder that may cause the output signal jumping and fault.
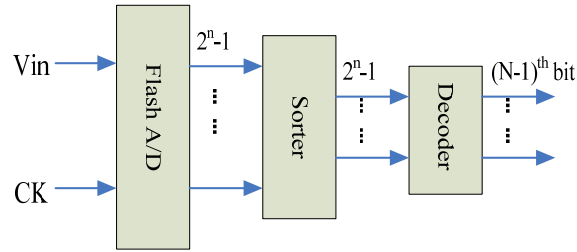

Figure 1.   The ADC structure from Terada et al.

The contributions of this paper not only provide an accuracy digital signal but also lower glitch fault in the ADC's output port. We simulate this prevented glitch circuit using the Tanner Pro. 13.0 tool suit. The technology is Generic0_25μm with 0.25-μm. The specifications of the implemented circuit as follows: 5-bit ADC, operation frequency is 333.3 MHz at 3.3V, and the area is $1221.16 \times 721.793 \mu m^2$.

The rent of this paper is organized as follows. Section 2 describes the relation works of DAC circuits, in the recent. The detail design process of this prevented glitch circuit is shown in Section 3. Section 4 presents the result of the improvement circuit and its fineness waveform. Section 5 shows the physical layout and remarks the conclusions.

2. Previous Works

In 2000's, Terada et al. integrated the Transconductance Latched Comparator [5, 8, 12] into ADC that is compose of the dynamic circuit of FLASH A/D, and static circuit of SORTER and encoder. Because the front circuit needs timing signal of CLOCK. Though the dynamic has higher speed and less number of transistors than static circuit, it is difficult to design.

A parallel comparison Flash ADC circuit [6, 12] is shown in Figure 2 that is used to accomplish the Transconductance Latched Comparator, where had the following specifications: higher conversion speed from analogy to digital, and easily to implement a n-bit ADC only necessary to associate (2^n-1) comparators, The V_{ref} (Reference Value) is connected to the one of input pin of comparator through 2^n serial resistors, and divide V_{ref} into equal $(V_{ref}/2^n)$'s value. The other pins of comparator are connected each other, moreover, an input signal V_{in}, can feed through here. Comparing the magnitude of V_{in} to V_{ref}, if V_{ref} is lower than V_{in} then an high-level signal is represented in the comparator's output, else the output is low-level. The Flash ADC has higher-speed while analog converts to digital, but has more complexion circuit when archives an n-bit ADC need 2^n-1 comparators. Thus, this methodology doesn't suit to higher solution ADC.
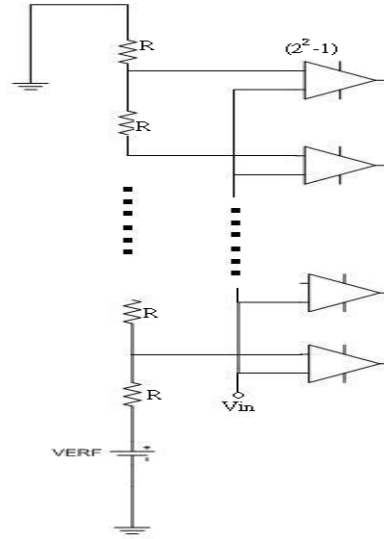
Figure 2.   The circuit of Flash ADC.

A. *Transconductance Latched Comparator*

The Transconductance Latched Comparator is combined with four simply NOT gates $(NOT_1 \sim NOT_4)$, six NMOS $(N_1 \sim N_6)$ logic gates, and one PMOS (P_1). This Transconductance Latched Comparator is operated by three input signals such as clock (CK), V_{in}, and the reference voltage V_{ref}. It also has two output signals such as V_{out+} and V_{out}-, respectively.

The operation of Transconductance Latched Comparator is illustrated as Figure 3. When $V_{in} > V_{ref}$ and the clock is 0, in this time, the circuit is controlled by P_1 switch. This circuit is trigged by the negative-edge.
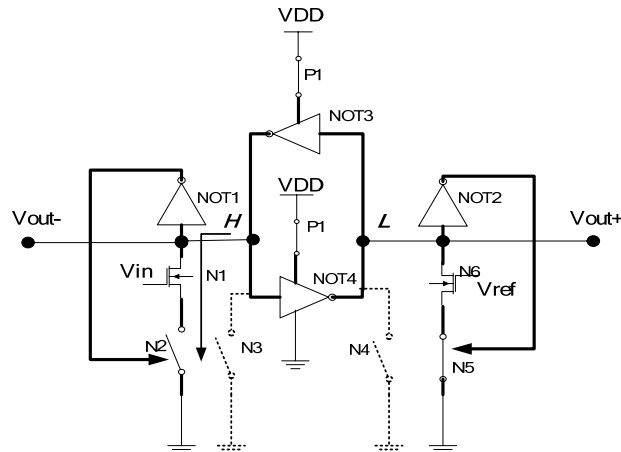

Figure 3.   The operation of Transconductance Latched Comparator

We found a resistor appearance in the output of Transconductance Latched Comparator that was cause of the transistors to due to the fault, which is shown in Figure 4 to be denoted red circles.
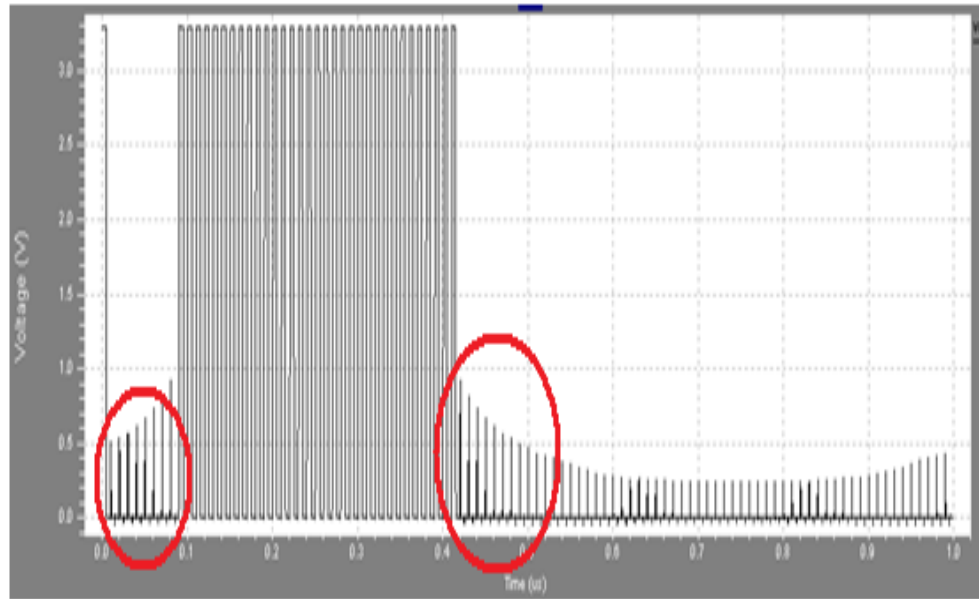

Figure 4.   Resistor causes a fault.

The structure of flash A/D is shown in Figure 5, in where we insert a Butterfly Sorter to remove the faults to happen in output of ADC. SORTER in [12] was made up of n's butterfly sorter, which is interconnected AND gate and OR gate, to correct the faults to be generated by the resistor in the output of flash ADC.

The operation of Butterfly Sorter describes as follows, referring to the top-right of Figure 5, when I_1 and I_2 are fed to "0" and "1", respectively. The output of Q_1 and Q_2 are associated to I_1 and I_2, respectively. Further, it can correct the output wave and remove the fault cause for resistive.
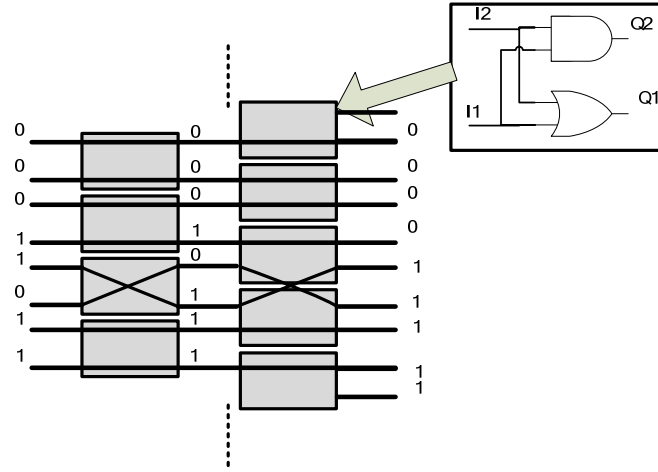
Figure 5.   Butterfly Sorter [3].

B. TSPC

In this paper, we attempt to remove the glitch faults by the conventional TSPC DFF. The TSPC DFF is composed of three PMOSs and three NMOSs, and two input signals and one input output signal. The specifications of those two stages as follows. In the first stage, we make inverting and delay the input voltage [2, 5, 10]. On the other hand, in the second stage, we re-invert and delay the V_{out1} (= V_{in2}). Why do re-invert in the second stage? The main reason is when the CK is low, the output of NMOS will make the output of PMOS to pre-charge up to V_{DD}, through the step-by-step method to obtain the necessary propagation, and the two-stage methodology circuit is shown in Figure 6. We use the charge-recharge flip action in CMOS to make the propagation and to restrain glitches.

Referring to Figure 6, the external second stage is accomplished to NAND gate. When in pre-charge phase, the output of V_{out1} and V_{out2} are pre-charged controlled by the PMOS_1 and PMOS_2, respectively. If a input signal of first stage occurs while CK is high-level, then the output of V_{out1} and V_{out2} are high-level, too. As the specification of two stages and double propagation that is used to implement the prevented glitch circuit (PGC).
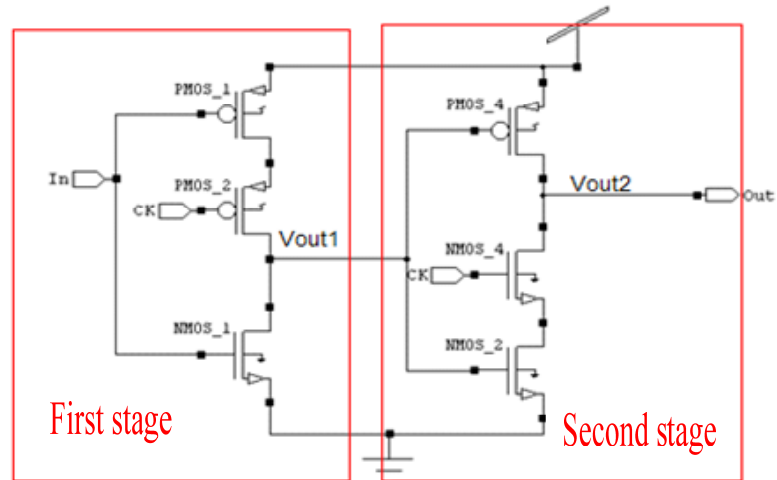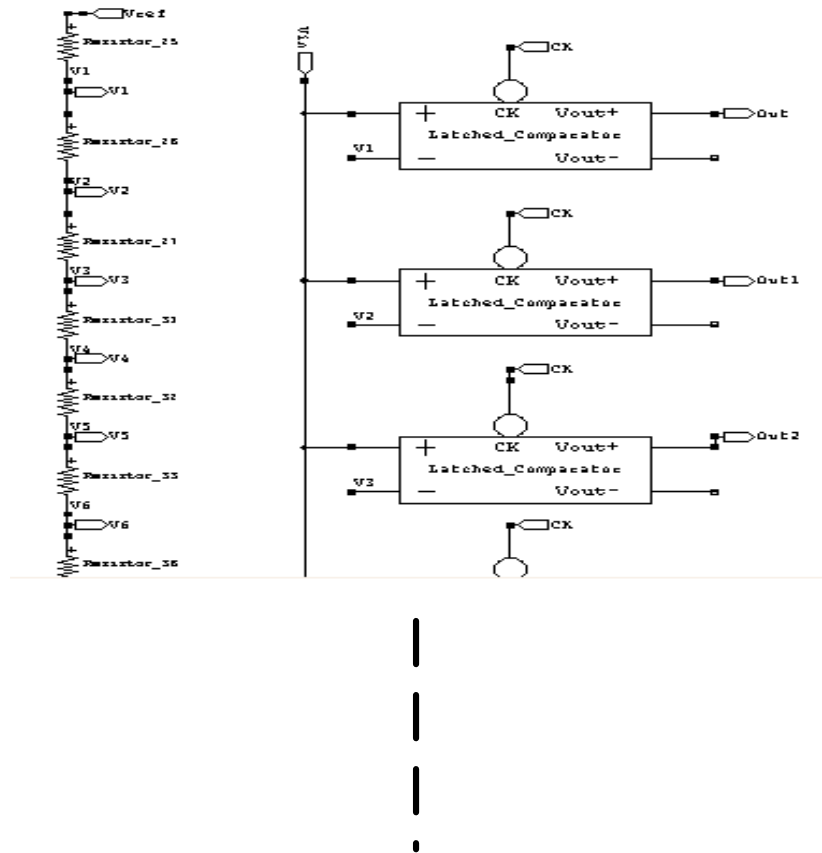
Figure 6.   Two stages circuit.

Figure 7.   The structure of parallel ADC

3. PGC Design

A. Parallel ADC Structure

The front-end of parallel of ADC is composed of two parts, the first part includes of 2^n resistors, and the second part is combination of 2^n-1 comparators, as shown in Figure 7. The V_{ref} is fed to 2^n resistors, and then divides into 2^n equivalent $V_{ref} / 2^n$. Each of $V_{ref} / 2^n$ is connected to the corresponded comparator. When an analog signal occurs in ADC, it will be compared to V_{ref}, immediately. If the input signal is larger than V_{ref} then the analog signal will be delivered to the next stage, else it will be blocked.
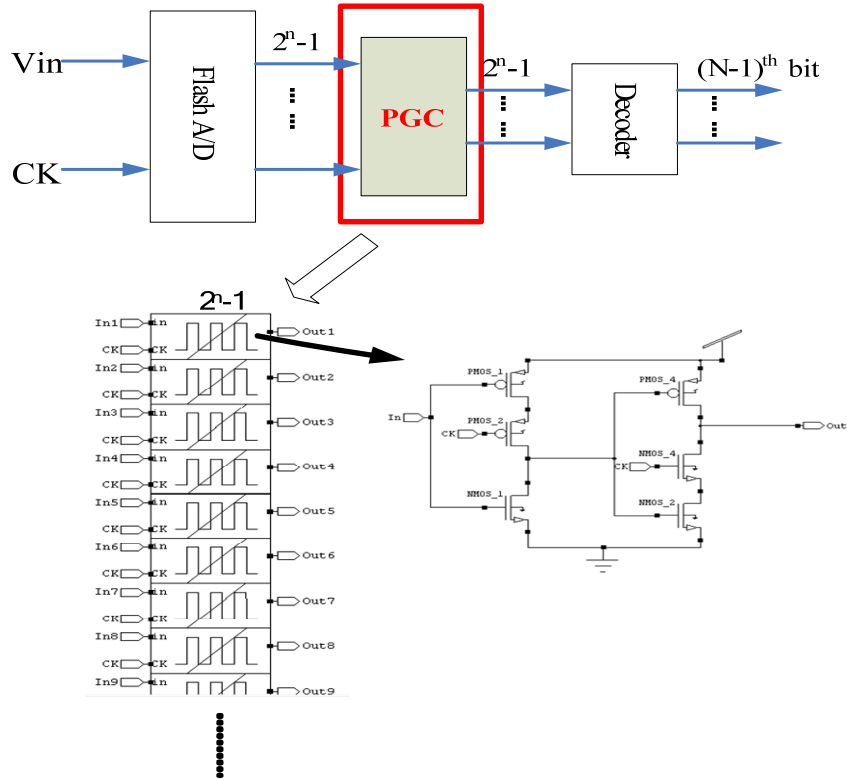

Figure 8.   A PGC block with 2^n-1 sub-circuits

B. Prevented Glitch Circuit (PGC)

We exploit the two-stage method, which is described Figure 6, to achieve the circuit of PGC that is shown in Figure 8. The PGC block is composed of 2^n-1 sub-circuits.   Where n is the bit number of ADC, for instance, a 5-bit ADC needs $2^5-1=31$ two-stage circuits are embedded into the PGC block. That is, we must prepare 31 Parallel ADCs (as shown in Figure 7) to match PGC sub-circuits.

C. Encoder Circuit

The encoder is implemented to the traditional logic-gate, such as AND, OR, and NOT [8, 9, 11]. For instance, a 5-bit ADC of this work has 31 input signals and 5 output signals.

4. The results and Analysis

The physical of this proposed 5-bit ADC is shown Figure 9. It works in 333.33MHz, the operation voltage is 3.3V, in addition to three input signals (analog input V_{in}, V_{ref}, and CK), five output pins denote 5-bit such as O_1, O_2, O_3, O_4, and O_5, respectively.

A. The Output in PGC

We use the butterfly characteristic of charge/re-charge to create the propagation, and then remove the glitches in clock. The charge phase occurs in the 1st stage and re-charge happens in the 2nd stage, both outputs are V_{out1} and V_{out2}, respectively. The wave of 1st output and 2nd input are shown in Figure 10.

We reuse the function of delay causes for reversing. Consequently, in the output port may generate higher density to gain the effect on removing glitch that result is shown in Figure11. The relation of outputs of each stage in PGC is shown in Figure 12.

We probe the output wave of flash ADC in PGC and the CK to find a delay time occurring in this circuit, in where the delay time is one clock cycle and to show in Figure 13.
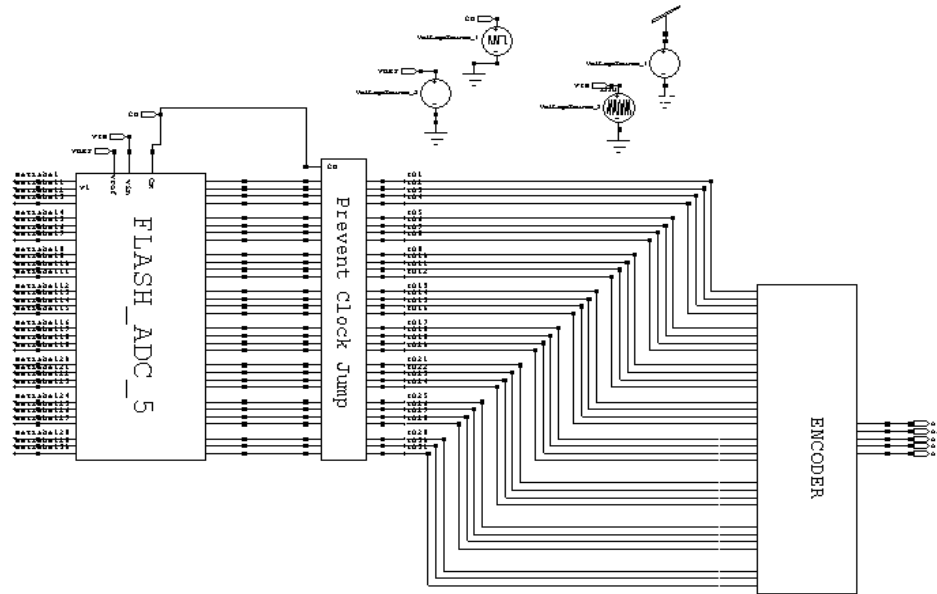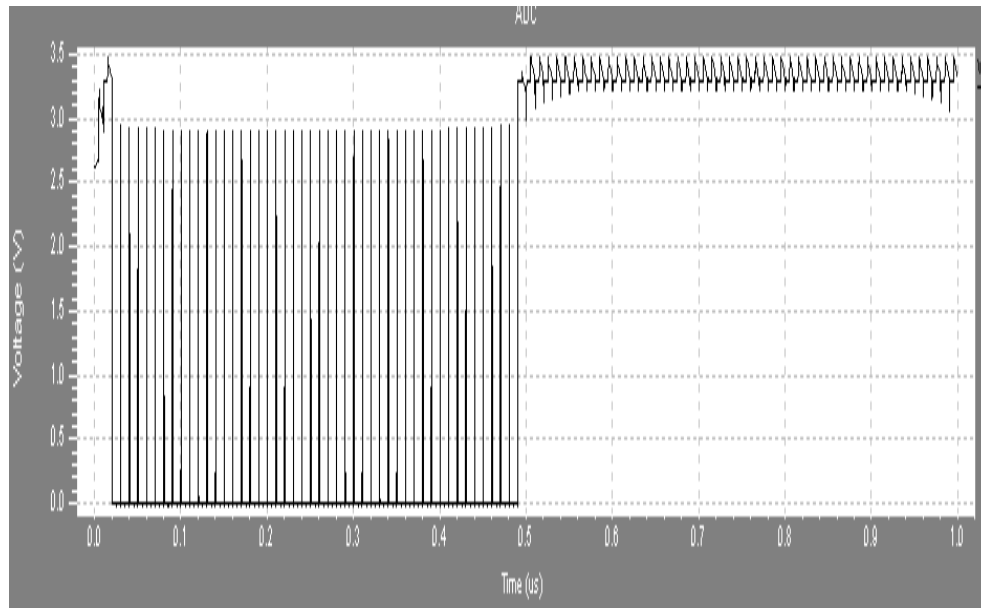

Figure 9. The schematic of 5-bit ADC in this work.

Figure 10.   The wave in 1st and 2nd stage of PGC.
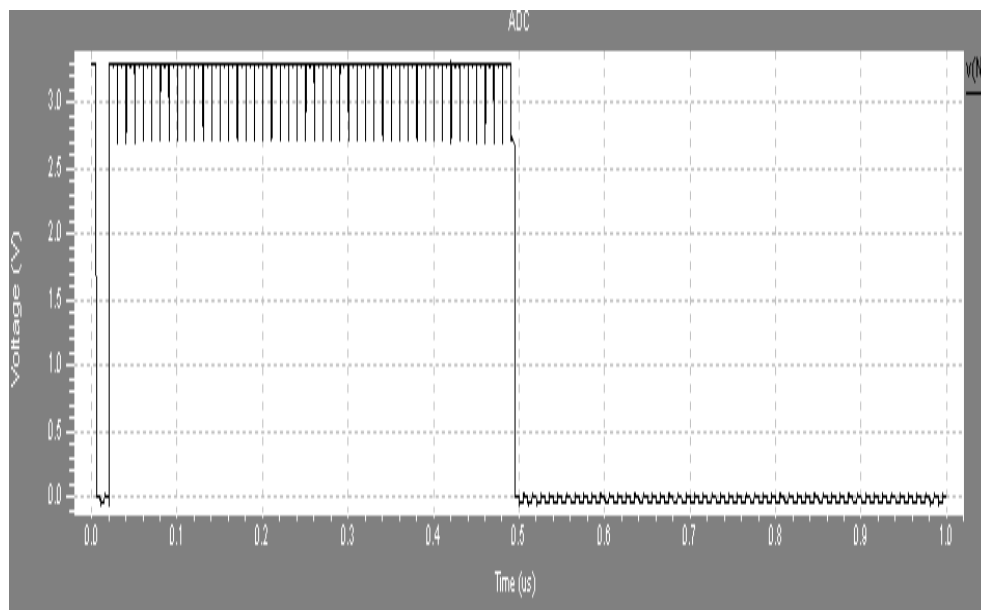

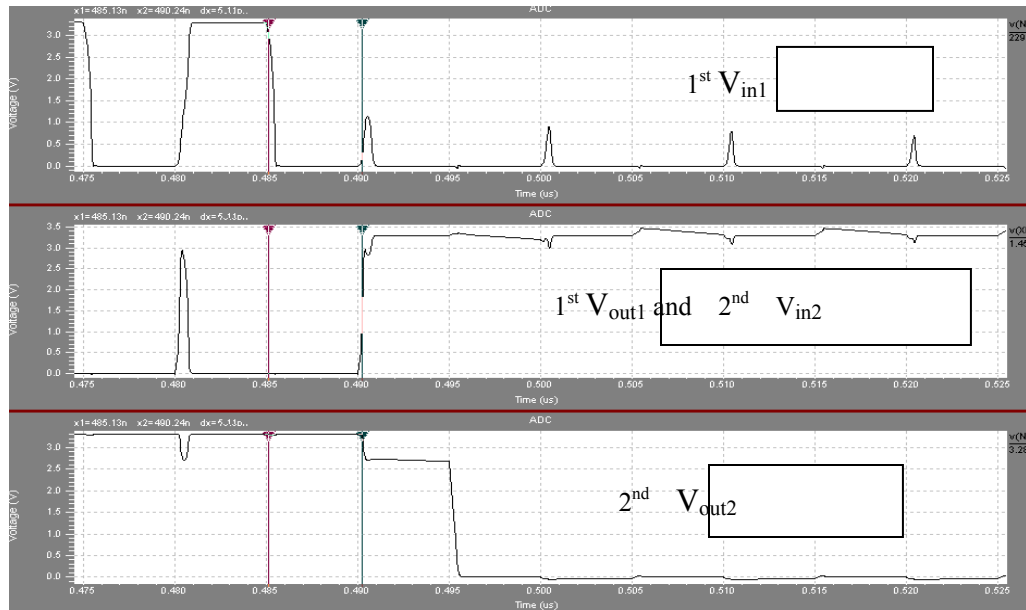Figure 11.   The output of PGC in the 2nd stage.

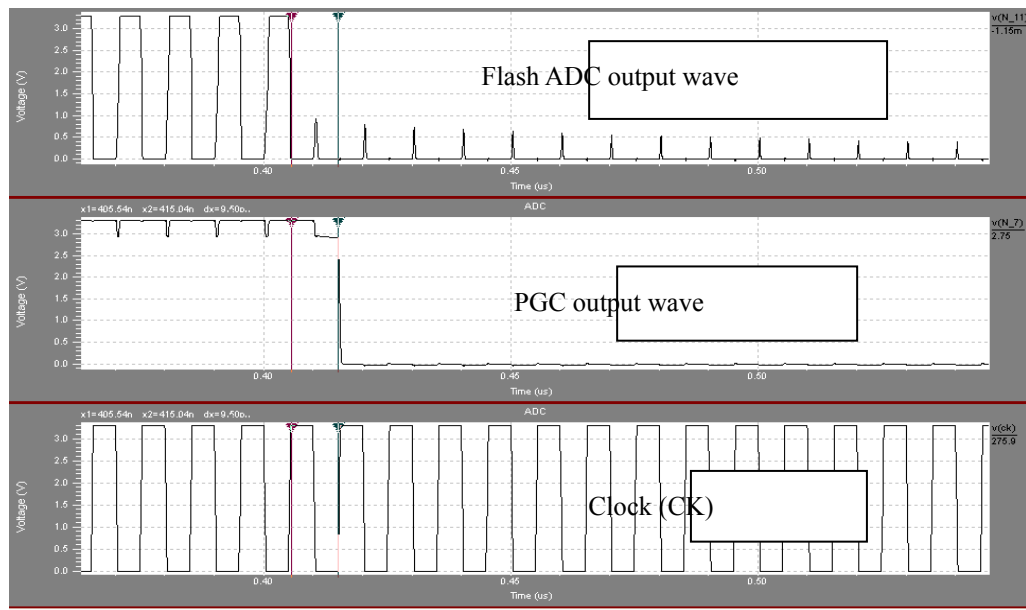Figure 12.   The output in PGC's each stage.

Figure 13.   The output wave in flash-A/D and PGC.

An input analog signal is processed by the achieved PGC's circuit. A stable and fine wave occurs in the output of PGC that is shown in Figure 14. We observe the output wave not find enormous glitch in its output.
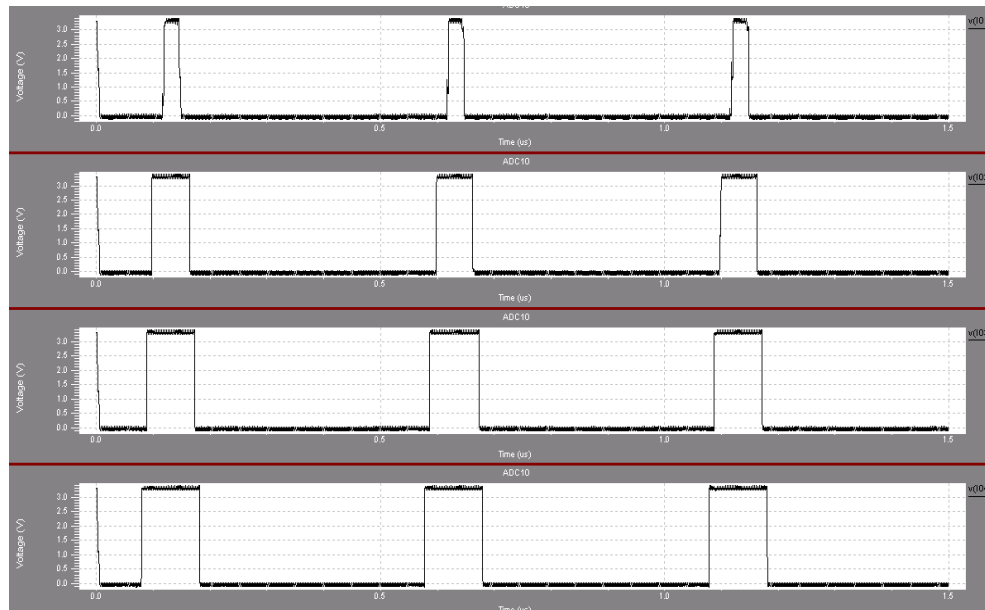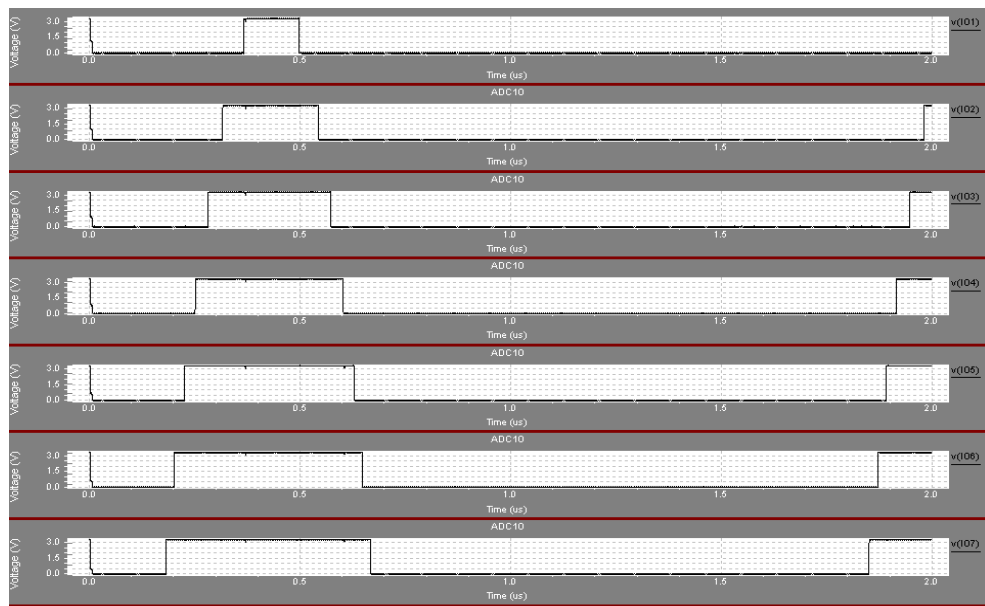
Figure 14.   The fine wave in PGC's output.

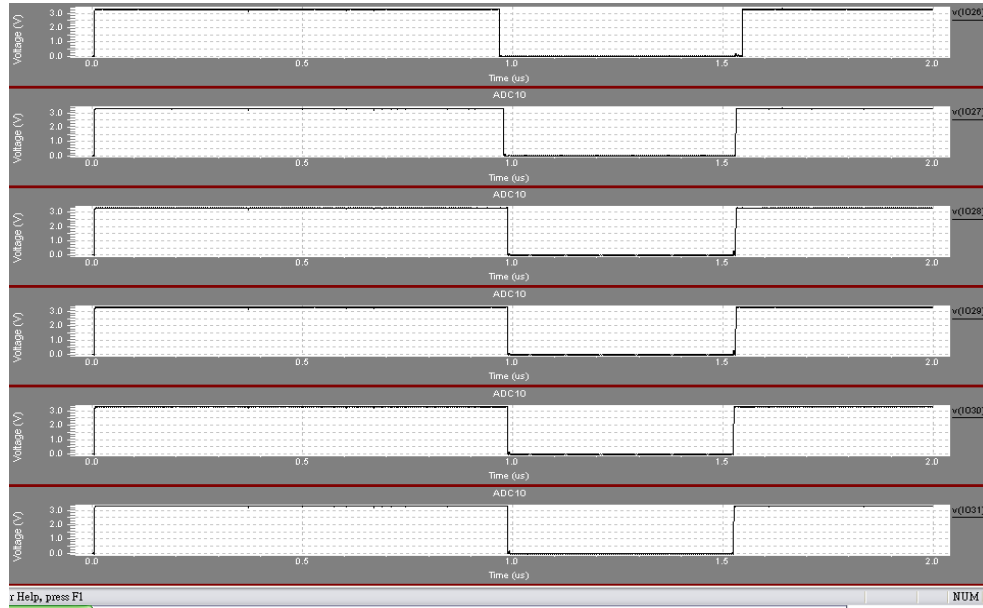Figure 15.   The output wave of ADC in lower order (1-7 digital-step).

Figure 16.   The output wave of ADC in higher order (26-31 digital-step).

B. The Output-wave of 5-bit ADC

For a 5-bit ADC have 31 digitizing output signals. The output wave of 1-7 lower order and 26-31 higher order are shown in Figure 15 and Figure 16, respectively. We observe the output wave finding it very well and fine, and not any glitch jump occurrence.

We also make this improved PGC circuit operating in 166.67MHz and 333.3MHz, the output wave are shown in Figure 17 and Figure 18, respectively.
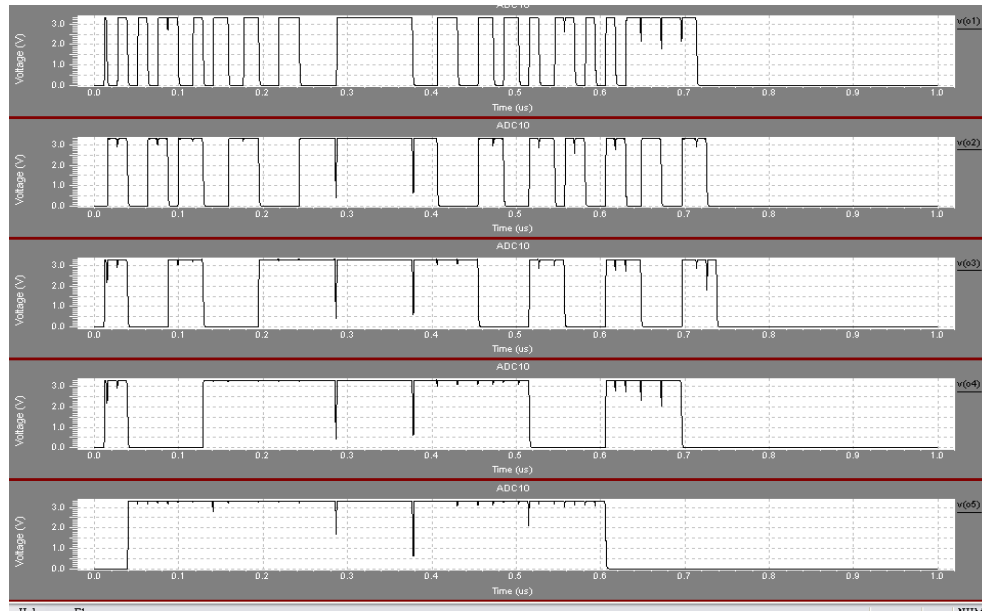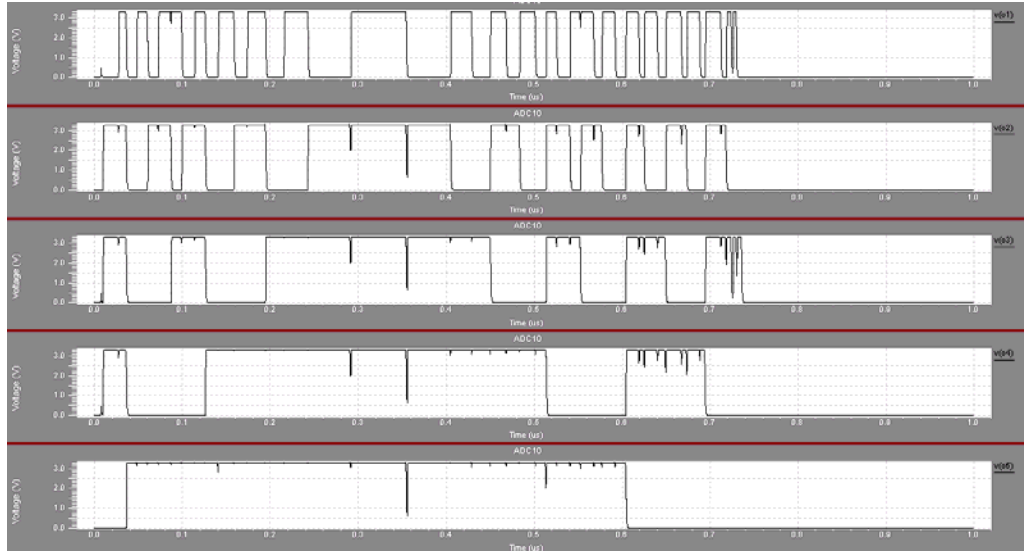

Figure 17.   The output of this work at166.67MHz.

Figure 18.   The output of 5-bit ADC for this work at 333.3MHz
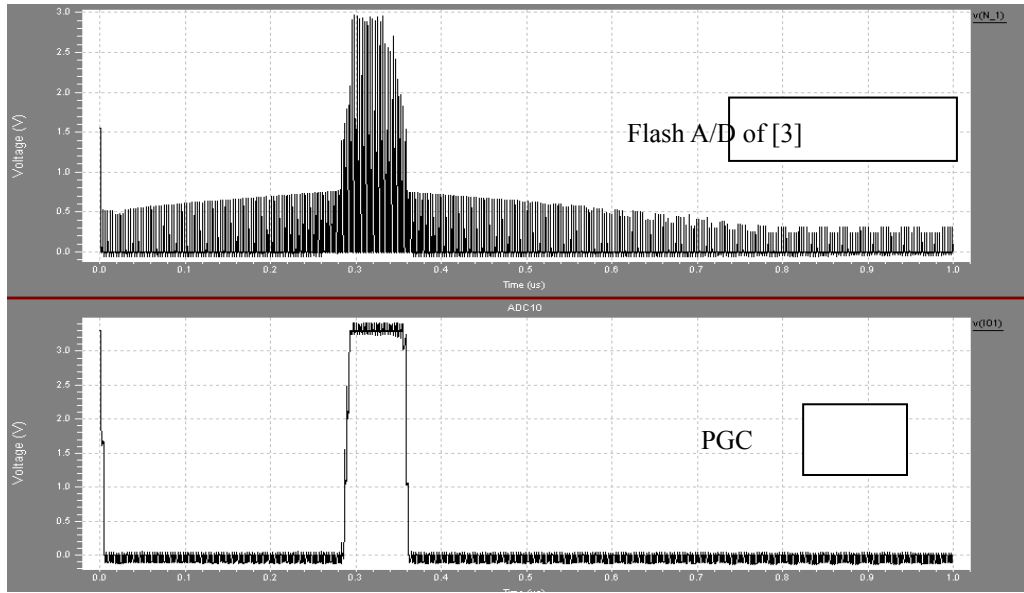
Figure 19.   The output of [3] and PGC at 333.3MHz.

C. Performance Analysis

In this section, we compared the output wave of this implemented PGC to [12], both two are operated in 333.3MHz and 166.67MHz. The output wave is shown in Figure 19 and Figure 20. We find that this improved PGC has higher stability and more fineness than [12]. As the result, that proves the improved ADC circuit not only reducing the area of transistors, but also
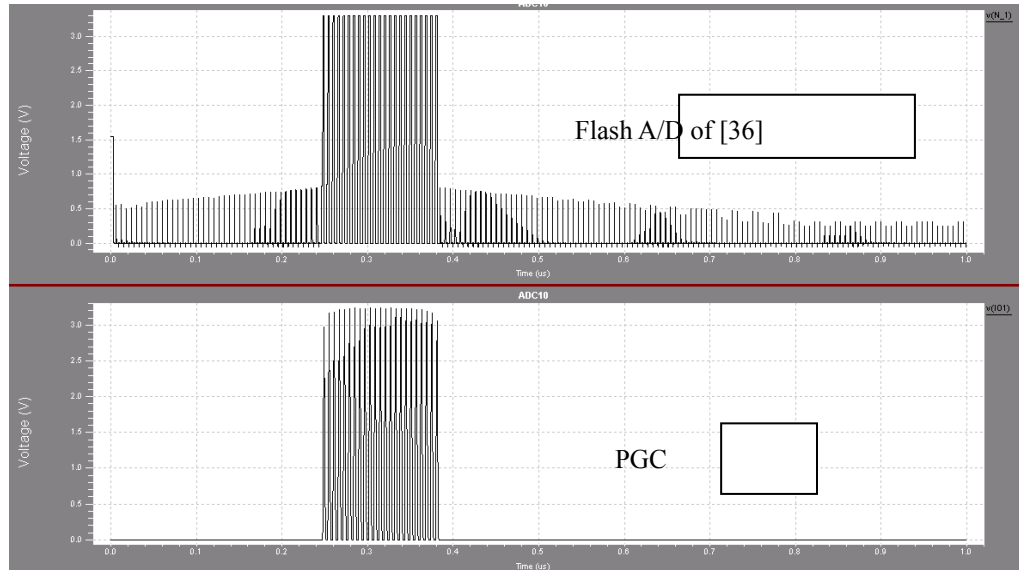
removing the glitch faults.

Figure 20.   The output of [3] and PGC at 166.67MHz.

In this paper, we also simulated this proposed circuit using Tanner Pro Tools 13.0, and the technology was Generic0_25μm 0.25-μm. Figure 21 shows the layout of the whole 5-bit DAC in our work, and its area is $1221.16 \times 721.793 \mu m^2$, only.

We compared our work with [3], we replaced the SORTER by the PGC to reach the goal for preventing glitches. The original structure of the Butterfly Sorter is composed of AND2 and OR2. In other words, we need 6 CMOS transistors to construct the AND2 and OR2. If we want to implement a 5-bit ADC, in which must support 31 Butterfly Sorter, i.e. the numbers of CMOS transistors is 186 (6×31). But, we only need 98 CMOS transistors to construct the PGC. As the result, we can reduce one half area that one half the numbers of CMOS transistors to the traditional structures.

Through simulating, we analyze the output wave of PGC to find that is more stable and fine than [3]. We show that the PGC can implement the goal to reduce glitch and faults.

5.   Conclusions

A 5-bit DAC with the characteristic of glitch prevent s is proposed to achieve high efficiency operation. This proposed circuit is architected to Tanner Pro. Tools 13.0, and the technology is Generic0_25μm 0.25-μm. And then the die area of this 5-bit DAC is 1221.16×721.793μm2. For the power consumption is 3.3V when the operation frequency is

333.3MHz. As for the cost reduction, we need one half the numbers of CMOS transistors to the traditional structures while it is configured and the density is 89.6%. The ADC is popularity application to many system, thus, we have much room to improve the structure of higher-order ADC with hybrid configuration using parallel model or flash model, etc.
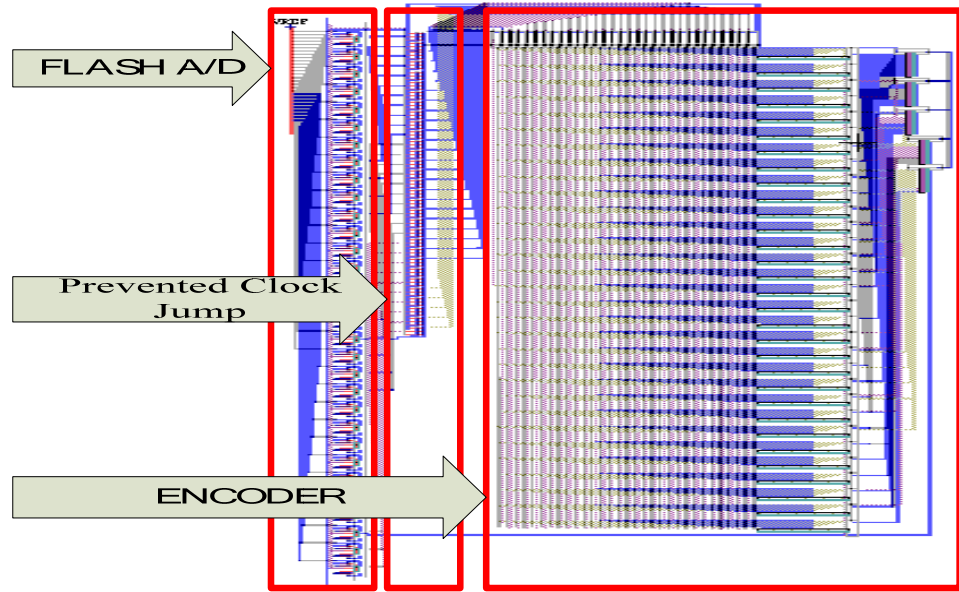

Figure 21.   The layout of 5-bit DAC of our work.

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Jih-Fu Tu received his B. S. degree and M. S. degree in Industrial Education from National Kaohsiung Normal University and National Taiwan Normal University, Taiwan in 1983 and 1990 respectively.

In 2003, he received the Ph. D. degree in Computer Engineering from Proston University in USA. He is now an Associate Professor in Department of Electronic Engineering, St. John's University from 1990. It interests in the field of computer architectures, integrated circuit design, SoC, intelligential node, and discrete event system for Petri net.