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Dependability Investigation of Wireless Short Range Embedded Systems: Hardware Platform Oriented Approach

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Abstract A new direction in short-range wireless applications has appeared in the form of high-speed data communication devices for distances of hundreds meters. Behind these embedded applications, a complex heterogeneous architecture is built. Moreover, these short range communications are introduced into critical applications, where the dependability/reliability is mandatory. Thus, dependability concerns around reliability evaluation become a major challenge in these systems, and pose several questions to answer. Obviously, in such systems, the attribute reliability has to be investigated for various components and at different abstraction levels. In this paper, we discuss the investigation of dependability in wireless short range systems. We present a hardware platform for wireless system dependability analysis as an alternative for the time consuming simulation techniques. The platform is built using several instances of one of the commercial FPGA platforms available on the market place. We describe the different steps of building the wireless hardware platform for short range systems dependability analysis. Then, we show how this HW platform based dependability investigation framework can be a very interactive approach. Based on this platform we introduce a new methodology and a flow to investigate the different parts of system dependability at different abstraction levels. The benefits to use the proposed framework are three fold: first, it takes care of the whole system (HW/SW -digital part, mixed RF part, and wireless part); Second, the hardware platform enables to explore the application's reliability under real environmental conditions taking into account the effect of the environment threats on the system; And last, the wireless platform built for dependability investigation present a fast investigation approach in comparison with the time consuming co-simulation technique.

Keywords: *embedded systems, dependability/reliability, HW/SW co-design, FPGA based design, wireless short range radio, COTS*

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1. Introduction

Wireless networking has revolutionized the way we communicate, the way we monitor resources, and the way we control personal/and professional equipments. In the past few years, wireless computing has strongly increased because of the mobility it provides; in addition to the cost of deployment that dropped considerably. Most of the links in future wireless communication networks will be established over relatively short distances. We would expect, one day, that everything will be wirelessly connected. This new direction in wireless communication is adopted by embedded multimedia applications leaders and microelectronic/semiconductor companies, in order to eliminate wiring between peripherals; head sets or photo-camera connected to printers are -typical examples of such applications.

Behind these applications, a heterogeneous architecture based on digital, analog, and wireless components is built (Figure 1). These systems are become an integral part of our today's life, as they are used in several applications, mobiles and multimedia systems, computer machines, etc. Furthermore, they are even more being introduced into critical systems and business life, such as emergency alarms, medical applications, modern railways, nuclear power controls... etc.

Table 1. Short Range Applications (examples)

Short Range Application	Frequencies MHz	Dependability Requirment
Security Systems	300-900	++++
Emergency Alarms	300-800	+++
Computer (mouse, keyboard)	UHF	++
Wireless Microphone	VHF	++
Medical Applications	300-900	+++++
Garage Door Opener	UHF	+++

This also can take advantage from the scaling-down of the semiconductor technology below 45 nm. On one hand, the massive usage and availability of these systems/applications on the marketplace (Table 1), bring products to a price consumers can pay for; On the other hand, improving their reliability may considered as the big challenge to face.

2. Wireless Systems Reliability Challenges

The safe and reliable operations of these systems can not be taken for granted. Improving the reliability of electronic systems becomes more and more complex. This is due to their heterogeneity and their density which contains a huge amount of software and deal with a set of varied components (Figure 2) [2,3,7,9,19]. Then, the dependability paradigm becomes a must and considered as the major goal to reach. It presents several types of challenges:

- The FMEA (Failure Mode and Effects Analysis), a well-known method, usually assisted by simulation to check potential errors in integrated circuits. FMEA helps to reduce increasing impacts of life-cycle consequences (risks) from a systems fault; is this method applicable for our target system (Figure 2)?
- We move up to systems which contain real heterogeneous hardware, software, mixed RF, and wireless components, described and implemented at different abstraction levels; then the identification and analysis of the impact of threats becomes a multifaceted task of development,
- Short range wireless systems are more and more used under harsh environmental conditions; then, how can we explore the impact of the environment on the design reliability?
- When we talk about reliable systems, we will need an effective way to discuss defective or incorrect behavior,
- Safety attribute in dependable systems is a large research subject by itself. Then, how it can be approved besides the pure functionality, that also the proper behavior concerning the relevant security attributes is achieved
- Guarantee the design dependability on progressively more complex wireless system is not only complicated, but it bring us to a difficult task that explore the entire embedded sub-systems, digital design, analog design, and wireless design (Figure 2).

One of the major challenges addressed in this paper is to investigate the dependability, among which reliability, in wireless embedded systems, and explore the difficulty of analysis such heterogeneous components-based system. We first present a hardware platform-based design approach as the most attractive solution for dependability study. Unlike the simulation-based approach, this platform-based framework allows to analyze the dependability of the system in a real environment with direct design verification at the desired cycle accurate level, with a real time execution. In this work dependability refers mainly to reliability, and the safety of the system. In Figure 1 we show the block diagram of a typical wireless system.

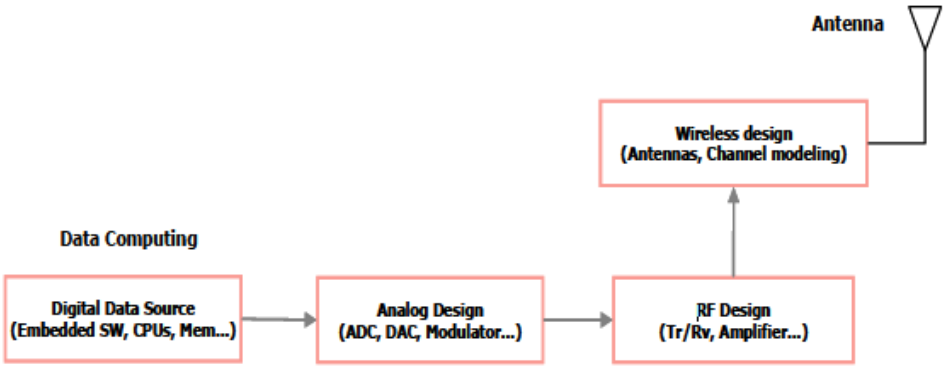

Figure 1. Wireless System Architecture block diagram

In compliance with the generic definition given in [2], if one summarizes the definition of the dependability/reliability as the correct running of the system during the whole operating process, taking into account the presence of exceptional inputs or stressful environmental conditions, one can say that nowadays wireless electronic systems are more and more vulnerable. This is due to their heterogeneity and their density. They contain a huge amount of software and deal with a set of mixed components. Therefore, the sources of derivation of such systems are various:

- Unanticipated communication between the digital data source and the analog Transmitter/Receiver,
- Agressions from outsider environnemental conditions,
- Faults within the complex software embedded in these systems,
- Improve ElectroMagnetic Compatibility (EMC) on the wireless data link,
- In the case of using a predesigned COTS (Commercial off-the-shelf), how to improve their dependability inside the system being designed,
- Design must meet FCC (Federal Communications Commission) requirements.

As we said earlier, behind these short range radio applications a real complex HW/SW architecture is built, usually referred to wireless SoC (System on Chip). Figure 2 illustrates the internal architecture of such system.

Thus, dependability investigation and fault tolerance of the whole embedded wireless system becomes a complicated equation, which involves several dependability stages (digital, analog, wireless). One will not be able to talk about the wireless part dependability without pointing out the other dependability parts. After that, the dependability of the whole wireless systems can be represented as a function that depends on the dependability of the three parts of the system, as fellow:

$$D_{ws} = f\left(D_{DP}, D_{AP}, D_{WL}\right)$$

D_{WS}: Dependability of whole Wireless System

D_{DP}: Dependability of Digital Part
D_{AP}: Dependability of the Analog/RF Part
D_{WL}: Dependability of the Wireless Links.

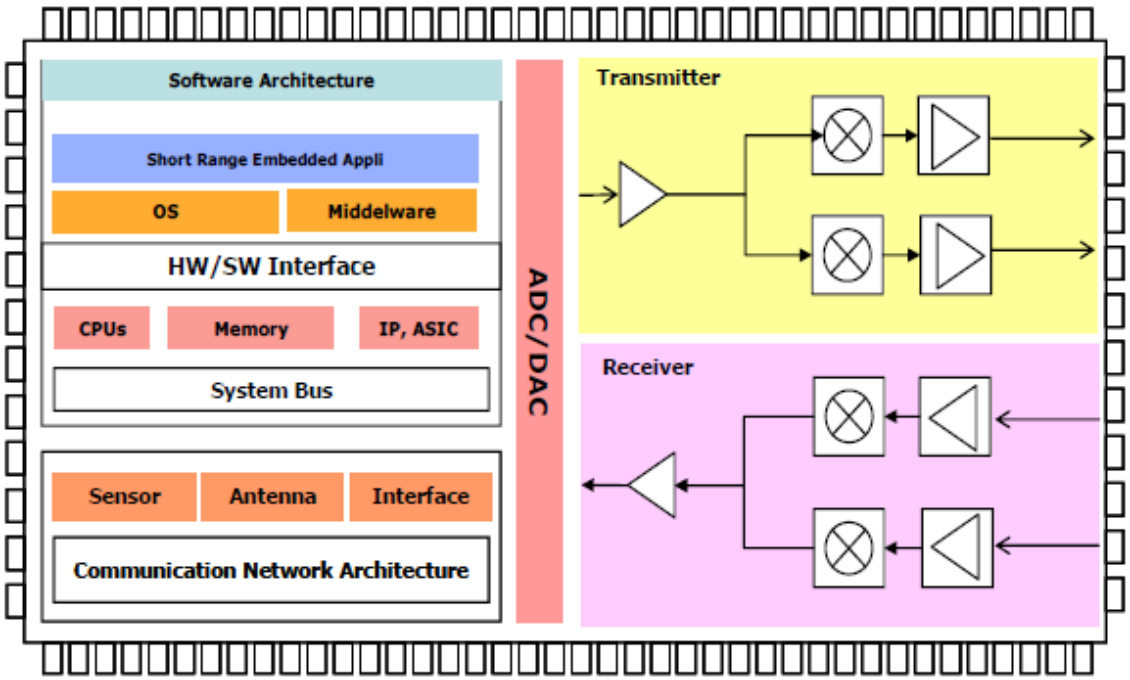

Figure 2. Internal Architecture of Wireless SoC (digital, analog, and mixed signal IPs)

The major question that we are addressing in this paper is: **can one really built such a reliable wireless system or prove that an embedded short range wireless system is reliable?**

To meet this big challenge, it is mandatory to analyze the wireless system as a set of sub-systems described at different levels, and then one requires:

- An effective dependability design methodology/flow and tools to assume the system checking of the heterogeneous components at the different level of the design,
- New electronic dependability automation tools flow analyzing processes,
- and, a real teamwork effort between embedded SW designers, HW designers, mixed signal designers, wireless networking, and power management experts.

The paper is organized as follows; first in section 1 and 2, short range wireless system dependability challenges are presented. Section 3 presents the state of the art and some related works. Section 4 presents the dependability framework. Section 5 introduces the hardware platform-based concept. Also, it gives an insight with regard to the wireless hardware platform built for dependability purposes, and details the implementation. Section 6 describes the dependability flow for embedded wireless systems. Some results and analysis are provided in section 7, while section 8 concludes the paper.

3. Approaches and Related Works

The general state-of-the-art methods that perform reliability analysis is based on the FMEA (Failure Mode and Effects Analysis), assembling data from the circuit system (e.g. statistical data of crashes) and performing analysis of the affected component. However wireless embedded circuits nowadays combine a high number of heterogeneous components such that the previous FMEA method is not be applicable. In related works and to our knowledge, the known methods for dependability investigation (e.g. FMEA) presents a lack of automation, fullness, and specification respecting the full wireless embedded systems analysis. Very few research studies have been reported in this subject.

Actually, there is no scientific method capable to estimate the dependability/reliability of the whole complex wireless embedded system of the different design levels. This paper is most likely the first step in this direction, although they have been several works suggesting such need in general.

In [4] Mariani presents a systematic platform-based approach for a fault-robust embedded SoC, including a design and validation methodology; in this work authors focus on the hardware parts of the integrated system. In [12] the authors present architecture to evaluate the reliability of a SoC; they propose to integrate an autonomic layer into the SoC to detect the chip's current condition and instruct appropriate countermeasures. This approach is performed at one specific abstraction level.

A.Albinet [11] proposes a practical approach to benchmarking the robustness of embedded operating systems (Linux as open source) with respect to faulty device drivers. In order to facilitate the conduct of fault injection experiments, they introduce the notion of the Driver Programming Interface (DPI) that precisely identifies the interface between the drivers and the kernel, in the form of a specific programming level (set of low level software functions). In [8], authors also care about the embedded operating system level and discuss its reliability. In these works a simulation approach is used, authors pay attention mostly to the control side of the embedded system (embedded OS).

In Table 2 we show a summary comparison, in terms of speed and complexity, between two techniques, hardware platform based design and co-simulation technique, used for reliability study of wireless embedded systems [1,13].

Table 2. PLATFORM BASED & CO-SIMULATION FOR DEPENDABILITY INVESTIGATION

	Speed	Complexity	Characteristics
Platform Based	Equal to SoC speed	+++	Close to the final Implementation
Co-Simulation Based	Very slow (RTL level)	+++++	Bottleneck to Simulate Envirenment threats

In overall, most of the techniques used for wireless embedded system dependability study are based on co-simulation practice, using software components models and mathematical equations for channel modulation (e.g. SRD Design Studio, Matlab/Simulink based model). In such techniques many hypotheses on the reliability of the system are made early in the design process, and have to be verified in a tardy stage of the design process (testing phase in real environment). If one or more of the assumptions is incorrect, it outcome a significant re-design and debug overtime as compared to the initial expected design time. Another ignored factor, there is a risk that these shortcomings will be missed the time-to-market of the product, and lead to displeased customers. Simulation-based techniques raise at least three or four inconveniences:

- A time consuming technique (very slow)
- Very hard to enable a co-simulation in the case of heterogeneous components (e.g.: RF components with digital ones),
- Presents a real bottleneck for environmental threats examination, since there is no existing software tool/platform to study the effect of the environment threats on the wireless links in the embedded system/application being designed,
- Furthermore, it can be very difficult or even impossible to analyse the reliability in some cases (e.g. in the case of Electromagnetic Compatibility perspective).

4. Dependability Framework

In wireless systems reliability investigation, one can discuss all the details about performance, design. and fault tolerance …etc. But it is necessary to adopt a global top-down methodology that investigates the dependability of the wireless embedded system as sub-systems/components as well as the interfacing between these components. The system architecture has to be divided into sub-systems and then probably a roadmap should first be roll out.

Also, previously mentioned, working on dependability issues of short range wireless application should be a coordinated effort between a numbers of experts (embedded SW designers, HW designers, mixed signal …etc). The methodology described in this paper is a process for performing and analyzing dependability of the whole embedded wireless system. It is based on a hardware platform approach. Two main steps are defined in our methodology:

4.1. Building the Wireless Platform

The first and most crucial step is to build the wireless platform. For that purpose, several instances were used of the new SmartFusion devices provided by MicroSemi (Actel) [5]. The wireless hardware platform is defined as a several reconfigurable instances connected with each other wirelessly. Afterward, the designer selects a set of these components to build his wireless embedded system. Two main structural designs are specified in the wireless platform, on-chip structural design and off-chip structural design.

Details about the two parts are given below. Such hardware platform enables the investigation of the reliability of the wireless application by analyzing the different components of the system separately, and at different abstraction level. It is now also possible to test the circuit/application in an environment very close to the final one, taking into account the operational conditions (where the system will be used). This wireless platform is the best alternative for the time consuming co-simulation approach.

4.2. Defining a Global Dependability Approach Based on This Platform

The methodology described in this paper is a method for performing and analyzing dependability of the whole embedded wireless system. It is based on a wireless hardware platform. The basic idea of the dependability framework presented in this work, is to develop several tightly coupled peripherals (dependability mechanisms) to manage and verify the wireless system based components at the different level of the design, digital, analog, and wireless. At digital design level, for example, these dependability mechanisms implemented in SW (C code) for the software side of the digital part, or HW (HDL) for the hardware side, will check and supervise the booting of the OS, the context switching, and the interrupt controller, also all the part of the system that have been implemented in hardware (HW IP). The specification and the implementation of these dependability mechanisms is strongly based on the IEC 61508 international norms requirements, integrated SoC design rules, also set of laws from test-benchs design are used.

5. Wireless Platform Overview: SmartFusion FPGA

FPGA fabrics with heterogeneous components are emerging in the industry, either for data processing application such as (audio codec, video encoder) or for communication applications such as client-server. The Microsemi (Actel) SmartFusion [5] and Xilinx Zynq family [15] boards are examples of these FPGA fabrics. These HW devices are considered to be the future of embedded systems design and validation [13].

SmartFusion device is a mixed-signal FPGA, and so far the only, device that integrates on the same chip programmable analog blocks (for mixed signal development), a set of logic gates (for HW IPs development), CPU-ARM Cortex-M3 processor (for digital design development),

and a set of communication connectors [5]. These characteristics make this device very appropriate for wireless applications development. So, we used several instance of this FPGA device to build a wireless platform. In this platform concept, the SmartFusion FPGA instance exchange data via wireless channels using antennas. We distinguish two main parts in the wireless platform, the on-chip structural architecture and the off-chip structural architecture. Figure 3 shows a global view of the wireless platform. The different "Mote: Mobile Note" of the platform communicate wirelessly via an antennas.

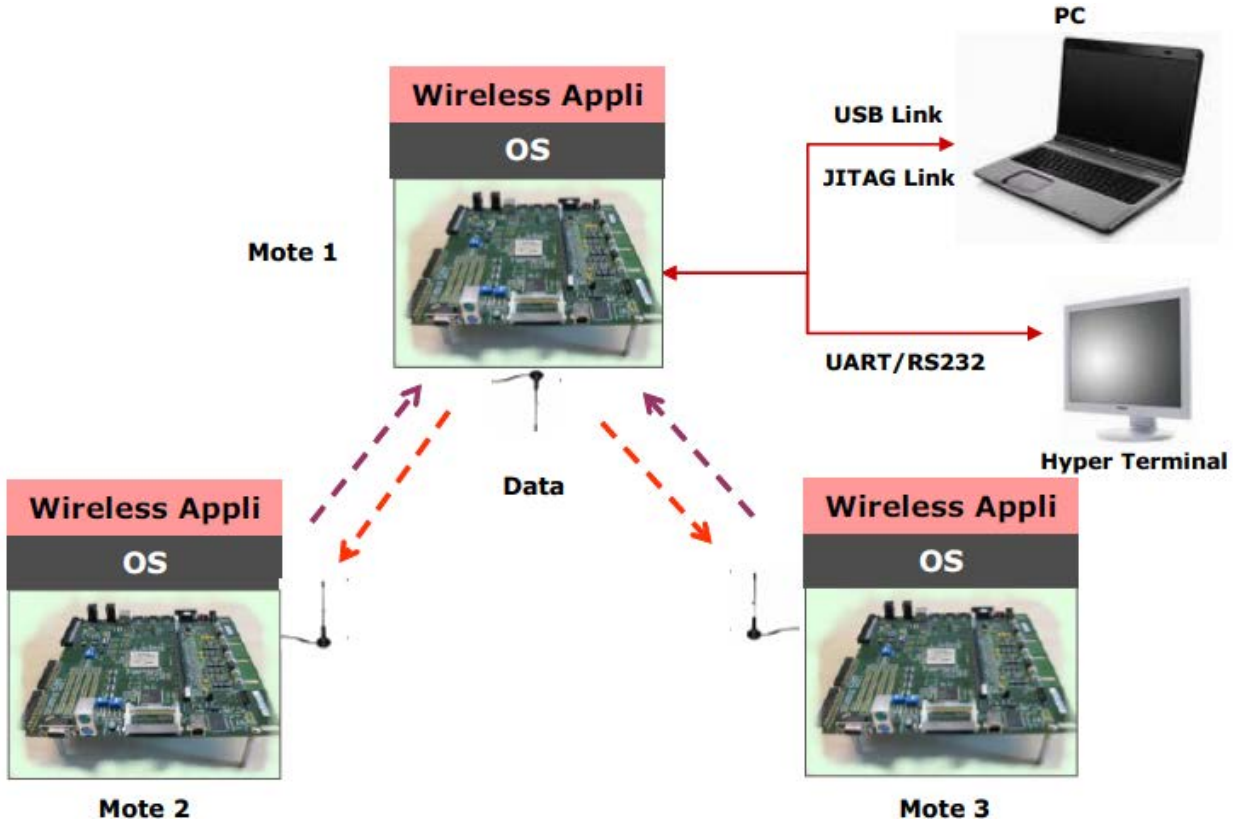

Figure 3. Wireless Platform based on SmartFusion Mixed Signal Device

5.1. On-chip Structural Design

The On-chip structural design of the wireless platform is composed of: an embedded architecture fully built inside the FPGA device, software control running on the ARM CortexM3 based architecture, and the analog modules.

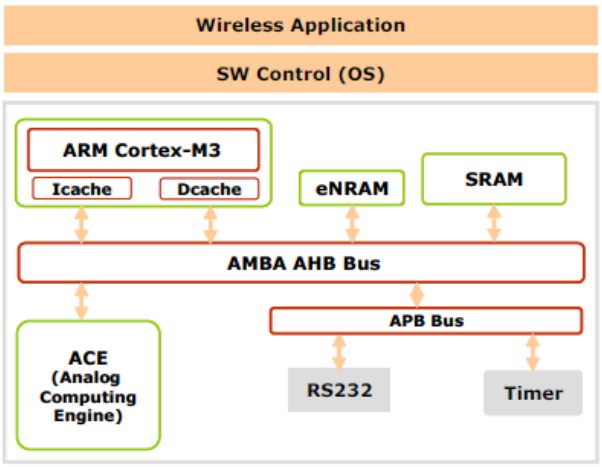

Figure 4. CortexM3 based architecture

- A digital HW/SW on-chip architecture was built based on the ARM-CortexM3 CPU as shown in Figure 4. The CortexM3 CPU is connected to a local booting memory (eNVM: embedded Non Volatile Memory) and a high speed data memory (SRAM) via an AMBA high performance system bus (AHB).
- The software digital part is mainly built around an embedded Operating System (FreeRTOS) as a software control that manages the execution of the software tasks on the target digital architecture. It sends the computing data off-chip via the analog mixed signal architecture.
- Also, the analog part embedded in the on-chip architecture it is designed around the Analog Computing Engine (ACE) and Analog Frontend (AFE) block. This analog block is connected directly to the rest of the system via a 32-bit wide connection. The block has also its own CPU, called ACE, it is almost a co-processor, which can perform functions such as automatically adjusting the resolution of the ADC (Analog to Digital Converter), initiate an digital-to-analog conversion or vice versa, basing on an active FPGA signal, and stop the Cortex-M3 when a particular event occurs.

5.2. Off-chip Hardware Architecture

Commercial off-the-shelf (COTS) components are designed to be used as black boxes. Integrating such COTS components into a short range wireless application, that involves high dependability requirements; may be mismatches between the failure assumptions of these

components and the rest of the system. For resolving these mismatches, system integrators must rely on methodologies that allow for the COTS hardware or software components. Even if the COTS blocks are delivered with deeper knowledge about their failure modes, dependability degree, and its behavior in the presence of faults, it still presents a real bottleneck.

The SmartFusion instances are connected via wireless links using antennas. This antenna is adapted via a USB connection in order to send data from one platform device (on chip architecture) to another one. In this stage of the wireless platform design, we used a COTS (Commercial off the Shelf) predesigned component. A task adaptation between the integrated COTS and the other parts of the architecture design (on-chip architecture) is performed. COTS dependability is a research subject by itself [6], we are focusing on the dependability of the adaptation interface between it and the rest of the architecture.

6. Global Dependability Approach

As we mentioned in related works, the known methods (e.g. FMEA) present a lack of automation, fullness and specification respecting the full wireless embedded systems analysis.

To break these barriers, it is mandatory to analyze the integrated circuit as a set of sub-systems described at different levels, using a dependability automation analyzing processes. And then, methodologies related to reliability and availability will be included.

The methodology described in this paper is a global method for performing and analyzing dependability of the whole embedded wireless system. It is based on a hardware approach.

The basic idea of the dependability framework is to have several tightly coupled hardware and software peripherals (dependability mechanism) to manage and verify wireless SoC based components at functional level. At OS level, for example, these dependability mechanisms implemented in SW will check and supervise the booting of the OS, the context switch and the interrupt controller.

As a first step of our work we focus in preparing the hardware prototyping platform as an alternative for the co-simulation technique.

Figure 5 summarizes the dependability framework using the wireless hardware platform approach. In such dependability paradigm, the system's components at hand are defined separately, at different abstraction levels (RTL, physical, or CMOS level) and with different specification languages (C, HDL). Then, the proposed methodology takes care of this issue by investigating the dependability at the several levels of the design by the use of dependability components described at the same level of abstraction as each component of the design. The shaded part of the flow (Figure 2) presents the part in which we are interested in. It's presents the HW/SW design (digital part) for dependability as one sub-system of the whole wireless embedded system.

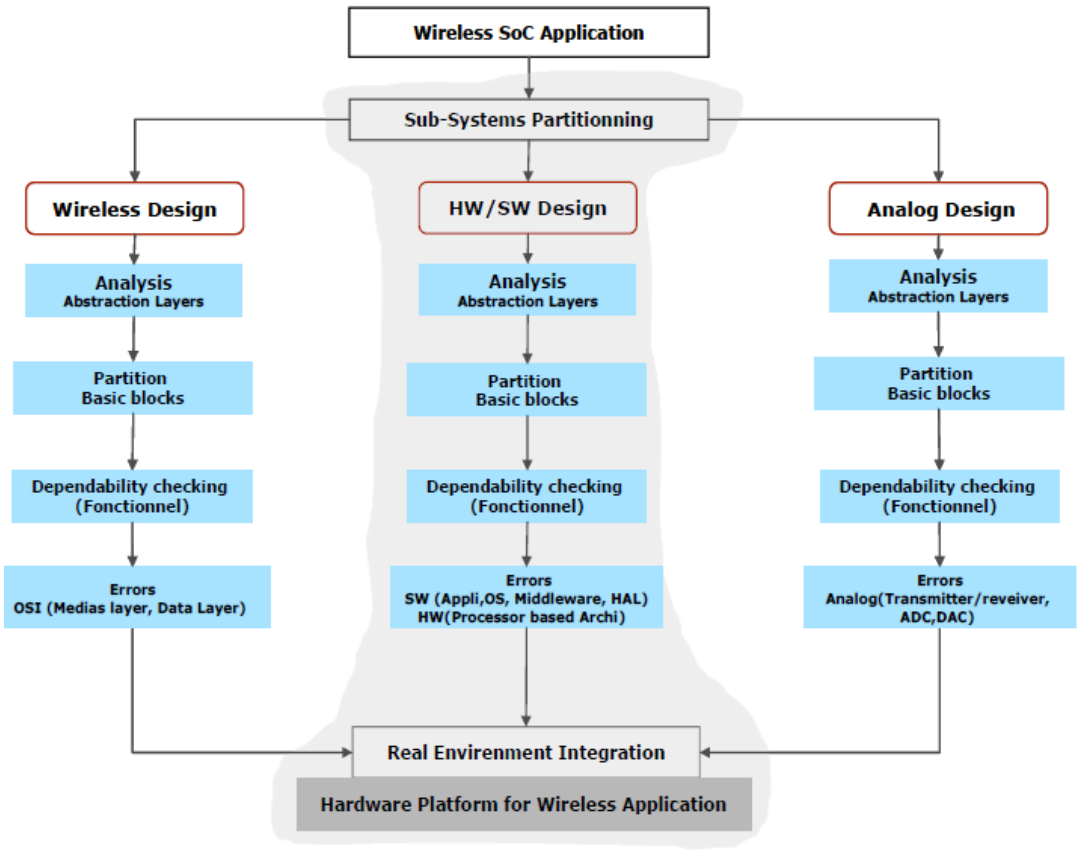

Figure 5. Dependability framework

The proposed method includes three steps of dependability investigation, wireless design, HW/SW design (or digital design), and analog design. In the first stage we extract information from the wireless SoC description, by partitioning it in sub-systems with basic building blocks (or functions). Partitioning means that these sub-systems shall be

maintained with respect to their purpose (wireless, digital, or analog design), while "basic blocks" means that they shall be the smallest significant division of function at such sub-system abstraction level.

As a result of that, the dependability flow covers the different sub-systems: wireless, digital, and analog part (block diagrams, RTL level, channel link level and CMOS components).

Another step in the methodology consists in extracting the usage profile and information of such basic blocks under a given specification. In a third stage, the information and usage profile are used to prepare a dependability library database: this library database is accomplished by entering information related both to the wireless safety specifications of the target application, the guidelines of the IEC 61508 norm, and the FCC (Federal Communications Commission) requirements.

At the end of this step, threats (errors) charge of the several sub-system's building blocks of the embedded system are computed, susceptible errors are ranked from the less to the most critical one. It includes specific indices required by the IEC 61508 norm for an eventual SIL (Safety Integrity Level) classification. In the last stage, a real time execution is carried out within the hardware platform; the measured results are collected from this first execution, in particular the information provided by the system wireless communication, is verified. Then the results are compared with the previous execution results, and in case of disparity, indications are given in order to correct the next exploration feedback.

One of the benefits of this direct execution is to accelerate the errors exploration process, and gives us enumerated information about the reliability and availability of the system being designed. The methodology described in this paper is a method for performing and analyzing dependability of the whole embedded wireless system (Figure 6). It is based on a mixed HW/SW approach. There are a number of factors that need to be considered to determine the best process.

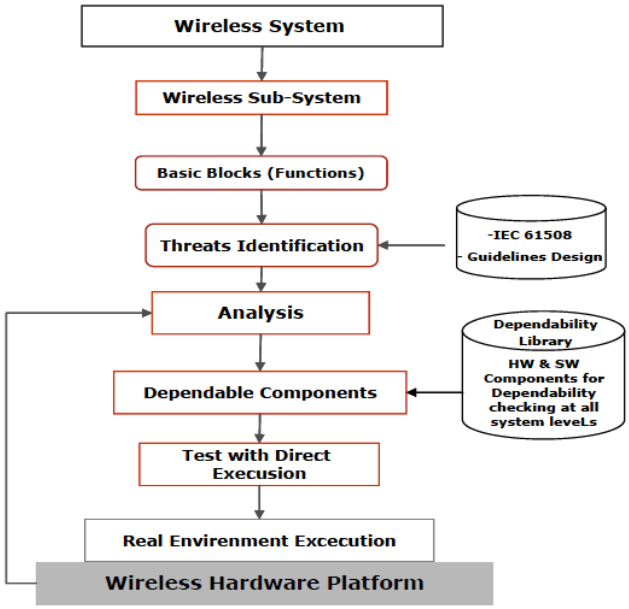

Figure 6. Dependability flow

It is considered that the most important feature is the investigation of the whole system dependability at different abstraction levels of the design, SW, digital, analog, and wireless.

In such dependability a paradigm, the components of the system at hand are defined separately, at different abstraction levels (transactional, RTL or transistor level) and with different specification languages (C, HDL). Then, the proposed methodology takes care of this issue by investigating the dependability at several levels of the design by the use of dependability components described at the same level of abstraction as each component of the design.

One can defines these dependable components (or dependability mechanism) as tightly coupled hardware and software peripherals run during the run time execution of the wireless system on the hardware wireless platform, in order to manage and verify the system's components at functional level. Hence, the following three main stages of dependability investigation are planned in our methodology:

- Dependability exploration within the HW/SW digital part
- Dependability exploration within the analog/RF part
- Dependability exploration within the Wireless part

As a result of that, the dependability flow covers the different sub-systems: wireless, digital, and analog part (block diagrams, RTL level, channel link level and transistor level) One can also add one more stages of dependability concerning the integrated COTS in the system being designed.

After partitioning the embedded wireless system to three sub-systems (digital, analog/RF, and wireless parts), in the first stage one extract information from each sub-system by partitioning each sub-system into several basic blocks (HW or SW blocks). Partitioning means that these basic blocks shall be maintained with respect to the abstraction level, and description language.

The next step in the methodology consists of extracting the usage profile and information of such basic blocks under a given specification. In a third stage, the information and usage profile are used to prepare a dependability components (mechanism) library database. This library database is constructed by entering information related to both to the wireless safety specifications of the IEC 61508 norm, and to some of the design guidelines available in the market.

6.1. Dependability Levels for Wireless Embedded Systems

A. HW/SW dependability level

The HW/SW sub-system presents the digital data source. On one side there is the hardware architecture, mainly represented by processor based architecture (not interested in their reliability for now, we used the available hardware architecture, Microblaze or PowerPC based one). On the other side, the embedded software is built around a small operating system (OS) which involves real-time computations for target sensors-based applications.

As we consider the OS as the central part of the embedded software, we have developed a generic software dependability component running at the same time as the software on the wireless hardware platform. We check, during a real time execution, the different SW functions of the OS, with a focus on the low level routines, system

booting system, synchronization, context switch, and kernel initialization. We have used the FreeRTOS operating system [14].

B. Analog dependability level

At this level, dependability library components are written in another level of abstraction (CMOS), at present we assume that checking analog components is carried out separately on another platform (software one) since we used pre-designed hardware blocks provided from the market as a component in which the transmitter/receiver and the wireless antenna are integrated. Hence, at this moment not much effort will be spend on this level.

C. Wireless link dependability level

According to the OSI (Open System Interconnect) communication protocol which consists of five data transfer unit levels (data, segments, packet, frame, and bit), for our reliability flow, and due to abstraction levels facilities provided by the hardware platform approach, the top three layers has been merged into one packet level. The merged approach is adopted in order to make easy the dependability checking and break down the complex task of building the dependability library.

Then, the library components explore the functional and procedural data transfer:

- **Data Packet**: we check the path determination and logical addressing
- **Data frame**: mainly we check the physical addressing on the hardware platform
- **Data bit** (byte): we check the binary transmission between network entities, from digital data source to transmitter, to wireless channel (mote 1), until the destination for the (mote 2).

As a result of that, the dependability flow covers the different sub-systems: wireless, digital, and analog part (block diagrams, RTL level, channel link level and transistor level) One can also add one more stages of dependability concerning the integrated COTS in the system being designed.

After partitioning the embedded wireless system to three sub-systems (digital, analog/RF, and wireless parts), in the first stage one extract information from each sub-system by partitioning each sub-system into several basic blocks (HW or SW blocks). Partitioning means that these basic blocks shall be maintained with respect to the abstraction level, and description language.

The next step in the methodology consists of extracting the usage profile and information of such basic blocks under a given specification. In a third stage, the information and usage profile are used to prepare a dependability components (mechanism) library database. This library database is constructed by entering information related to both to the wireless safety specifications of the IEC 61508 norm, and to some of the design guidelines available in the market.

6.2. Functional Safety and IEC 61508

The IEC 61508 international norms define requirements for dependability/safety of electrical/electronic/programmable electronic related systems [7,10].

Even if these norms not really refer to complete wireless HW/SW embedded systems, they contain some accurate rules and requirements for the system subcomponents. They include CPUs, memory systems, bus network and so on. An extension of such a norm to SoC systems will be appearing soon. The basic concepts of IEC61508 is the definition of safety integrity level (SIL), i.e. the discrete level (one out of a possible four) for specifying the safety integrity requirements of the safety functions to be allocated to the safety-related systems. Safety integrity level 4 has the highest level of safety integrity and safety integrity level 1 has the lowest. This factor concept is taken into account when specifying the different components of the dependability library.

7. Results, Analysis and Future Work

The effort required for the first step to set up the hardware wireless platform based on the SmartFusion devices is three person/months, and this is only for a particular digital/analog configuration. In the case of reuse of the same processor based architecture, this effort could be reduced.

This work allows the investigation of the dependability/reliability in mixed wireless systems context, as the first step in understanding the complexity of approving the dependability of such systems, which is a multifaceted problem. Our current steps have shown that the usage of hardware platform for embedded wireless short-range radio application reliability study is the most attractive approach in comparison with the time-consuming co-simulation approach. It allows the analysis of the heterogeneous parts of the wireless systems (digital data source, wireless and analog part) by verifying the system at the different design levels.

This wireless hardware platform is an important step toward a seamless dependability study of complex embedded wireless systems/applications. The goal behind the proposed approach is to build a dependability library database of reusable components on the road to help the designers to verify and approve the dependability of the system being designed, in an environment close to the real operational conditions.

One of the most difficult steps in building the wireless platform is the bridging between the instances of the SmartFusion devices, which bring us to bridge the digital and analog part (which is on the same chip in this case) with the off-chip architecture (transmitter/receiver, antenna).

Building this wireless platform in the context of the design, re-configuration and reuse, allows the validation and verification of the dependability of several wireless applications on the same hardware platform.

Our basic motivation is to build pre-designed HW and SW components that can check the reliability of the different basic blocks of the system, and give us numeric information to improve the dependability of the system at functional level. These dependability components are build up according to the international safety/reliability standards (IEC 61508) and the guidelines usually used in circuits design. In fact to reach and built these library components for all the abstraction levels and for the general case is very hard and may be not a realistic goal, in proportion to the large heterogeneity of the applications.

In our dependability platform, the embedded software is built around the open source FreeRTOS Operating System, and a wireless application. For now, the wireless application

is represented by small benchmarks that allow several functions to exchange data wirelessly.

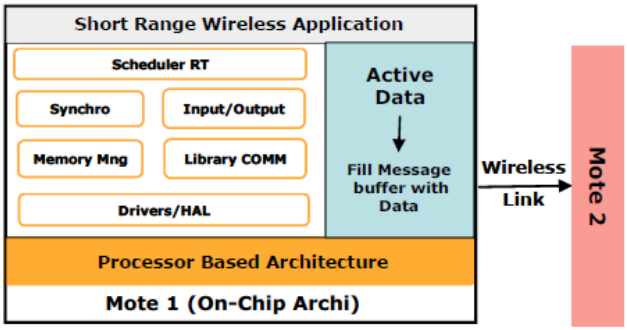

Figure 7. Embedded SW Architecture

FreeRTOS is an open source, highly portable, multi-tasking operating system for memory-efficient networked embedded systems and wireless networks. FreeRTOS has been ported on the several instances of the platform devices (SmartFusion FPGA). The FreeRTOS manage the execution of the software functions on the CPU and the interruption handlers. The CPU based architecture is built around a general purpose embedded processor (ARM Coretx M3) and memories. The FreeRTOS configuration is about 8 kilobytes of RAM. Figure 7 shows the embedded SW architecture.

The wireless application that runs on the ARM Cortex M3 processor computes the waveform sample values. The ACE SSE registers are addressable and accessible from the ARM Cortex-M3 processor. The ARM Cortex-M3 processor writes the computed data value to the DAC register and this updates the 1-bit DAC output accordingly.

Then, this digital architecture sends data for the analog part (transmitter/receiver) in order to drive it for the destination (Mote 2) via an antenna. During this design step we identify the threats (both for HW or SW based architecture) and do an analysis using these dependability library components, with direct feedback execution on the platform until eliminate all the possible errors.

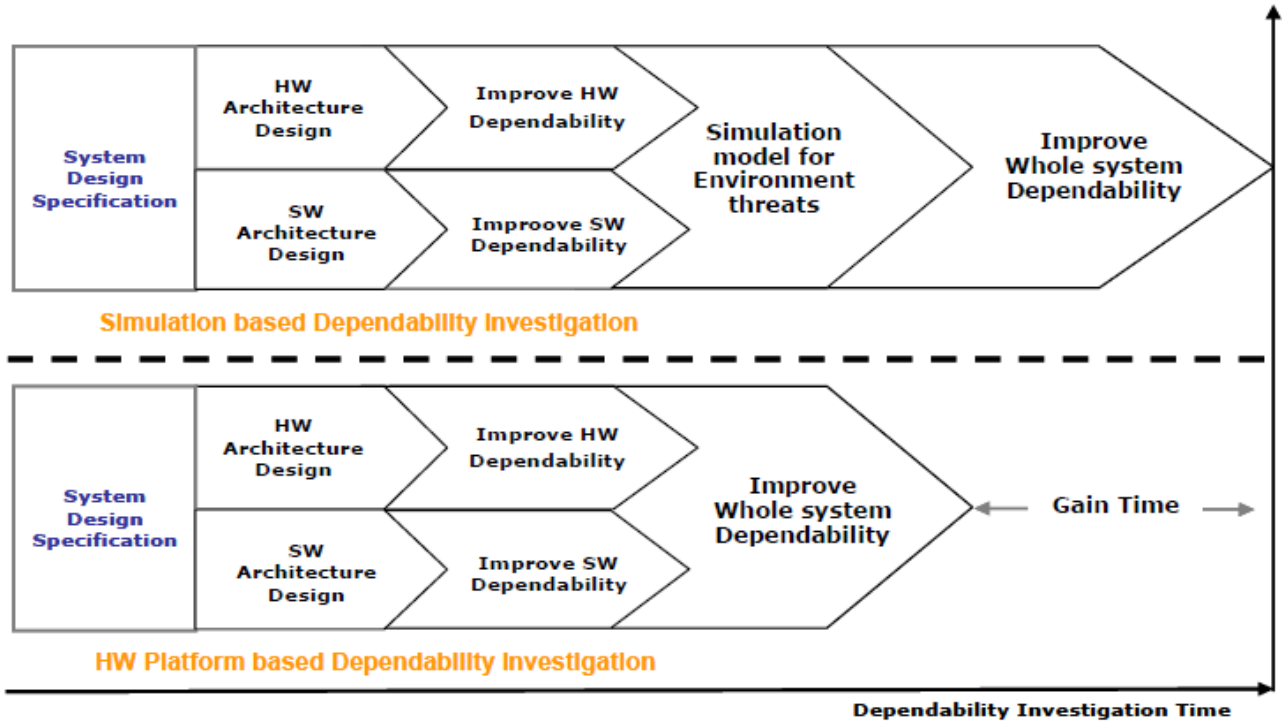

Figure 8. Wireless platform & Co-Simulation for Reliability investigation: Gain Time

The use of a hardware platform approach for short range embedded wireless systems dependability investigation, allows the analysis of the different design levels of the wireless systems (digital, wireless and analog) by check the reliability of the design in a real execution environment.

The critical step in building the platform is the bridging between the platform's Motes using these COTS wireless components and develops the dependable adapter interface for them.

The effort needed for this first step to set the digital part (on-chip architecture) is estimated to be two months, and this is only for a particular on-chip configuration. For following wireless application dependability study the effort should be considerably reduced, thanks to the reuse of the pre-designed components. In Figure 8 we show the gain time using the hardware platform to investigate the dependability in comparison with a co-simulation technique, where step which consist to develop a simulation model for the environment threats is added.

The reconfigurable platform based dependability design reuse in the context of wireless short range application reliability was the motivation for us to consider a dependability library of pre-designed HW and SW components that check reliability parameters at the different abstraction layers of the wireless system, according to the excited international reliability standards (ex: IEC 61508). In fact, in proportion to the large heterogeneity of the short range wireless applications/architectures, we believe that to reach and built these library components for the general case is very hard and may be not a realistic goal.

The major benefits in short range wireless systems dependability investigation will be reached if the time of the investigation is reduced, since design for reliability at all the abstraction levels is a really time-consuming. This

is why a hardware platform-based dependability investigation technique is more appropriate then a co-simulation one. The reusability/reconfigurability of this platform allows also covering a large number of short range wireless applications. Such flexible platform give us the possibility in the near future to investigate the EM (Electromagnetic field failures) on these short range radio within a reverberation room as a part of the research project.

8. Conclusion

This paper deals with the dependability/reliability analysis in short range wireless embedded systems.

For this purpose, we firstly and successfully built a hardware wireless platform. The platform is built using several instances of one of the commercial FPGA platform available on the market (SmartFusion). Secondly, based on this platform we introduced a new methodology and a flow to investigate the different parts of the wireless system dependability. The goal behind the proposed approach is to build a dependability library database of reusable components on the road to help the designers to verify and approve the reliability of the system being designed. The hardware approach presented in this paper for dependability study, gives the designers another alternative then the time consuming co-simulation technique, to check the reliability of the systems.

The goal behind the construction of the wireless hardware platform is to help the designers to verify and approve the reliability of the system being designed in an environment very close to the real application settings. Based on the platform a new dependability flow/methodology was introduced to facilitate the reliability verification in complex short-range wireless systems, taking into account the different parts of the system: embedded SW, digital part, analog/RF part, and the wireless link part.

References

[1] A.Sangiovanni-Vincentelli and all “Benefits and Challenges for Platform-Based Design,” Design Automation Conference (DAC), 2004, pp. 409-414.

[2] Avizienis, A; Laprie, J.-C.; Randell, B.; Landwehr, C. “Basic concepts and taxonomy of dependable and secure computing” IEEE Transactions on Dependable and Secure Computing, Issue Date: Jan.-March 2004, Volume: 1 Issue:1 On page(s): 11-33.

[3] H.G Kerkhoff, X.Zhang “Design of an Infrastructural IP Dependability Manager for a Dependable Reconfigurable Many-Core Processor” Proceedings of the 2010 Fifth IEEE International Symposium on Electronic Design, Test & Application, Pages: 270-275.

[4] R.Mariani, S.Ulmiano “A Platform-Based Technology for Fault-Robust SoC Design” Design and Reuse SoC conference 2007.

[5] http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion

[6] Alan Bensky “Short-range wireless communication: Fundamental of RF system Design and Application” 2005.

[7] Functional safety and IEC 61508, September 2005.

[8] Francis M.David, and all “Improving Dependability by Revisiting Operating System Design” HotDep'07: Proceedings of the 3rd workshop on on Hot Topics in System Dependability (2007).

[9] Edmond, Gupta, Siewiorek, Brennan “ASSURE: automated design for dependability," pp.555-560, 27th ACM/IEEE Design Automation Conference (DAC '90).

[10] Riccardo Mariani and all “Applying IEC 61508 to Integrated Circuits” Volume 6, Number 2, 2007.

[11] Arnaud Albinet, Jean Arlat, Jean-Charles Fabre “Chapter 14. Benchmarking the Impact of Faulty Drivers: Application to the Linux Kernel” Dependability Benchmarking for Computer Systems Published Online: 7 JAN 2008.

[12] Andreas Bernauer and all ‘An Architecture for Runtime Evaluation of SoC Reliability’ In INFORMATIK 2006 - Informatik für Menschen, Lecture Notes in Informatics, Köllen Verlag, vol. P-93 of GI-Edition.

[13] B.Senouci, A.Bouchhima, F.Rousseau, F.Petrot, A.Jerraya, “Fast prototyping Methodology of Distributed SoC applications on a Multiprocessor Hardware Platform", IEEE Distributed Systems Online, vol. 8, no. 5, 2007, art. No. 0705-o5002.

[14] http://www.freertos.org/.

[15] http://www.xilinx.com/.

[16] Stefan Lindenmeier, Anestis Terzis “A DSSS-Based Wireless Short Range Data-Link Original Research Article AEU” - International Journal of Electronics and Communications, Volume 57, Issue 3, 2003, Pages 161-167.

[17] Clive Pygott, Stephen P. Wilson “Justifying reliability claims for a fault-detecting parallel architecture” Journal of Systems Architecture, Volume 43, Issue 10, 1997, Pages 735 751.

[18] Nicola Mazzocca, Stefano Russo, Valeria Vittorini “Formal methods integration for the specification of dependable distributed systems” Journal of Systems Architecture, Volume 43, Issue 10, 1997, Pages 671-685.

[19] K. Masselos, A. Pelkonen, M. Cupak, S. Blionas “Realization of wireless multimedia communication systems on reconfigurable platforms” Journal of Systems Architecture, Volume 49, Issues 4–6, September 2003, Pages 155-175.

[20] K.G.Padmasine, S.Muruganand “System on Chip (PSoC) Control for High Current Magnet Power Supply” Journal of Embedded Systems, 2014, Vol. 2, No. 1,11-14.

[21] Dadashi, M.; Rashid, L.; Pattabiraman, K.; Gopalakrishnan, S., "Hardware-Software Integrated Diagnosis for Intermittent Hardware Faults," Dependable Systems and Networks (DSN), 2014 44th Annual IEEE/IFIP International Conference on, vol., no., pp.363, 374, 23-26 June 2014.