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# Design & Implementation of Low Power 3-bit Flash ADC in 0.18µm CMOS

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**Abstract—This paper describes the design and implementation of a Low Power 3-bit flash Analog to Digital converter (ADC). It includes 7 comparators and one thermometer to binary encoder. It is implemented in 0.18um CMOS Technology. The pre-simulation of ADC is done in T-Spice and post layout simulation is done in Microwind3.1. The response time of the comparator equal to 6.82ns and for Flash ADC as 18.77ns.The Simulated result shows the power consumption in Flash ADC as is 36.273mw .The chip area is for Flash ADC is 1044um$^2$ .**

**Index Terms— CMOS, Comparator , Flash ADC, T-Spice**

## I. INTRODUCTION

Applications such as wireless communications and digital audio and video have created need for cost-effective data converters that will achieve higher speed and resolution. The needs required by digital signal processors [1] continually challenge analog designers to improve and develop new ADC and DAC architectures. There are many different types of architectures, each with unique characteristics and different limitations[2]. Figure.1. shows the general block diagram of ADC.Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Flash ADCs are ideal for applications requiring very large bandwidth; however, they typically consume more power than other ADC architectures and are generally limited to 8-bits resolution.

## II. ARCHITECTURE

Fig.2. shows a typical flash ADC block diagram. For an "N" bit converter, the circuit employs $2^{N-1}$ comparators. A resistive divider with $2^N$ resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a "1" when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator in Fig.3.output is "0". Comparatator design specification is shown in Table I. As shown in Fig. 2, the flash ADC is composed of three major components: resistors string,

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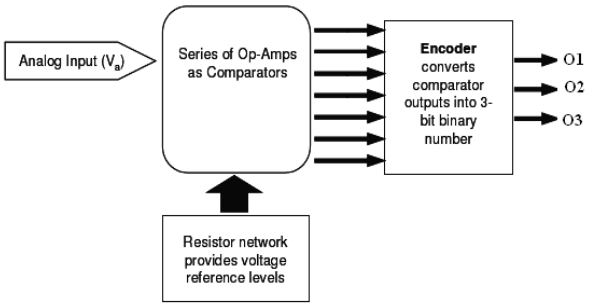


**Fig. 1. Block for 3-Bit Flash ADC**

comparators and encoder. The analog input voltage is concurrently compared to the reference voltage levels generated from resistors string and the speed of A/D conversion is therefore maximized. The outputs of comparators form a thermometer code (TC) which is a combination of a series of zeros and a series of ones, e.g., 000…011…111. Because binary code is usually needed for digital signal processing, a thermometer code is then transformed to a binary code through a ($2_k$-1)-to-k TC-to-BC encoder, where k is the resolution (bits) of ADCs. The cost of such a traditional encoder increases exponentially with the resolution. Optimizations on area cost, circuit latencies an power consumptions are greatly expected. In this paper we have low power Comparator used in the design throughout.

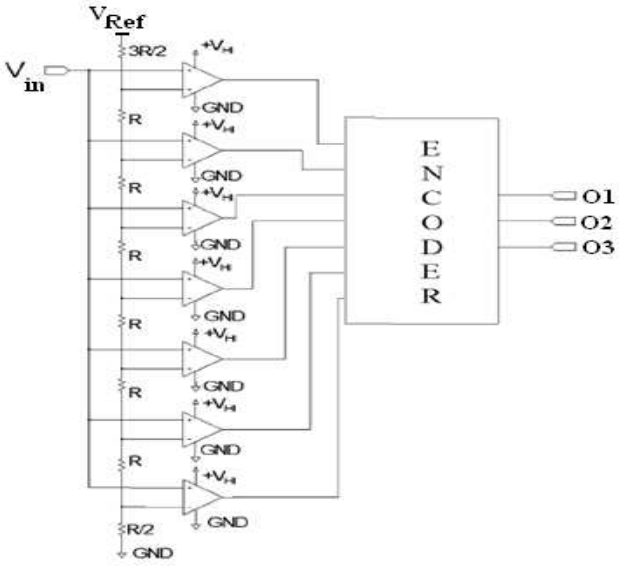


Fig. 2. Circuit for a 3 Bit Flash ADC

A.Comparator Circuit & Design Specification

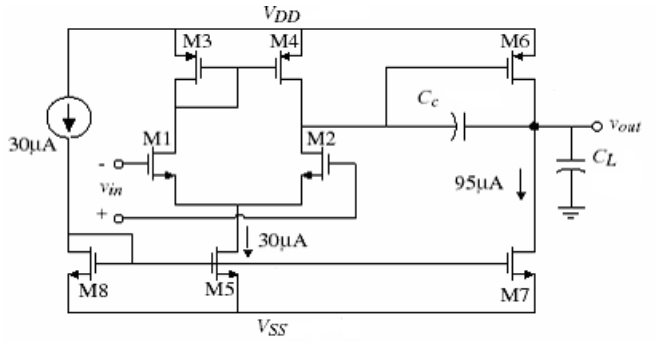


Fig.3. Low power Comparator circuit used in proposed Flash ADC

TABLE I

DESIGN SPECIFICATION FOR COMPARATOR

| | |
|---|---|
| Technology | 0.18u CMOS Technology |
| Supply Voltage | ±1.3V |
| Resolution | 3-bit |
| Voltage Gain | >10000 |
| Slew Rate | 20v/us |
| $C_L$ | 1.25pf |
| Vout Range | ±2.0V |
| Gain Bandwith | 30MH$_Z$ |

B.Thermometer to Binary Encoder Design

Below table II show the two digital codes.This table can be used to design a suitable combinational circuitas as Fig.4.
From the above table using K'map technique below equations are derived.
O1 = C1
O2 = D2 + C1'B1 + B1'A2
O3 = E1D2 + D2'D1 + C1'B1 + A2'A1
Fig. 3 shows the basic schematic for the Low power Comparator which is simulated under the parameters given in the Table I . This low power Comparator is used in the proposed 3 bit Flash ADC design. The Encoder shown in Fig.4 shows the basic construction derived and implementation in Pre-layout & Post-layout Design and Simulation results .

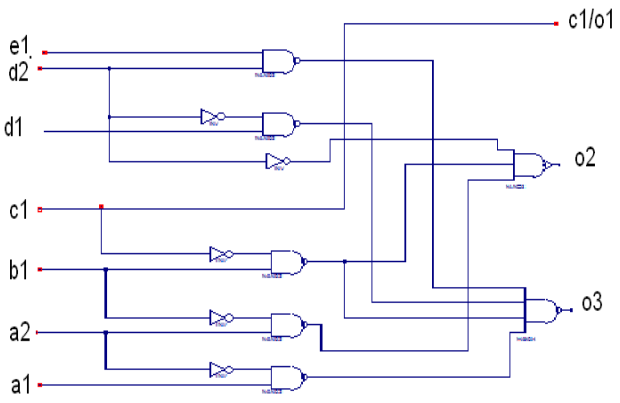


Fig.4. Thermometer to Binary Encoder

TABLE II

TRUTH TABLE FOR THERMOMETER TO BINARY ENCODER

| Thermometer code | | | | | | | Binary Code |
|---|---|---|---|---|---|---|---|
| E1 | D2 | D1 | C1 | B1 | A2 | A1 | O1 O2 O3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 0 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 0 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 1 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 1 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 0 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 0 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 1 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 1 1 |

III. SIMULATION RESULTS

Pre-layout and Post-layout Simulation Results prepared with 220 dpi resolution and saved with no compression, 8 bits per pixel (256 color or grayscale)
A Pre-layout Simulation Results
1.Comparator Output Waveform
As shown in fig.4.sinewave signal is applied to the noninverting terminal of the comparator and reference signal is applied to the inverting terminal of the comparator. We have got the following waveform.

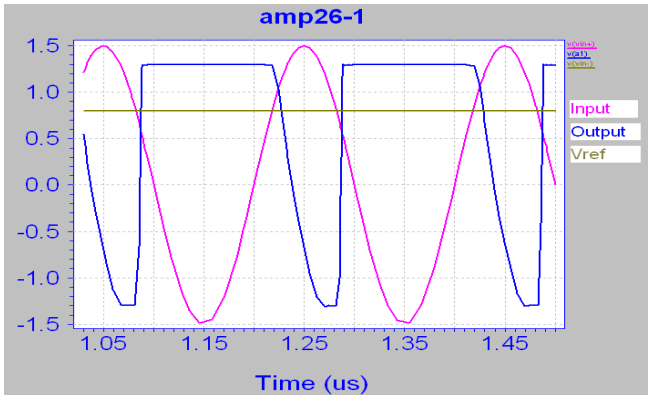


Fig.4. Comparator output

2.Comparator Response Time
We have got the response time of the comparator equal to 6.82ns. Below fig.5.shows the response time of the comparator.

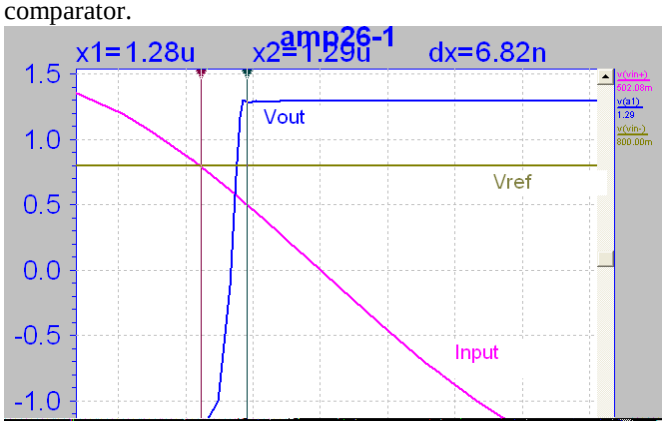


Fig.5. Comparator Response time

3.ADC Output Waveform

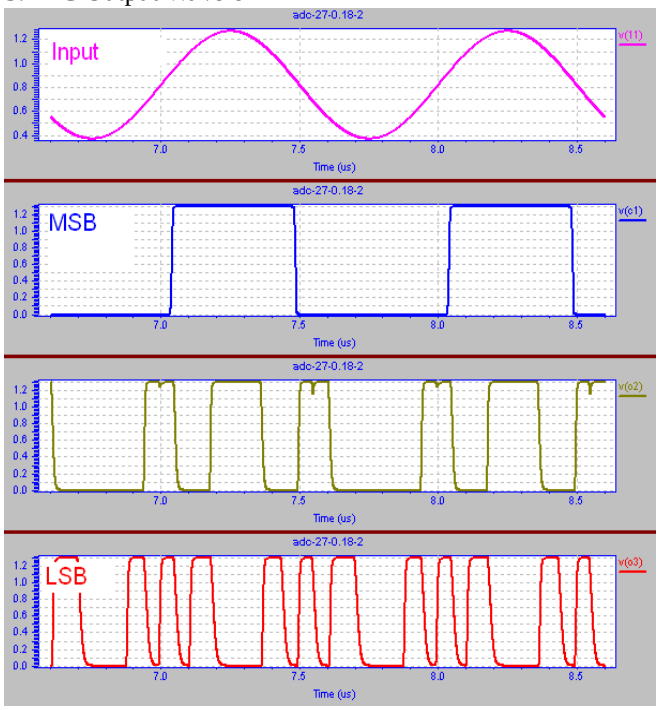


Fig.6. Flash ADC Output

As shown in the Fig.6., as the input signal's amplitude increases output signal in digital format also increses.Here output is swing from 0v to 1.3v.

4.ADC Response Time

We have got the response time of the ADC comparator equal to 18.77ns. Below fig.7 shows the response time of the Flash ADC. Time interval between the instant when a step input is applied and the instant when the output reaches the corresponding logic level (depends on the input step amplitude). One drawback of the submicron CMOS technology is the reduction in the power supply voltage, which results in a reduced signal swing and hence a lower dynamic range. With op-amps and comparators, the fully differential signal paths require fully differential outputs as well as inputs, and they are known as fully differential op-amps and comparators. Since this technique uses symmetrical layout, many of the noise voltages (power supply noise, clock-feedthrough noise, offset voltages) appear as common-mode signals. They are to a considerable extent canceled in the differential output voltage $v_{out}$ at all frequencies.

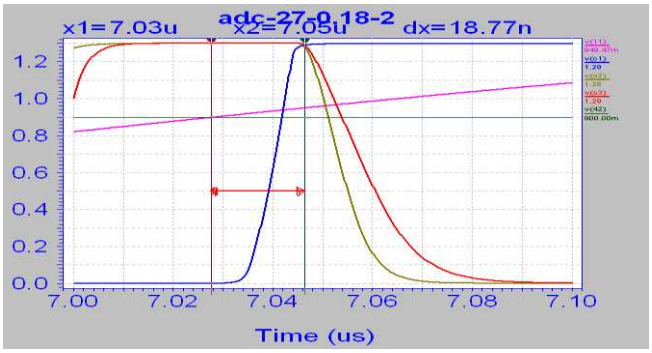


Fig.7. ADC Response Time

B.Post Layout Simulation Results

1.Layout of Comparator

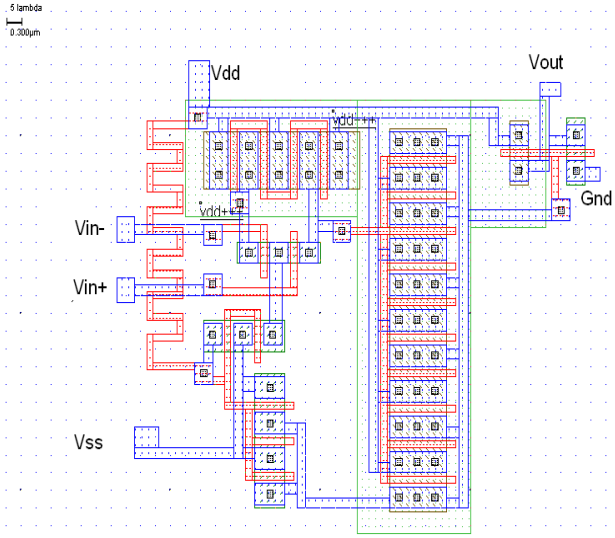


Fig.8. Comparator Layout

2.Layout of ADC

Below fig. 9 shows the basic simplified layout of the complete flash ADC. It includes seven comparators and one thermometer to binary encoder. Most power consumption of the ADC occurs in the comparator as expected. Especially, the comparator's power dissipation is very large as it changes to the higher resolution. Therefore, comparator section is the critical component for low power consumption. It is hard to reduce power consumption in the flash architecture when the comparators are operating. Flash ADC provides fastest conversion rate due to its parallelism. Comparator is the key block for high speed operation. A direct conversion ADC or flash ADC has a bank of comparators sampling the input signal in parallel, which leads to much power consumption as the number of bits increases. Migrating existing designs to a next submicron technology helps to reduce the power consumption significantly. the thermometer output of an A/D converter is usually converted by an encoding circuit to another more compact and useful binary code before being transmitted as data to external circuits.

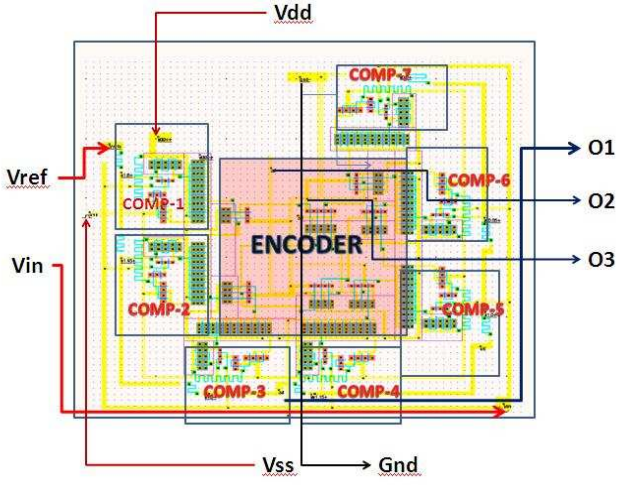


Fig. 9. Simplified Layout of 3 Bit Flash ADC

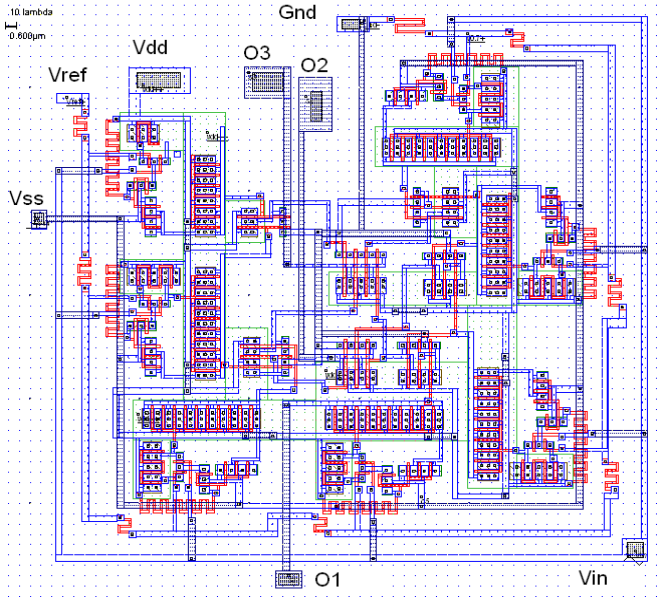


Fig.10. ADC layout

3.Comparator Output Waveform

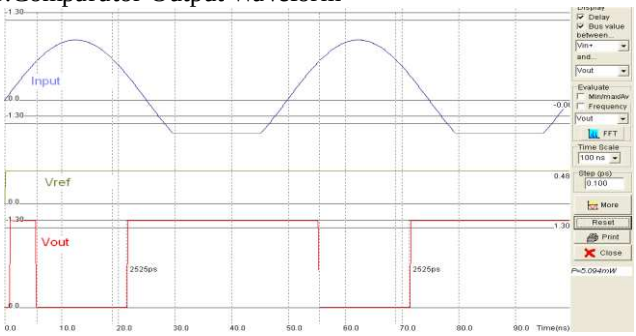


Fig.11. Comparator Output

Above fig.8 and fig.9.layout simulated to have fig10. And 11 shows the output of comparator when the sine wave signal is applied to the non-inverting terminal of the comparator in fig.10.

4. ADC Output Waveform

Below fig.11. shows the output of the 3-bit Flash ADC taken in the microwind3.1. the total power dissipation of the ADC is 36.273 mw. Power dissipation is one of the important characteristic of the Flash ADC. Several techniques for power Savings has been devised by several authors [2]. In this paper the method used for 3 Bit Flash ADC demonstate the use of Low power Comparator in Flash ADC. Also flash ADCs are too costly for high resolutions because their complexity increases exponentially with the number of bits.

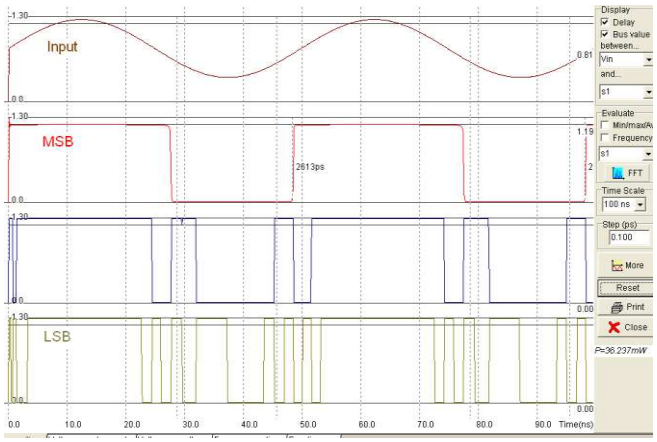


Fig.11. ADC Output

## IV. RESULTS

The 3-bit ADC based on flash type is designed in standard CMOS 0.18 um technology and the simulations are done by using Hspice. The supply voltage is given as 1.3V and the input range is set as 1.5V. The pre-simulation of ADC is done in T-Spice and post layout simulation is done in Microwind3.1.The various aspects of the ADC are summarized in Table III as follows.

TABLE III
SPECIFICATION SUMMARY FOR FLASH ADC

| | |
|---|---|
| Technology | 0 .18um |
| Resolution | 3-bit |
| Power supply | 1.3 v |
| Input Voltage Range | 0 to 1.5V |
| Frequency | 20 MHz |
| Resolution time | 18.77ns |
| Power Dissipation | 36.237mw |
| Chip area | 1044um$^2$ |

## V. CONCLUSIONS AND FUTURE WORKS

In this paper, a 3 Bit flash ADC architecture with low hardware complexity and low latency is proposed.This 3bit flash type Analog to digital converter have limitations such as this device is accurate for the conversion of analog voltage to digital form from 0 to 3 voltage in amplitude and for accurate result the input voltage should be greater or lesser than the reference voltage of the comparator about ± 0.05 volt. Moreover, this architecture can be extended to medium-to-high resolution applications because this simplicity of the circuit.

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