International Journal of Soft Computing and Engineering (IJSCE)
ISSN: 2231-2307, Volume-2, Issue-2, May 2012

An Advanced Online Memory Testing For Fault Diagnostic Systems

Atluri.Jhansi rani, K.Harikishore, Fazal Noor Basha, L.Veera Raju, K.Purnima

Abstract— An increasing part of microelectronic systems is implemented on the basis of pre designed and pre verified modules, so-called cores, which are reused in many instances. Core-providers offer RISC-kernels, embedded memories, DSPs, and many other functions, and built-in self-test is the appropriate method for testing complex systems composed of different cores. The main objective of this project is to designing a system, in such a way that; it is having the capability to detect the faults in the Read only memories. Whether the faults may be Software or Hardware, all faults can be recognized by our designed system. BIST (Built in self test) concept is introduced to detect the faults in the memories. The proposed approach offers a simple test flow and does not require intensive interactions between a BIST controller and a tester. The scheme rests on partitioning of rows and columns of the memory array by employing low cost test logic. It is designed to meet requirements of at-speed test thus enabling detection of timing defects.

Index Terms— DSPs, RISC-Kernels, BIST

I. INTRODUCTION

Embedded memories are more challenging to test and diagnose than their stand-alone counterparts. This is because their complex structures are paired with a reduced bandwidth of test channels resulting in limited accessibility and controllability. Consequently, the memory built-inself-test (MBIST) has established itself as one of the mainstream design for test (DFT) methodologies as it allows one to generate, compress, and store on chip very regular test patterns and expected responses by using a relatively simple test logic. The available input/output channels, moreover, suffice to control built-in self test (BIST) operations, including at-speed testing and detection of timing defects.

Non-volatile memories are among the oldest programmable devices, but continue to have many critical uses. ROM, PROM, EPROM, EEPROM, and flash memories have proved to be very useful in a variety of applications. Traditionally, they were primarily used for long-term data storage, such as look-up tables in multimedia processors or permanent code storage in microprocessors. Due to the high area density and new sub micrometer technologies involving multiple metal layers, ROMs have also gained popularity as a storage solution for low voltage/ low-power designs.

The following Figa shows the salient architectural features of a ROM. Every row consists of M words, each B-bit long. Bits belonging to one word can be either placed one after another or interleaved forming segments, as illustrated in the figure.

Decoders guarantee the proper access to memory cells in either a fast row or a fast column addressing mode, i.e., with row numbers changing faster than word numbers or vice versa. It is worth noting that algorithms proposed in this paper do not impose any constraints on the addressing scheme so that the memory array can be read using either increasing or decreasing address order.

A Generic scan based logic BIST architecture A generic single clock logic BIST architecture based on the well known STUMPS technique is illustrated in Figure 1. The figure depicts the circuit-under-test or core, and the logic BIST controller in the highlighted area. The circuit is composed of combinational logic, and possibly embedded memories, separated by multiple scan chains. Various components of the logic BIST controller are shown in the highlighted area. These components include test pattern generation block - composed of the pseudo-random pattern generator (PRPG) and phase shifter circuit, the output response analysis block - composed of multiple input signature register (MISR), space compactor, and optional AND gates. In addition, there are two counters: the pattern counter, and the shift counter which for each pattern keeps track of the number of cycles required to fill the scan chains.

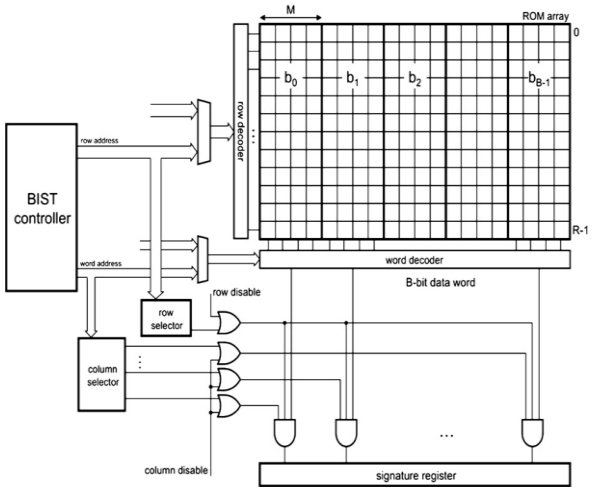


Fig.-1: Schematic Diagram

Manuscript received May 02, 2012.

A. Jhansi Rani, Department of ECE, K L University, Vijayawada, India, 9985799965., (e-mail:Jhansi.atluri@gamil.com).

Prof. K.Harikishore, Asst. Professor, Department of ECE, K L University, Vijayawada, India, (e-mail: Kakarla.harikishore@gmail.com).

Dr. Fazal Noor Basha, Asst. Professor, Department of ECE, K L University, Vijayawada, India,

L.VeeraRaju, Department of ECE, K L University, Vijayawada, India, 9966461747., (e-mail: veera.raju143@gamil.com).

K. Poornima, Department of ECE, K L University, Vijayawada, India. (e-mail: purnima_483@yahoo.co.in)

The decoder block shown in the figure drives the test points. Finally, the multiplexers between the phase shifter and scan inputs are used to concatenate several shallow BIST-mode scan chains into a few deep ATPG-mode scan chains accessed directly from the chip pins in case top-up ATPG is use to improve the fault coverage obtained by BIST.

The schematic diagram summarizes the architecture of a test environment used to collect diagnostic data from the ROM arrays. In addition to a BIST controller, it consists of two modules and gating logic that allow selective observation of rows and columns, respectively. Assuming permanent failures, the BIST controller sweeps through all ROM addresses repeatedly while the row and column selectors decide which data arriving from the memory rows and/or columns is actually observed by the signature register. Depending on a test scenario, test responses are collected in one of the following test modes.

1. Row disable = 0 and column disable = 1; the row selector may enable all bits of the currently received word, thereby selecting a given row; this mode is used to diagnose row failures and, in some cases, single cell faults.
2. Row disable = 1 and column disable = 0; assertion of the row disable signal effectively gates the row selector off; the column selector takes over as it picks a subset of bit lines to be observed (this corresponds to selecting desired columns and is recommended to diagnose column and single cell failures).
3. Row disable = 0 and column disable = 0; de-asserting both control lines allows observation of memory cells located where selected rows and columns intersect.

It proceeds iteratively by determining a signature, which corresponds to the selected rows or columns, followed by a transfer of such a test response to the ATE through an optional shadow register. If the obtained signature matches the reference (golden) signature, we declare the selected rows and/or columns fault-free. Time required to filter out failing sites accurately depends on how selection of observable rows and columns is carried out. Our scheme employs an enhanced version of deterministic partitioning originally proposed for scan-based diagnosis. It assures the fastest possible identification of fault sources down to the array nodes that cannot be recognized as fault-free ones.

II. Row Selection

We start by introducing the general structure of the row selector shown in Fig-2. Essentially, it is comprised of four registers. The up counters partition and group, each of size n = _0.5 log2 R_, keep indexes of the current partition and the current group, respectively. They act as an extension of the row address register that belongs to the BIST controller (the leftmost part of the counter in Fig. 4. A linear feedback shift register (LFSR) with a primitive characteristic polynomial implements a diffractor providing successive powers of a generating element of GF(2n), which are subsequently used to selectively invert data arriving from the partition register. The same register can be initialized when its input load is activated. Similarly, one can initialize a down counter called offset by asserting its input load.

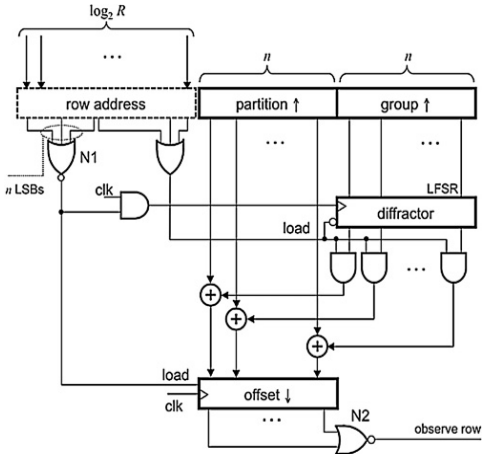


Fig.-2: The diagram depicts the output of gate N2

As can be seen, the diffractor is loaded at the beginning of a test run (row address = 0) with the group number 3 (112), and then it changes its state every four cycles by following the trajectory 1 → 2 → 3. At the same cycles, i.e., 0, 4, 8, and 12, the offset counter is reloaded with the sum of the partition number 2 (102) and the previous state of the diffractor, except for the first load, when only the partition number goes to the offset counter as the outputs of the AND gates are set to 0. After initializing, the offset regiter counts down and reaches zero at cycles 2, 5, 11, and 12, which yields an active signal on line "observe row" resulting, in turn, in observing data from the memory rows with addresses 2, 5, 11, and 12, respectively.

III. Column Selection

Fig-3 shows the column selector used to decide, in a deterministic fashion, which columns should be observed. Its architecture resembles the structure of the row selector as both circuits adopt the same selection principles. The main differences include the use of a BIST column address register and a diffractor clocking scheme. Moreover, the offset counter is now replaced with a combinational column decoder, which allows selection of one out of *B* outputs of the word decoder. It is worth noting that the diffractor advances every time the column address increments. Its content added to the partition number yields a required column address in a manner similar to that of the row selection.

The phase shifters PS1, PS2, and PS3 are then to output states of the original trajectory, but starting with the values of 4, 6, and 5, respectively. When various partition groups are examined, the diffractor traverses the corresponding parts of its state space while the phase shifters produce appropriate values that ensure generation of all $2n - 1$ combinations. The missing all-0 state is again obtained by means of AND gates.

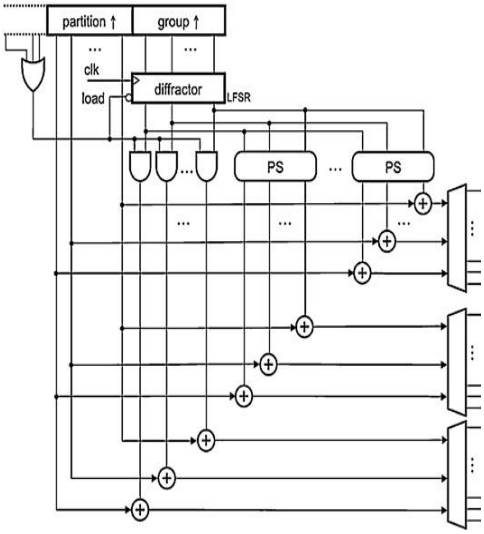


Fig.-3: Column Selector

IV. Combined Row and Column Selection

In order to reduce the area overhead, some components of the row selector and the column selector can be shared. The circuit by which this concept is implemented is shown in Fig where the partition and group registers feed both selectors. Since the word address increments prior to the row address, the memory array is read in the fast column.

As no interaction between control signals arriving from the word and row address registers is needed, the scheme enables reading the memory array in the fast row mode as well, after exchanging the row and column address registers. Furthermore, the combined row and column selector is designed in such a way that none of the components require clock faster than the one used to increment either the word or row address register. As a result, the proposed scheme allows reading memory at-speed, and thus detection of timing defects. Finally, as the combined selector makes it possible to collect the row and column signatures in parallel, such an approach allows one to reduce the diagnostic time by half. In this mode, however, two signature registers are required.

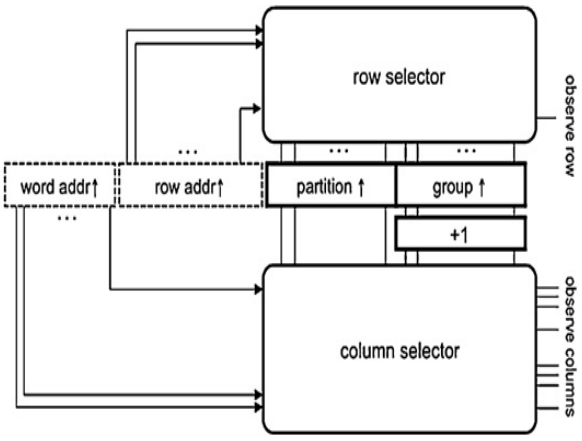
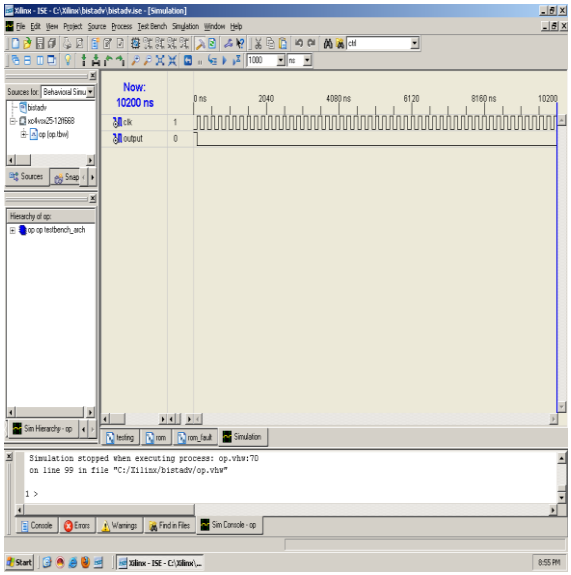


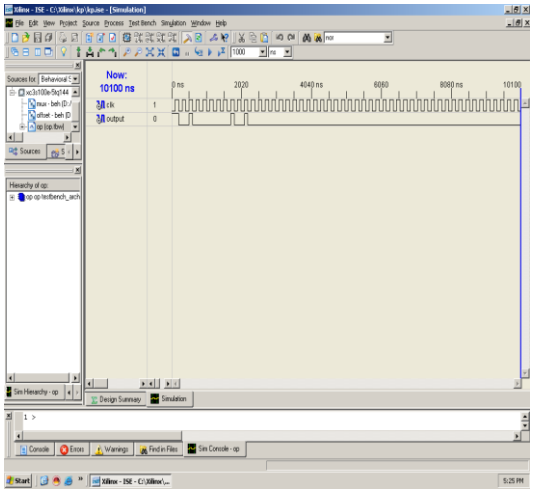
Fig.-4: Combined Row and Column Selector

V. Simulated Results

A. Heterogeneous Simulation Report for a Fault- Free Memory



B. Simulation report for a memory which consists of faults



Novel Built-In Self-Test (BIST) approaches for integrated optoelectronic systems are presented. The proposed approaches enable system evaluation under realistic operating conditions (including crosstalk degradation) through BER testing. They can speedup both circuit-level and system-level testing by providing means for accessing different parts of the circuit easily and allowing time-consuming performance tests to be run in parallel with boundary-scan tests.

VI. CONCLUSION

In this project, a new fault diagnosis scheme for embedded read-only memories is presented. It reduces the diagnostic data that needs to be scanned out during ROM test such that the minimum information to recover the failure data is preserved, and the time to unload the data is minimized. The presented approach allows an uninterrupted collection and processing of test responses at the system speed. This has been achieved by using low-cost on-chip selection

mechanisms, which are instrumental in very accurate and time efficient identification of failing rows, columns, and single memory cells. In particular, the scheme employs the original designs of row and column selectors with phase shifters controlling the way the address space is traversed.

Furthermore, the new combined selection logic allows the scheme to collect test results in parallel (leading to shorter test time) without compromising quality of diagnosis. Results of experiments performed on several memory arrays for randomly generated failures clearly confirm high accuracy of diagnosis of the scheme provided the signature registers and the proposed selection logic are properly tuned to guarantee a desired diagnostic resolution.

References

[1] J. T. Chen, J. Rajski, J. Khare, O. Kebichi, and W. Maly, "Enabling embedded memory diagnosis via test response compression," in Proc. VTS, 2001, pp. 292–298.

[2] J. T. Chen, J. Khare, K. Walker, S. Shaikh, J. Rajski, and W. Maly, "Test response compression and bitmap encoding for embedded memories in manufacturing process monitoring," in Proc. ITC, 2001, pp. 258–267.

[3] D. W. Clark and L.-J. Weng, "Maximal and near-maximal shift register sequences: Efficient event counters and easy discrete logarithms," IEEETrans. Comput., vol. 43, no. 5, pp. 560–568, May 1994.

[4] X. Du, N. Mukherjee, W.-T. Cheng, and S. M. Reddy, "Full-speed fieldprogrammable memory BIST architecture," in Proc. ITC, 2005, paper 45.3.

[5] D. Gizopoulos, Ed., Advances in Electronic Testing—Challenges and Methodologies. Dordrecht, The Netherlands, Springer, 2006.

[6] International Technology Roadmap for Semiconductors. (2009) [Online]. Available: www.itrs.net

[7] Y.-H. Lee, Y.-G. Jan, J.-J. Shen, S.-W. Tzeng, M.-H. Chuang, and J.-Y. Lin, "A DFT architecture for a dynamic fault model of the embedded mask ROM of SoC," in Proc. Int. Workshop Memory
Technol. Design Testing, 2005, pp. 78–82.

[8] J.-F. Li and C.-W. Wu, "Memory fault diagnosis by syndrome compression," in Proc. DATE, 2001, pp. 97–101.

[9] G. Mrugalski, J. Rajski, and J. Tyszer, "Ring generators: New devices for embedded deterministic test," IEEE Trans. Comput.-Aided Design, vol. 23, no. 9, pp. 1306–1320, Sep. 2004.

[10] N. Mukherjee, A. Pogiel, J. Rajski, and J. Tyszer, "High throughput diagnosis via compression of failure data in embedded memory BIST," in Proc. ITC, 2008, paper 3.1.

[11] D. Niggemeyer and E. M. Rudnick, "Automatic generation of diagnostic memory tests based on fault decomposition and output tracing," IEEE Trans. Comput., vol. 53, no. 9, pp. 1134–1146, Sep. 2004.

[12] J. Rajski and J. Tyszer, "Diagnosis of scan cells in BIST environment," IEEE Trans. Comput., vol. 48, no. 7, pp. 724–731, Jul. 1999.

speed memory testing with a slow memory tester," U.S. Patent 6 404 250, Jun. 11, 2002.

[13] J. Rajski, N. Tamarapalli, and J. Tyszer, "Automated synthesis of phase shifters for built-in self-test applications," IEEE Trans. Comput.-Aided Design, vol. 19, no. 10, pp. 1175–1188, Oct. 2000.

[14] J. Rajski, N. Mukherjee, J. Tyszer, and A. Pogiel, "Fault diagnosis in memory BIST environment," U.S. Patent Applicat. 20110055646, Sep.18, 2008.

Jhansirani.Atluri was born in Narasaraopet, Guntur (Dist.), AP, India. She received B.Tech. in Electronics & Communication Engineering from St. Ann's College of Engg.,Chirala ,prakasam (Dist.,),AP, India ,M.Tech from KL University , Vijayawada, AP, India. *E-mail: jhansi.atluri@gmail.com*

Harikishore.Kakarla was born in Vijayawada, Krishna (Dist.), AP, India. He received B.Tech. in Electronics & Communication Engineering from St. Johns College of Engg.,Kurnool(Dist.,),AP, India, MTech from G. Pulla Reddy Engineering College, Kurnool, AP, India. He is pursuing Ph.D in the area of VLSI in KL University, Vijayawada, AP, India. He has published 01 National Conference Level. *E-mail: Kakarla.harikishore@gmail.com*

Dr. Fazal Noorbasha was born on 29th April 1982. He received his, B.Sc. Degree in Electronics Sciences from BCAS College, Bapatla, Guntur, A.P., Affiliated to the Acharya Nagarjuna University, Guntur, Andhra Pradesh, India, in 2003, M.Sc. Degree in Electronics Sciences from the Dr. HariSingh Gour University, Sagar, Madhya Pradesh, India, in 2006, M.Tech. Degree in VLSI Technology, from the North Maharashtra University, Jalgaon, Maharashtra, INDIA in 2008, and Ph.D. Degree in VLSI from Department Of Physics and Electronics, Dr. HariSingh Gour Central University, Sagar, Madhya Pradesh, India, in 2011. Presently he is working as a Assistant Professor, Department of Electronics and Communication Engineering, KL University, Guntur, Andhra Pradesh, India, where he has been engaged in teaching, research and development of Low-power, High-speed CMOS VLSI SoC, Memory Processors LSI's, Digital Image Processing, Embedded Systems and Nanotechnology. He is a Scientific and Technical Committee & Editorial Review Board Member in Engineering and Applied Sciences of World Academy of Science Engineering and Technology (WASET), Advisory Board Member of International Journal of Advances Engineering & Technology (IJAET), Member of International Association of Engineers (IAENG) and Senior Member of International Association of Computer Science and Information Technology (IACSIT). He has published over 20 Science and Technical papers in various International and National reputed journals and conferences.

L.Veera Raju was born in Vijayawada, krishna (Dist.), AP, India. He received B.Tech. in Electronics & Communication Engineering from Prasad V. Potluri Siddhartha college of Engineering, Vijayawada (Dist.,),AP, India ,M.Tech from KL University , Vijayawada, AP, India. Email id: veerarajulanke@gmail.com

K.Purnima was born in Tenali, Guntur Dt., AP, India She received B.Tech. in Electronics & Communication Engineering from Vignan Engg., college, Vadlamudi, Guntur (Dist.,),AP, India ,M.Tech from KL University , Vijayawada, AP, India. Email id: purnima_483@yahoo.co.in