# A 346 μm² VCO-Based, Reference-Free, Self-Timed Sensor Interface for Cubic-Millimeter Sensor Nodes in 28 nm CMOS

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***Abstract*—We present a 346 μm² reference-free, asynchronous VCO-based sensor interface circuit demonstrated in 28 nm LP bulk CMOS. This design is specifically for sensor node interfaces which do not have the power or volume available for the high accuracy current sources, voltage sources, or low jitter timing references needed for traditional ADCs. By using a straightforward VCO design, it achieves wide resolution, voltage scalability, and process portability while consuming only ∼1/100th the area of prior approaches and avoiding costly reference circuitry. In the design measured for this paper, resolution can be scaled from 2.8 to 11.7 bits and $V_{DD}$ from 500 mV to 1.0 V. The design contains a single-point calibration scheme that works across temperature, voltage, and resolution settings. Minimum power consumption is 11.7 μW at 0.6 V $V_{DD}$ and minimum energy per conversion step is 41.2 fJ/b at 0.6 V $V_{DD}$ and 9.42 bits of effective resolution.**

***Index Terms*—Low area, post-processing, reference-free, scalable resolution, self-timed, sensor interface, temperature insensitive, VCO, voltage scalable, wireless sensor node.**

## I. Introduction

WIRELESS sensor nodes form the foundation for many cutting-edge solutions in infrastructure monitoring, environmental monitoring, and medical applications, and are often deployed in hard-to-reach places that require a small form factor [2]. These applications create new challenges in circuit design, where for the smallest applications, sensor nodes can be cubic millimeter in volume with microwatt-level power consumption, requiring small, voltage scalable IC designs that emphasize area and energy efficiency. An example system is shown in Fig. 1. This system is 1.0 $mm^3$ and includes a pressure sensor to monitor pressure in tumors for determining the effectiveness of chemotherapy treatments [3]. When sensor data is recorded and later post-processed, such as eye pressure monitoring of glaucoma patients or strain-gauge monitoring of bridges, large tradeoffs in sensor interface design can be leveraged to achieve efficiency goals. Salient features to trade away include speed and linearity. Linearity in particular is an unusual feature to trade-off since it closely relates to effective number of bits (ENOB). However, in these applications a full look-up table can be available via off-line post-processing, and high-frequency signals are not being reconstructed from the data [4].

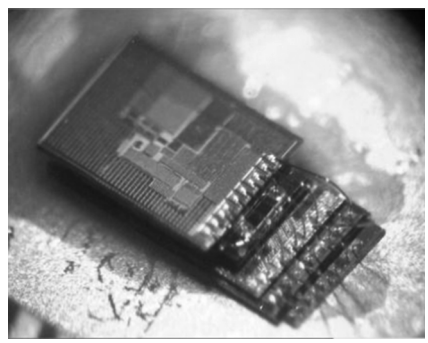

Fig. 1. **Target application.** Millimeter-scale wireless sensor nodes that cannot support high accuracy references [3].

Healthcare monitoring provides one particularly compelling application area for wireless sensor nodes. Researchers have developed implantable devices that can monitor and record health data to relay critical information to doctors, or to operate in a closed loop fashion. A millimeter-sized intraocular pressure sensor [5] can be inserted into a glaucoma patient's eye to record continuous eye pressure measurements, giving doctors a more complete history of daily pressure fluctuations and allowing for more informed decisions for treatment options. These measurements can be post-processed off-chip [4], which enables sensor interfaces such as that described in this work, achieving energy efficiency in a compact footprint.

Energy efficiency can be improved by using an interface that scales energy requirements with performance requirements. Wireless sensor nodes often employ multiple sensors, each with varying resolution requirements. The example system in Fig. 2 has three sensors: a 9 bit strain gauge, 7 bit temperature sensor, and 5 bit battery sensor. One way to interface with all three sensors is to implement a 9 bit ADC, reading all sensors at the maximum resolution of 9 bits. This strategy wastes energy by reading the temperature and battery sensors with more accuracy

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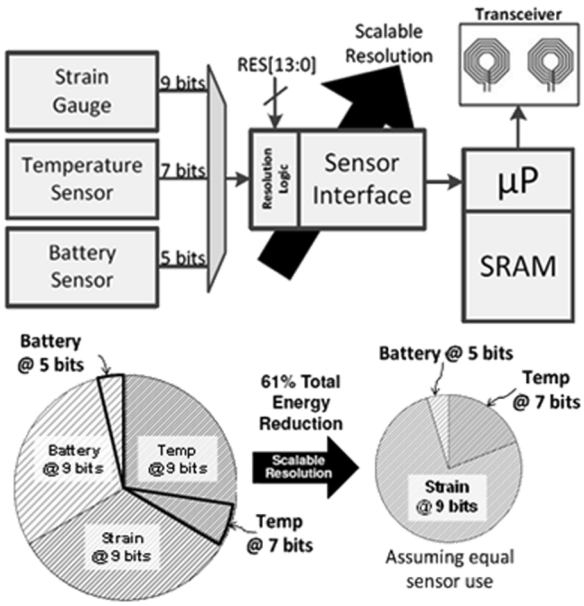


Fig. 2. **Multiple sensor application.** Energy scalability can be applied to multi-sensor applications, adjusting resolution (and energy) based on application specific requirements.

than necessary. Assuming equal use of all sensors, up to 61% energy reduction could be achieved by reading each sensor with its appropriate resolution. Using this architecture, assuming that energy decreases by a factor of $(1/C)^R$, where R represents the number of resolution steps and C is a scaling factor, then a 7 bit interface would use $(1/C^2) \times Energy_{9\text{bit}}$ and a 5 bit interface would use $(1/C^4) \times Energy_{9\text{bit}}$, resulting in a total energy *reduction* of $(1/3)(2-(1/C^2)-(1/C^4))$. Based on simulation results, C was calculated to be roughly equal to 2.6, resulting in a total energy reduction of 61%. In measured results, a 7 bit sensor used 19.25% of the 9 bit sensor energy, and the 5 bit sensor used 15.41% of the 7 bit sensor energy (3.01% of the 9 bit sensor). This resulted in measured energy reduction of 59%. This could be achieved by implementing three separate ADCs [6], each with different resolution capability, where each only communicates with its designated sensor. This increases the overall area and design cost by requiring a large number of readout circuits, and can increase energy consumption due to tail currents. A resolution scalable sensor interface can reduce energy consumption while occupying a small area, allowing the sensor node to scale energy with performance requirements by changing the resolution setting for each sensor individually.

Traditional ADC designs, such as successive-approximation register (SAR), achieve moderate resolution and energy efficiency through high accuracy capacitor arrays (DACs) and comparators, which require high accuracy references. However, high accuracy current, timing, and voltage references are often not feasible in wireless sensor nodes and these systems lack the space and power budget to include on-chip references. Many off-chip references require multiple components and are too large for such applications. For example, a typical off-chip current [7] is 24 mm$^2$ (packaged) without required resistors and capacitors, operates with a minimum 1 V supply, and dissipates 400 mW. Each of these specifications is individually infeasible for wireless sensor nodes, and the power requirement may even cause tissue damage when used in the eye pressure monitor. Due to the capability for off-chip correction, highly linear sensor readout circuits—and their associated references—are unnecessary. A previously published ADC design intended for use in wireless sensor nodes [8] attempts to address this design space by creating a resolution configurable, low energy SAR which can operate at 8 or 12 bits. However, this implementation is large at 0.63 mm$^2$, consumes 25 $\mu$W, and must operate at 1 V $V_{DD}$.

Other common design approaches for sensor interfaces include $\Delta\Sigma$, flash, and pipelined ADCs. $\Delta\Sigma$ designs achieve high resolution (12–18 bits) through filtering and decimation. These designs are typically high power (36 $\mu$W to 2.9 mW) [9], [10] and have large area (0.03 mm$^2$ to 2.32 mm$^2$) [11], [12]. A high accuracy timing reference for the modulator and digital filter is also required. Flash ADCs are extremely fast, but consume significant power (460 $\mu$W to 0.54 W) [13], [14] and are very large (0.033 mm$^2$ to 0.88 mm$^2$) [15], [16] due to the need for $2^N-1$ comparators in an N bit converter. Finally, pipelined ADCs are popular for ADC architectures with sample rates up to 100 MS/s and resolutions from 8 to 16 bits. These designs are both high power (mW-scale) and large (0.06 mm$^2$ to 0.63 mm$^2$) [17], [18], and also require high accuracy references.

In this paper, we describe a self-timed 346 $\mu$m$^2$ (0.000346 mm$^2$) VCO-based sensor interface in 28 nm LP CMOS. The topology is mostly digital and technology portable, and the extremely compact nature frees up silicon area for other system components. Dynamic resolution scaling requires only two additional standard cell FFs per additional bit of resolution, whereas previous designs [19] require exponentially larger capacitors. These capacitors do not scale well with technology and increase the area penalty in advanced process technologies. The proposed design uses no voltage or current references, and is self-timed, which further enables compact design.

Section II describes the proposed system, giving an overview of the circuit components and describing the methods for dynamically scalable resolution and offset calibration. Section III presents the measured results and an analysis of system performance. Section IV compares previous works with the proposed design and Section V concludes the paper.

## II. Circuit Description

The proposed design is VCO based, where the analog input voltage is first converted to the frequency domain and then digitized through a time-to-digital converter. In order to facilitate the self-timed nature of the design, the analog input voltage is converted to two frequencies, and those frequencies are compared to each other to form the measurement. As shown in Fig. 3, the circuit consists of two current starved VCOs, each followed by a pre-loadable ripple counter to count cycles, and a small finite state machine. The VCOs are designed to have opposing frequency responses—one with a positive response (PRVCO) where frequency increases with higher input voltage and one with a negative response (NRVCO) where frequency decreases with higher input voltage. The VCOs are designed such that the PRVCO and NRVCO have the same frequency at $V_{DD}/2$. These output frequencies are then fed into counters for

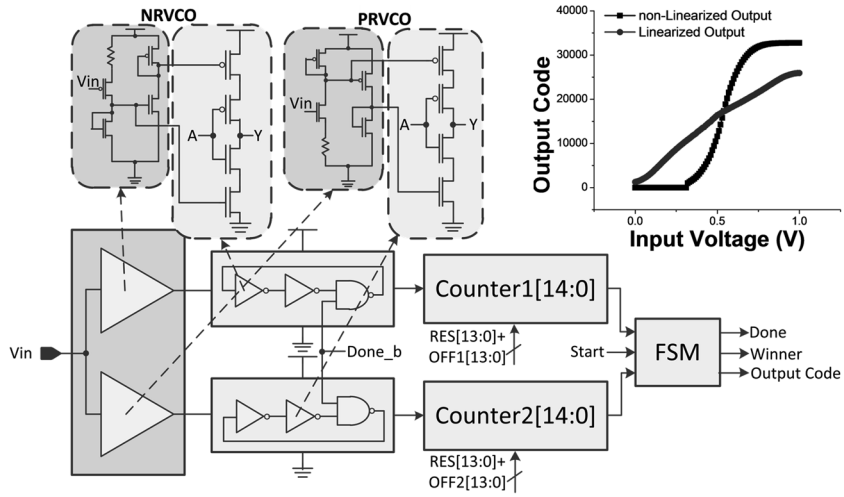


Fig. 3. **Sensor interface block diagram and measured output codes.** The sensor output is taken in as the input voltage ($V_{IN}$) and digitized into the above output code, which is linearized using simple degenerated amplifiers. The amplifiers increase the usable input voltage range from 0.4–0.6 V to 0.1–0.9 V. Output code measurements in the above graph are taken with an active counter bit setting of 14 bits.

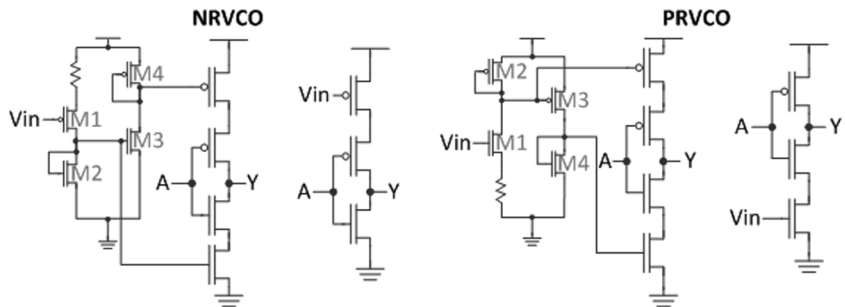


Fig. 4. **Linearized vs. non-linearized voltage controlled oscillators.** Each stage of the linearized VCOs has PMOS and NMOS starving transistors with the linearizing amplifiers controlling the oscillator's frequency response. The non-linearized VCOs have either a PMOS header (NRVCO) or an NMOS footer (PRVCO).

digitization. Due to their opposing frequency responses, one of the two VCOs will be faster than the other for each given input voltage $V_{IN}$—the NRVCO will be faster when $V_{IN} < V_{DD}/2$ and the PRVCO will be faster when $V_{IN} > V_{DD}/2$. The measurement is self-timed and ends when the faster of the two counters causes an MSB transition from 0 to 1. The FSM detects this transition and stops the oscillation of both VCOs, which freezes the counter values. The value on the slower counter, as well as one bit representing which counter finished first (PRVCO or NRVCO), are stored as the result of the measurement.

### *A. Voltage-Controlled Oscillators and Linearizing Amplifiers*

The VCOs are implemented using 5-stage current-starved ring oscillators, with four current-starved inverters and one current-starved NAND gate for control. The two oscillator frequencies become equal at the 'crossover point'. The current starving transistors and bias generators are sized such that this crossover point nominally occurs when $V_{IN} = V_{DD}/2$. This increases resolution by keeping the VCOs in a naturally linear range of operation, and increases linearity by equalizing the slopes of the two halves of the output code graph. The starving transistors, and the number of VCO stages can be optimized to achieve improved linearity, speed, or power consumption. Appropriately sizing the starving transistors and in combination with the linearizing amplifiers can improve the linearity, and decreasing the number of VCO stages will increase the speed and energy of the system.

The opposing frequency responses are created in the bias generation through the use of degenerated common source amplifiers, as shown in Fig. 3. These amplifiers also increase VCO linearities and greatly extend their input range ($4\times$). The PRVCO uses an NMOS-based common source amplifier and the NRVCO uses a PMOS-based common source amplifier. In both of these circuits (Fig. 4) M1, M2, and the resistor comprise the common source amplifier, M3 mirrors the current to the output node and M4 acts as a load for M3. Increasing the sizes of both M2 and the degenerating resistor increase linearity at the cost of increased power consumption and area. To achieve a reduction in power, the linearizing resistor can be sized up, which also improves linearity, but greatly increases the area of the amplifiers. In simulation, when the linearizing resistor is sized up from 80 k$\Omega$ to 160 k$\Omega$, the input range stays constant but the power reduces from 26.9 $\mu$W (in one amplifier) to 15.2 $\mu$W. This corresponds to a decrease in power by $0.56\times$ for an area increase of $2\times$.

These amplifiers do not require high accuracy current sources or bias voltages, and take only the sensor output voltage as an input. The goal of these amplifiers is to bias each oscillator in its highly linear range of operation for a wider range of input voltages, while simultaneously generating opposing frequency

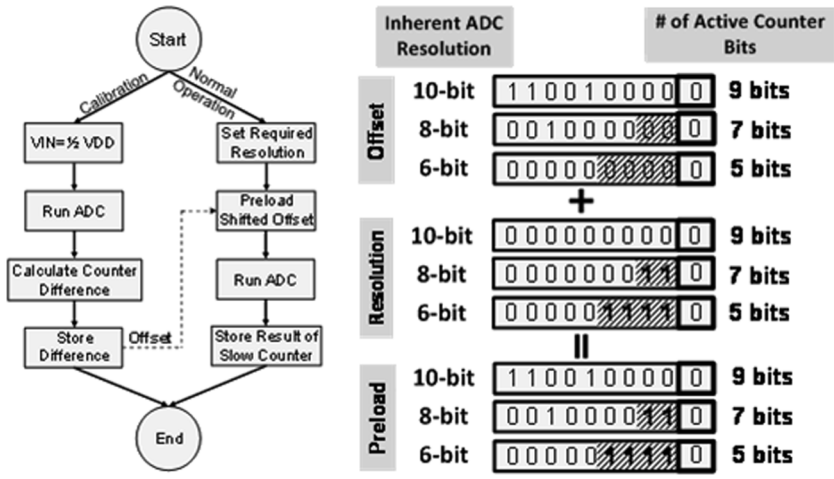


Fig. 5. **Calibration flow and preload calculation example.** (Left) Single point calibration flow chart. (Right) Preload calculation combining the active counter bit setting and calibration offset code.

responses. Each amplifier provides two biases, one for VCO headers and one for VCO footers. Without linearizing amplifiers, the oscillators saturate and turn off in high and low voltage ranges, restricting the usable input voltage range to between 0.4 V and 0.6 V (for 1 V $V_{DD}$), instead of the full 0.1–0.9 V range of the linearized design. Full-range input voltage can also be used, but results in decreased linearity.

For high-accuracy measurements, linearity can be further corrected through post-processing of the data with a full table, which is common in wireless sensor node applications [20]. This correction is done off-chip after data collection from the sensor nodes is complete. In low-resolution applications, such as wakeup monitors, post-processing is not needed. Without the use of a look-up table, the output code response (slope) varies with input voltage. Measurements of the system with 14 active counter-bits at 1 V $V_{DD}$ show a slope of 17540 codes/V in the range of 0.1 V to 0.3 V input voltage, 15368 codes/V from 0.3 V to 0.5 V, 10302 codes/V from 0.5 V to 0.7 V, and 11415 codes/V from 0.7 V to 0.9 V. This difference in slope affects the overall linearity of the system and necessitates the use of a full, off-chip, look-up table for high accuracy measurements. The measurements in this design used a full look-up table via an off-chip computer. Smaller look-up tables can be implemented on-chip, eliminating the need for off-chip correction, but would result in an increase in linearity errors. The off-chip look-up table consists of a high resolution, full-range, input voltage to output code mapping. The smaller, on-chip, look-up table would contain a more sparse representation of the same mapping, and the output value can be calculated using linear interpolation of a subset of points in the table via software. The look-up table does not need to scale with resolution, as a larger table will always work well for smaller resolution values. If it is necessary to scale the number of entries in the look-up table, then for each fewer bit of resolution half of the entries could be eliminated (every other entry).

### *B. Non-Linearized VCOs*

Another design approach would directly use $V_{IN}$ to starve the oscillators, which avoids the need for linearizing amplifiers to generate bias voltages. As shown in Fig. 4, this could be accomplished by using just an NMOS footer for the PRVCO (i.e., no header) and just a PMOS header for the NRVCO (i.e., no footer). The circuit would have the same functionality with decreased resolution, linearity, and operating range, but also decreased power consumption and area. Crossover point sizing and calibration in the non-linearized VCOs is similar to the linearized version but does not require sizing between the linearizing amplifiers and the header/footer combinations. Instead only the NMOS footer and PMOS header need to be sized to achieve equal frequencies at the crossover point.

Some wireless sensor node applications could benefit from this type of functionality. Battery monitors typically operate in a narrow range of voltages, where users may prefer high accuracy in a small voltage range and very low accuracy outside of that region. This can save both power and area, as the linearizing amplifiers consume nearly half of the total power.

### *C. Crossover Point Calibration*

The crossover point can be single-step calibrated to correct for VCO variation or sizing mismatch between the starving transistors. Fig. 5 shows the calibration algorithm. First, $V_{IN}$ is set to $V_{DD}/2$ and the converter is run until completion (one of the two counters has an MSB transition and both oscillators are stopped and the counters frozen). At this voltage, the oscillator frequencies should be equal and therefore the counter values should be equal. If there is any mismatch between the two devices, their frequencies will differ with a corresponding difference in counter values. The difference remaining between the two counters at the end of the measurement is loaded back onto the slower counter as its offset in each subsequent conversion. This effectively speeds up the slower counter enough to equalize the frequencies at $V_{DD}/2$, and the pre-calibration and post-calibration shift in output response is shown in Fig. 6.

The calibration value needs to be measured only once, at the maximum resolution and mid-range power supply, and can then be shifted for lower resolutions since it does not significantly vary with $V_{DD}$ or temperature, as shown in Section III. The reference voltage of $V_{DD}/2$ can be provided directly from

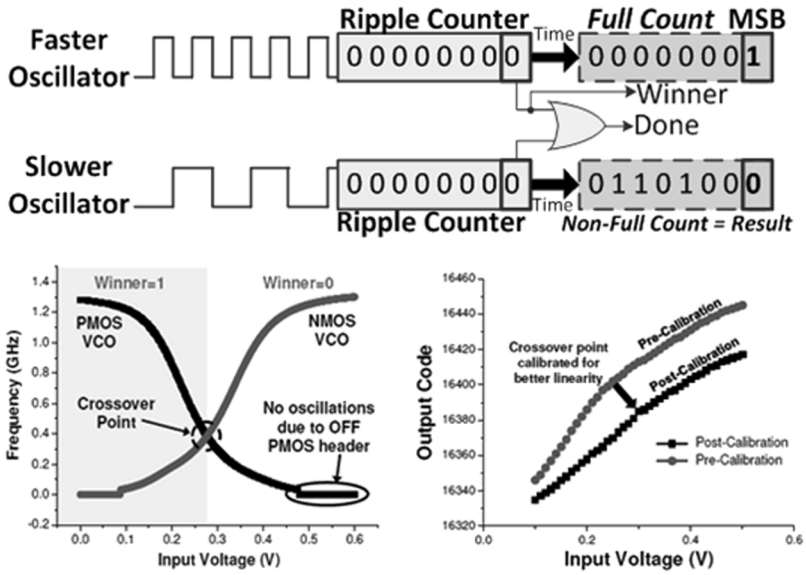


Fig. 6. **Sample FSM operation and crossover point calibration.** (Top) FSM to monitor MSB transitioning. (Bottom Left) PSV and NSV simulated frequencies vs. input voltage. (Bottom Right) Measured output code vs. input voltage and crossover point calibration for a 6 bit active counter-bit setting.

the power supply through a small reference circuit, or could be provided off-chip in a one-time testing scheme, since accuracy is not critical. Any errors in this reference value will translate into offsets in the crossover point, which may slightly decrease resolution. This calibration method allows for full range offset compensation.

### *D. Dynamic Resolution Scaling*

Dynamically scalable resolution is achieved through pre-loading the upper bits of the ripple counters. Resolution is defined by the frequencies of the two VCOs, where the faster oscillator sets the conversion time, and the slower oscillator sets how fast the counter runs during the time period, resulting in a ratio:

$$OutputCode \propto \frac{f_{\text{slow}}}{f_{\text{fast}}}$$

The resolution is limited by how finely $f_{\text{slow}}$ and $f_{\text{fast}}$ can be measured, but this can be controlled by counter length, which extends the time of the measurement. Thus, maximum achievable resolution is directly controlled by the maximum counter value. Since there are two counters in this design, if each counter has 10 active counter-bits plus 1 bit of MSB, the maximum achievable resolution, which corresponds to the resolution of the sensor interface, is 11 bits (where one bit of information is obtained by recording which counter was faster). By reducing the number of active counter-bits, the maximum conversion time, maximum resolution, and energy all reduce as well. The maximum counter value can be reduced by pre-loading a '1' into the higher order bits of the counters, thereby deactivating them as shown in Fig. 5. Resolution is impacted as in the following equation:

$$OutputCode = \left(\frac{f_{\text{slow}}}{f_{\text{fast}}}\right) \times maxCounterValue.$$

Resolution scales linearly between 2.8 and 11.7 bits of effective resolution with 11 pre-loadable counter-bits, with each additional bit of resolution adding two flip-flops (one to each counter). Low resolution applications can achieve extremely small footprints by limiting the number of counter-bits.

The output code calculated by the FSM is based on the following logic:

IF (NRVCO is slower) THEN

OUTPUT CODE = NRVCO counter value

IF (PRVCO is slower) THEN

OUTPUT CODE =(2 × maxCounterValue) − (PRVCO counter value).

This output code is affected by the active counter-bit setting. To decrease the overall system resolution, counter-bits are deactivated by pre-loading a '1' into higher order bits. This reduces the amount of conversion time but also sets minimum and maximum bounds on the output codes. When the system is at full resolution, the output codes can range from zero to 2× the maximum value stored on one counter. With resolution scalability, the output codes are offset by the following amount:

$$OutputCode\ Offset = \sum_{i=N}^{maxCounterBit-1} 2^i$$

where $N$ is the active counter-bit setting and $maxCounterBit$ is the number of available counter-bits in the design, excluding the MSB. This sets a minimum bound for the output code, restricting it to the number of pre-loaded counter-bits. Thus, with resolution scaling, the output code always decreases from both sides of the graph toward the crossover point, keeping the midrange output code value constant across all active counter-bit settings.

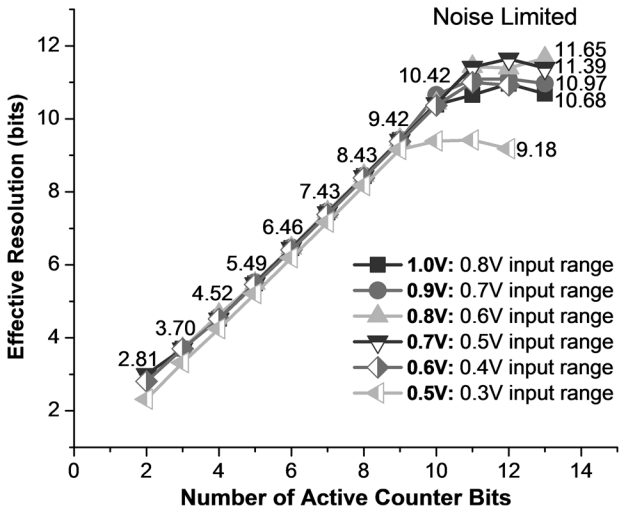


Fig. 7. **Effective resolution versus the number of active counter bits.** Resolution scales linearly with the number of active counter bits and is not impacted by voltage scaling until $V_{DD} = 0.5$ V (near-threshold).

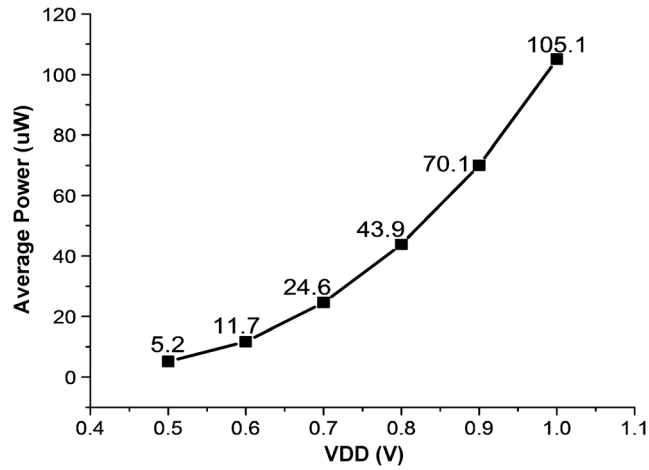


Fig. 8. **Average power versus power supply.** Average power consumption over scaled $V_{DD}$ from 0.5 V to 1.0 V.

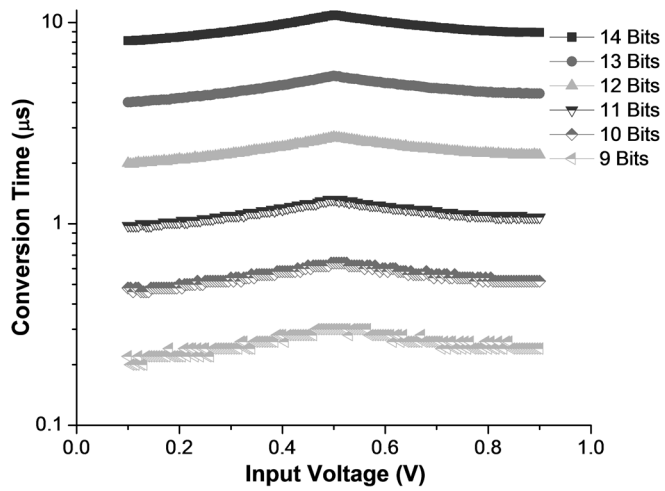


Fig. 9. **Conversion time.** Measured conversion time for each input voltage and for active counter-bit settings from 9 to 14 bits.

## III. Measurement Results

This chip was fabricated in a 28 nm LP CMOS process and included four different variations of the proposed interface for testing purposes. The 4 different variations were: 3-, 5-, and 7-stage ring oscillators using LVT starving transistors, and a 5-stage ring oscillator with SLVT starving transistors. Each sensor interface included 14 bit counters to measure maximum resolution and resolution scalability.

The length of the VCO determines the speed, power, energy, and noise characteristics with which the interface can operate. For this implementation, a shorter VCO was chosen to increase the speed (decrease the energy consumption), setting the frequency range to about 1.3 GHz in simulation. Longer VCOs would give enhanced noise characteristics as a result of increased averaging over stages, but would greatly decrease the overall speed and increase energy.

### *A. Resolution, Energy, and Power With Voltage Scaling*

Effective resolution, measured as

$$\log_2(V_{\mathrm{inputRange}}/\mathrm{RMS}_{\mathrm{Noise}}),$$

scales linearly from 2.8 to a noise-limited 11.7 bits over a power supply range of 0.6–1.0 V (Fig. 7). Noise was measured by fixing the input voltage and measuring the standard deviation of output codes over 100 separate conversions. Due to the inherent nonlinearity of the interface, the noise was measured at three different input voltages: at the lowest $V_{IN}$, highest $V_{IN}$, and at $V_{DD}/2$, though only a weak dependence on input voltage was observed during noise measurements. At 0.5 V $V_{DD}$ (representing near-threshold operation in this LP process [21]), the noise-limited maximum resolution decreases to 9.2 bits. Each additional active counter-bit contributes nearly 1 additional bit of effective resolution. The linear relationship between counter-bit setting and measured resolution allows for simple resolution control logic, which is beneficial in targeted ultra-low power applications.

Average power scales from 105 $\mu$W to 11.7 $\mu$W as $V_{DD}$ is reduced from 1.0 V to 0.6 V (Fig. 8), tapering off at 5.2 $\mu$W at 0.5 V as the constant current draw of the linearizing circuit begins to dominate. Conversion time scales exponentially with the number of active counter-bits (Fig. 9), from 36 ns to 9.3 $\mu$s (2.8 to 11.0 bits) at 0.6 V, and also scales with input voltage $V_{IN}$. At very low resolution, the conversion time saturates as the FSM delay becomes limiting. These conversion times are acceptable for sensors where values change on the scale of milliseconds (e.g., temperature), and are comparable to low voltage (0.8 V) ADCs presented in [13], [18]. Energy per measurement also scales exponentially with resolution, from 0.6 pJ to 217 pJ at 0.6 V. Thus, reducing the number of active counter-bits is highly beneficial to system energy, decreasing it by up to 1000×.

Fig. 10 shows an energy consumption breakdown for the seven active counter-bit setting (7.4 bit effective resolution). Static energy from the linearization circuits starts increasing below 0.7 V while minimum energy per measurement is 27 pJ, which is achieved at 0.6 V. Energy per conversion step at a fixed $V_{DD}$ (Fig. 11) remains relatively constant over a range of 5–10 active counter-bits, increasing at higher resolutions due to system noise limitations and at lower resolutions due to the saturation of both power and conversion time. The minimum

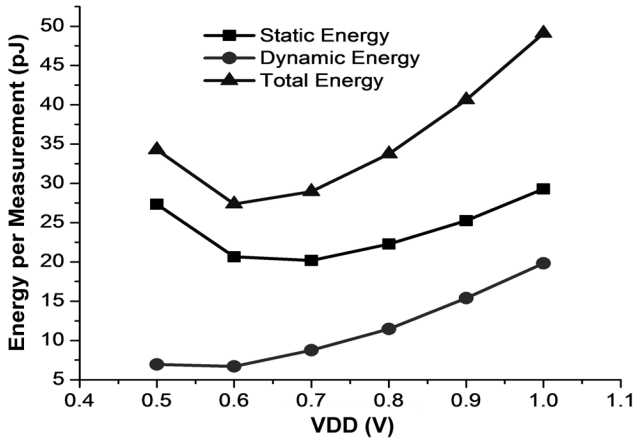


Fig. 10. **Energy breakdown over power supply.** Static and dynamic energy breakdown over scaled $V_{DD}$ for 9.4 bit effective resolution operation.

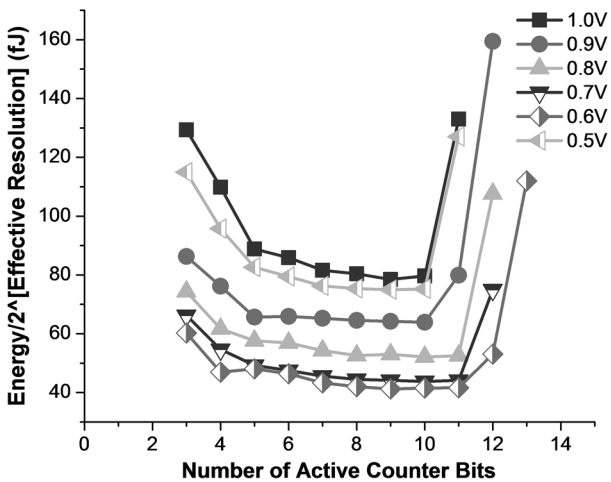


Fig. 11. **Energy per conversion step (fJ/conv-step).** Energy per bit of resolution for each preset resolution value and each $V_{DD}$ setting.

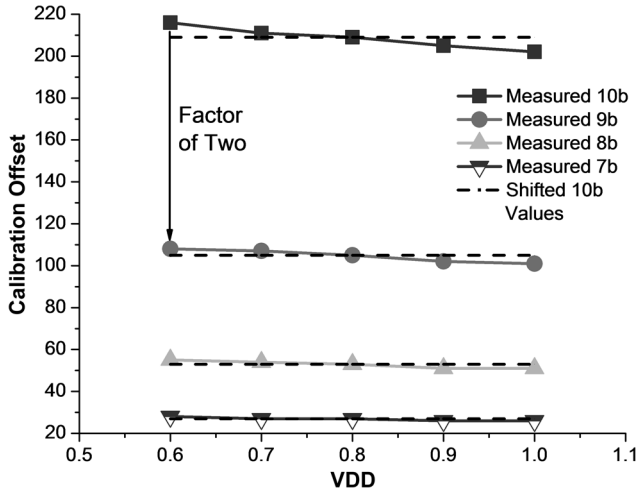


Fig. 12. **Calibration offset code versus power supply.** Measured calibration offset code from stored and values scaled by the number of active counter bits.

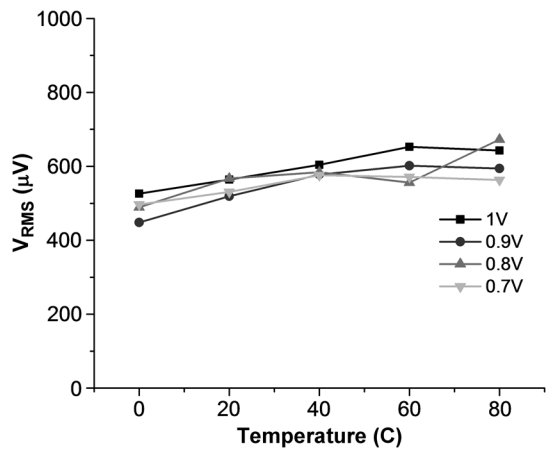


Fig. 13. **RMS noise versus temperature.** RMS noise increases with temperature up to a maximum of 673 $\mu$V at 0.8 V $V_{DD}$, which corresponds to a resolution of 10.22 bits.

achieved value for energy per conversion step at a setting of 9.4 bits of effective resolution is 41.2 fJ/step at 0.6 V with a maximum of 80.4 fJ/step at 1 V $V_{DD}$. Energy per conversion step is constant between 5 active counter-bits and 10 active counter-bits due to the exponential scaling of energy and linear scaling of effective resolution.

### *B. Crossover Point Calibration*

Fig. 12 shows measured and calculated offset values versus voltage and active counter-bit settings. The calculated values are shown as dotted black lines, where the offset is constant across power supply and scales by a factor of two for each additional active counter-bit. At a measured active counter-bit setting of 10 bits, the calibration offset average at 0.8 V is 209 counts. The maximum observed error between measurement and calculation due to $V_{DD}$ scaling is 16 counts, which corresponds to a shift of 8 mV in input voltage. Calibration measurements show that this estimation is accurate for each active counter-bit setting, and that $V_{DD}$ offset error reduces with decreasing resolution, resulting in a maximum error of only 1 count (4 mV input voltage) at the 7 bit active counter-bit setting.

### *C. Noise and Calibration Error Over Temperature*

Sweeping temperature from 0 °C to 80 °C shows that the RMS noise of the system increases with temperature with a maximum increase of 0.18 mV at 0.8 V $V_{DD}$, which corresponds to a resolution degradation of 0.46 bits (Fig. 13). This degradation affects the maximum achievable resolution while all resolution values that are not noise limited remain unchanged. Calibration offset codes were also measured across temperature and power supply to determine the maximum error expected from a one-point calibration scheme (Fig. 14). A maximum error of 34 counts (22 mV input voltage shift) occurs at 0 °C and 0.7 V $V_{DD}$.

The results in Fig. 14 show that for this implementation, calibration offset codes decrease monotonically with temperature. This is because the PRVCO is faster than the NRVCO for all points in the graph, due to either sizing or threshold voltage mismatch. To compensate, the slower counter (NRVCO) is pre-loaded with calibration offset codes—effectively speeding up the NRVCO by giving it a head start. When temperature increases, NMOS drain current decreases more rapidly than PMOS drain current. The linearizing amplifier in the NRVCO

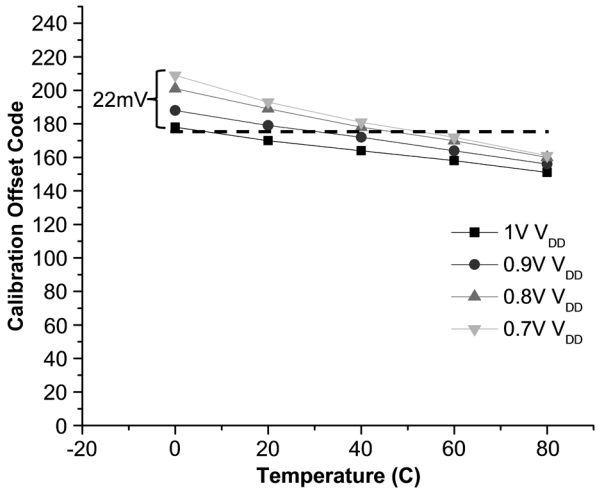


Fig. 14. **Calibration offset code measurement versus temperature.** Measured calibration offset code decreases with increasing temperature. Maximum error of 34 counts at 0.7 V $V_{DD}$ (22 mV $V_{IN}$ shift) between the stored single point calibration code (horizontal dashed line) and the measured codes.

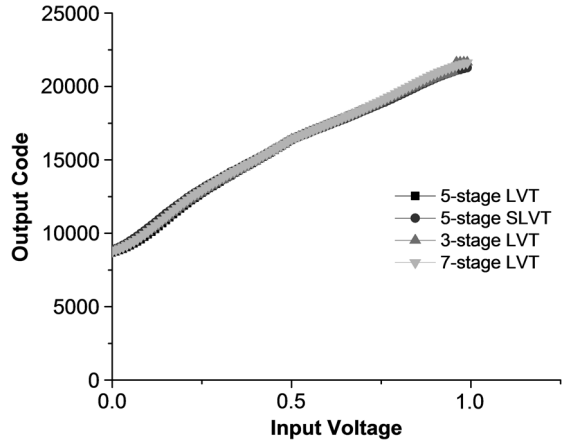


Fig. 15. **Output code versus input voltage of four sensor interface variants**. Four different variations of the proposed interface were implemented, varying threshold voltage (LVT/SLVT) and ring oscillator length (3, 5, or 7 inverters), each measured at a 13 bit active counter-bit setting in this graph. The output response and resolution do not significantly vary with these modifications.

is controlled by a PMOS input transistor and the amplifier in the PRVCO is controlled by an NMOS. Due to this difference in temperature dependence, the PRVCO slows down more rapidly than the NRVCO, causing the oscillator frequencies to approach each other at higher temperatures, thus reducing the required calibration offset code monotonically.

Since the calibration offset codes decrease monotonically with temperature, the single point calibration measurement should be taken at a midrange temperature (40 °C for these measurements) to minimize error.

Temperature variation affects the output code range of the ADC. With increasing temperature the minimum output code value increases and the maximum output code value decreases, decreasing the overall range. At 0 °C, 1 V $V_{DD}$, and an active counter-bit setting of 7 bits, the output code range is 204 levels. When the temperature increases to 60 °C, the output code range decreases to 177 levels. This change in output response affects the accuracy of the off-chip, full look-up table. Using one look-up table (nominal temperature measurements) over all temperatures would result in a maximum error of about 0.08 V (input voltage), or 0.1 bits of resolution. However, multiple look-up tables could be used to reduce this error. Calibration measurements using the given oscillators provide an accurate estimation of temperature (Fig. 14) if averaged over several measurements to account for power supply variation. These temperature estimations can be used to select an appropriate off-chip look-up table for use in subsequent measurements. With a look-up table for each 20 °C temperature step, the maximum error due to temperature variation can be reduced to 0.02 V (input voltage), or 0.04 bits.

### D. Output Response and Linearity

Fig. 15 shows the measured output code versus input voltage of four different variations of the proposed sensor interface. The output response shows very little change with either threshold voltage or ring oscillator length. All of the variations showed similar responses with power supply scaling. Process and temperature analysis were not analyzed for the different interface variations.

At 1 V, the average INL and DNL in the 7 active counter-bit setting (7.4 bit effective resolution) are $+0.12/-0.52$ LSB and $+0.22/-0.17$ LSB, respectively, after digital correction through a full look-up table. Fig. 16 shows the pre- and post-transformation output codes. This table would likely be contained off-chip in most applications [2].

### E. Non-Linearized VCOs

Included and measured on the test die was a non-linearized variant of the design. As described in Section II-B, this version of the system connects $V_{IN}$ directly to the headers and footers of the VCOs in order to decrease the sensor interface power. As seen in Fig. 17, between 55.4% and 68.2% of overall power (at 1 V and 0.6 V $V_{DD}$, respectively) can be reduced, making the minimum power draw 3.7 $\mu$W (0.6 V $V_{DD}$). This reduces the input range from 0.1–0.9 V to 0.4–0.6 V (a 4$\times$ difference), for a 1.0 V supply.

### F. Area and Low Resolution Modifications

The proposed sensor interface core area occupies 346 $\mu$m$^2$, and the die microphotograph is shown in Fig. 18. This area does not include a register used to store the offset value for crossover calibration. An additional eight registers to store the offset value would add roughly 50 $\mu$m$^2$ in additional area. Compared to more traditional implementations, this area is 100$\times$ smaller than a resolution scalable (up to 10.5 b) SAR [19] (ideally scaled from 65 nm) and 10$\times$ smaller than an 8 bit 28 nm sub-ranged SAR [22]. For testing purposes, the proposed circuit was implemented with 15 counter-bits (14 active bits and the MSB, used to determine which counter finished first). The maximum resolution achieved was 11.7 bits. In a typical implementation, there would be four fewer counter-bits (eight fewer flip-flops), reducing overall area by 70 $\mu$m$^2$. In low resolution applications, area reduction can be even more aggressive, e.g., reducing the number of counter-bits to 6 yields an overall area

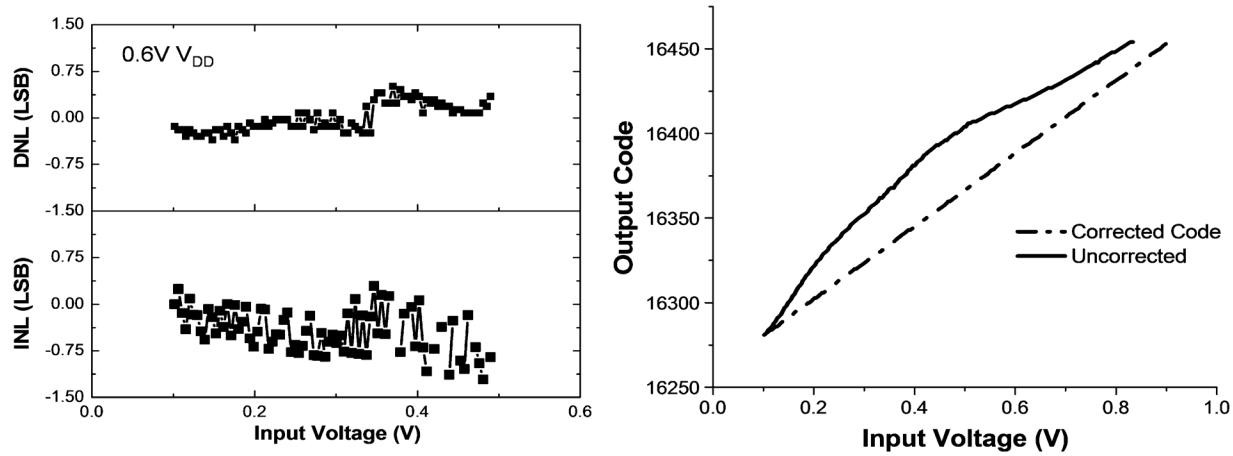


Fig. 16. **Post-correction DNL, INL and output code response.** (Left) Post-correction DNL and INL for 7 bit active counter bit setting with a look-up table (0.6 V $V_{DD}$). (Right) Uncorrected and corrected (look-up table) output codes versus input voltage for an active counter bit setting of 7 bits. Post-correction is performed after data collection from the sensor nodes.

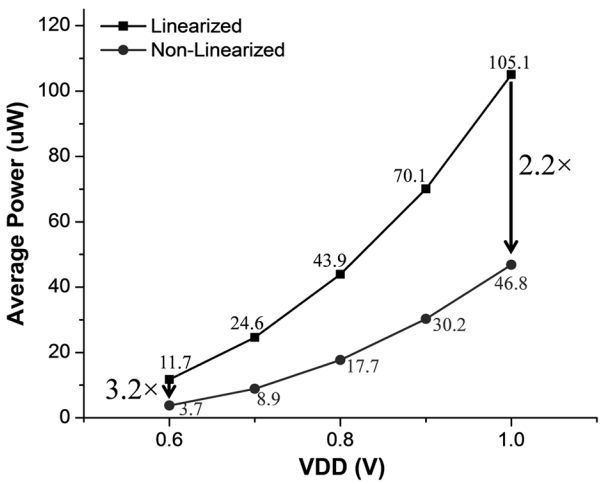


Fig. 17. **Average power of the linearized and non-linearized sensor interfaces versus power supply voltage.** A small input voltage range (0.2 V) is acceptable for certain applications (e.g., battery monitors), reducing the average power consumption by 2.2× at full $V_{DD}$ and 3.2× at 0.6 V $V_{DD}$ by eliminating the need for the linearizing amplifiers.

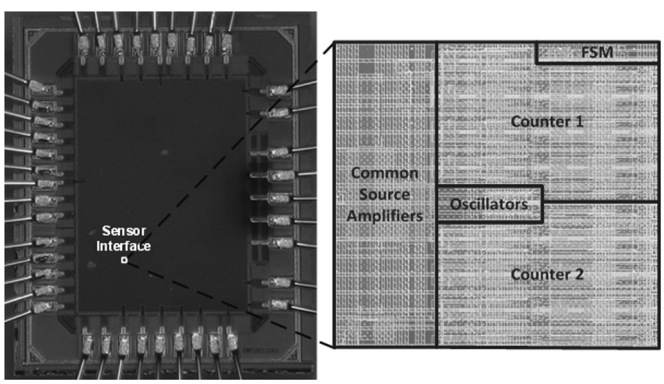


Fig. 18. **Die microphotograph and chip layout**. Fabricated in a 28 nm LP CMOS process and occupies 346 $\mu m^2$.

of 170 $\mu m^2$ (2× smaller). This implementation provides 5.5 bits of maximum effective resolution.

## IV. Comparison With Prior Works

Table I compares the proposed linearized design and three closely related, published ADCs with salient features listed. The first comparison point [19] is a resolution scalable SAR ADC implemented in 65 nm CMOS. This paper leverages a reconfigurable DAC to target sensor networks and medical monitoring for energy-constrained systems. The application space, voltage scalability, and resolution reconfigurability make this paper a pertinent comparison point to the proposed design. Compared to this work, resolution scalability for our design is increased by 4 bits (2.8 to 11.7 bits ER versus 4.77 to 8.84 bits ENOB), conversion time at low voltage is improved by 50× and area (assuming ideal scaling from 65 nm to 28 nm) is decreased by 100×. While power consumption is higher for our design (11.7 $\mu$W to 0.2 $\mu$W), that does take into account the high accuracy timing reference and high accuracy voltage references needed, which can be on the order of milliwatts [7].

The second comparison point [6] is a wireless strain sensing microsystem that incorporates two ADCs for multi-sensor readout. This system provides an important comparison between a resolution scalable implementation for multi-sensor wireless nodes, and an implementation that leverages multiple interface circuits to increase readout efficiency. Area is significantly increased in this design in order to facilitate two ADCs, and high accuracy references are needed for proper operation of the comparators and $\Delta\Sigma$ ADCs. For wireless sensor nodes implemented in smaller processes, this implementation would be challenging to build.

The third comparison paper [23] is a wireless blood pressure sensing microsystem that leverages an 11 bit cyclic ADC. This paper provides a good comparison against another wireless sensor implementation, but one that uses a non-traditional ADC topology in order to achieve low power dissipation in a small area. This implementation achieves 12 $\mu$W power dissipation at a power supply of 2 V in 1.5 $\mu$m CMOS. Because the cyclic ADC incorporates high-accuracy capacitors, it may not scale well to 28 nm or other advanced process nodes. Additionally, the conversion scheme relies on a high resolution comparator

TABLE I
RESULTS AND COMPARISON

| | This Work | | | Yip [19] ISSCC 2011 | Suster [6] ISSCC 2007 | Cong [23] JSSC 2009 | Taylor [24] JSSC 2010 |
|---|---|---|---|---|---|---|---|
| Technology | 28nm | | | 65nm | 1.5µm | 1.5µm | 65nm |
| Architecture | VCO | | | SAR | 1st-order ΔΣ<br>2nd-order ΔΣ | Cyclic ADC | VCO-based ΔΣ |
| Key Features | Sclable Resolution, Low Area | | | Scalable Resolution | Multi-Sensor Multi-ADC | Low Power | Variable Rate |
| Requires Accurate Current Sources | **No** | | | Yes | Yes | No | No |
| Requires Low Jitter Timing Reference | **No** | | | Yes | Yes | Yes | No |
| Area (µm²) | **346** | | | 212,000<br>39,339 (scaled) | 1,597,000 (total)** | 532,400** | 70,000<br>12,989 (scaled) |
| VDD (V) | 0.6 | 0.8 | 1.0 | 0.4 – 1.0 | 3.0 | 2.0 | 1.2 and 2.5 |
| Effective Resolution | 2.8 – 11.0 | 3.7 – 11.7 | 3.7 – 11.0 | 6.4–10.5* | 11.2* – strain<br>12.6* – temp | 12.3* | 13.1–14.8* |
| Power (µW) | 11.7 | 43.9 | 105.0 | 0.206 (@0.7V) | Not Reported | 12 | 8,000 – 17,000 |
| Conversion Time (µs) | 0.036 – 9.3 | 0.022 – 3.3 | 0.016 – 1.0 | 0.5 (@1.0V)<br>200 (@0.4) | (1st-order) 5.88<br>(2nd-order) 50 | 500 | 0.00086 – 0.002 |

* ENOB to ER conversion via IEEE standard 1057.
** Not Reported—Estimated from die microphotograph *Ideal* scaling applied to areas.

and precise timing references in order to properly operate the large number of switches in the design.

The fourth comparison paper [24] is a reconfigurable VCO-based delta-sigma modulator. This paper uses a mostly digital design with digital background calibration and dithering, eliminating the need for high accuracy voltage, current and timing references. This paper provides an important comparison against another VCO-based ADC which also aims to eliminate high accuracy references, and capitalize on a digital implementation to achieve large area gains over traditional implementations. However, the large amount of calibration circuitry used in this implementation requires area usage of about 13,000 $\mu$m$^2$ (38$\times$ larger than the proposed design—after ideal scaling), and between 8–17 mW power consumption (683$\times$–1453$\times$ increase over the proposed design).

Additional comparison points can be readily found in B. Murmann's ADC survey [25]. Other implementations that are less than 0.1 mm$^2$ in size can be found with ENOB between 4 and 12 bits [26], [27], but power on the order of mW, and area between 4$\times$ and 290$\times$ larger than our proposed design. Other scalable resolution ADCs [8], [19], [28] present SAR topologies with limited resolution scalability from two settings (8 bits or 12 bits) up to a 5 bit range (5–10 bits), and comparable power consumption of 0.2 $\mu$W to 17.4 $\mu$W. In addition to requiring high accuracy references, these designs require large capacitor arrays for resolution scaling, up to 1800$\times$ more area than the proposed design, and a limited range of resolution scalability (2–4$\times$ less resolution range). As shown, our design is unique in its combination of exceptionally small area, wide range of resolution scalability, and simplicity in reference-free design.

## V. CONCLUSION

This paper presented a reference-free, VCO-based sensor interface circuit in 28 nm LP CMOS, designed to specifically address the constraints of wireless sensor nodes. This design is implemented in an area $\sim$1/100th that of prior approaches. Resolution scales between 2.8 and 11.7 bits, and the power supply is scalable from 500 mV to 1.0 V. The design contained a single-point calibration scheme that functions well across temperature, voltage, and resolution. The ease of design and use, in addition to the wide range of operating conditions of this circuit, allow for implementation in a variety of sensor applications.

## ACKNOWLEDGMENT

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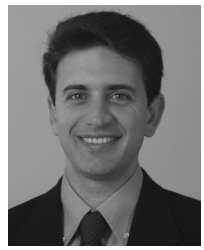

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