International Journal of Soft Computing and Engineering (IJSCE)
ISSN: 2231-2307, Volume-2, Issue-1, March 2012

Matlab -based Simulation & Analysis of Three - level SPWM Inverter

Kapil Jain, Pradyumn Chaturvedi,

Abstract: ***The multilevel began with the three level converters. The elementary concept of a multilevel converter to achieve higher power to use a series of power semiconductor switches with several lower voltage dc source to perform the power conversion by synthesizing a staircase voltage waveform. However, the output voltage is smoother with a three level converter, in which the output voltage has three possible values. This results in smaller harmonics, but on the other hand it has more components and is more complex to control. In this paper, different three level inverter topologies and SPWM technique has been applied to formulate the switching pattern for three level inverter that minimize the harmonic distortion at the inverter output. Simulation result has discussed.***

Key Words: SPWM, THD, PWM

I. INTRODUCTION

Multilevel inverter is based on the fact that sine wave can be approximated to a stepped waveform having large number of steps. The steps being supplied from different DC levels supported by series connected batteries or capacitors. The unique structure of multi- level inverter allows them to reach high voltages and therefore lower voltage rating device can be used. As the number of levels increases, the synthesized output waveform has more steps, producing a very fine stair case wave and approaching very closely to the desired sine wave. It can be easily understood that as motor steps are included in the waveform the harmonic distortion of the output wave decrease, approaching zero as the number of levels approaches infinity.

Hence Multi- level inverters inverters offer a better choice at the high power end because the high volt- ampere ratings are possible with these inverters without the problems of high dv/dt and the other associated ones.

Kapil Jain, Assistant Professor in Department of Electronics & Communication,Institute of Information Technology & Management, Gwalior (M.P.), India.Mail id : kapiljn5@gmail.com

Pradyumn Chaturvedi, Assistant Professor in Department of Electrical Engineering, Samrat Ashok Technological Institute,Vidisha (M.P.), India. Mail id: pradymnc74@rediffmail.com

II. MULTILEVEL INVERTER TOPOLOGIES

The basic three types of multilevel topologies used are [10] [4]:

(1) Diode clamped multilevel inverters
(2) Flying capacitors multilevel inverter or capacitor clamped multilevel inverter
(3) Cascaded inverter with separate DC sources.

A .Diode Clamped Multilevel Inverters

The diode clamped multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m level diode clamp inverter needs (m-1) capacitors on the dc bus.

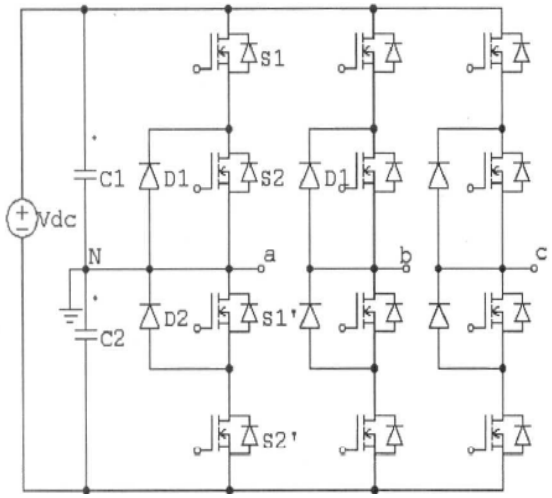

Fig. 1 Diode Clamped Three Level Inverter

In this paper, diode clamped multilevel inverters topology is used shown in fig 1.

B. Flying Capacitor Multilevel Inverter

It uses ladder structures of dc side capacitors where the voltage on each capacitor differs from that of the next capacitor. To generate m- level staircase output voltage, (m-1) capacitors in the dc bus are needed. The size of the voltage increment between two capacitors determines the size of the voltage levels in the output wave.

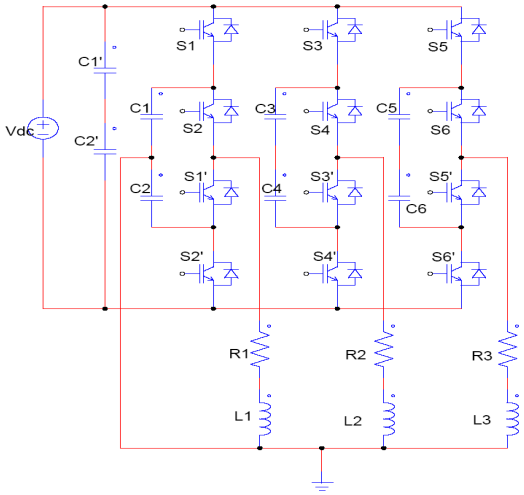

Fig. 2 Flying Capacitor Three Level Inverter

C. Cascaded Inverters with Separate DC Source

This inverter is nothing but the sereis connection of single connection of single pahse inverters with separate dc source. This inverter can be avoide extra clamping diodes or voltage balancing capacitors.

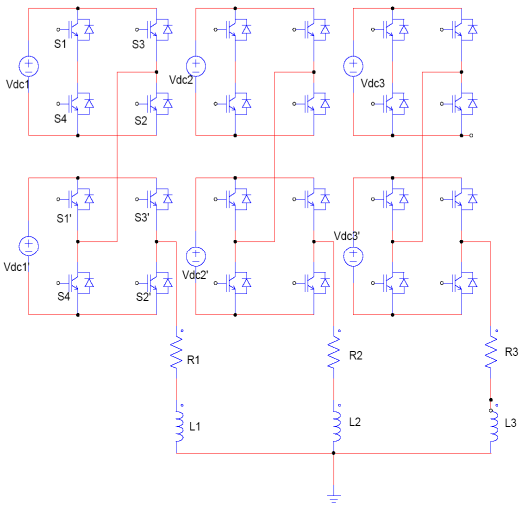

Fig. 3 Cascaded Inverters with Separate DC Source

III. SYSTEM CONFIGURATION

The proposed three level inverter with RL load, which consists of voltage source inverter. The inverter model connected to the RL load is controlled to produce the staircase voltage and sinusoidal current. Three levels PWM based on constant carrier frequency for three level inverter systems is proposed to reduce the harmonic contents in the output voltage and decrease the voltage rating of the power device.

IV. CONTROL TECHNIQUE OF THREE LEVEL INVERTER

The sinusoidal PWM technique is very popular for industrial converters. Fig 4. Shows the general principle of SPWM, where an isosceles triangle carrier wave of frequency fc is compared with the fundamental frequency f sinusoidal modulating wave, and the points of intersection determine the switching points of power devices. There are 8 switches states in the traditional three phase two level inverter. However, there are 27 switches states in three level inverter.

Three level pulse width modulated waveforms can be generated by sine carrier PWM. Sine carrier PWM is generated by comparing the three reference control signals with two triangular carrier waves [12] [6].

$V_{io} = V_{dc}/2 \quad , \quad V_{ref,\,i} > V_{tri,1}$

$= 0 \quad , \quad V_{tri,1} > V_{ref,\,i} > V_{tri,2}$,where i = a, b or c

$= -V_{dc}/2 \quad , \quad V_{tri,2} > V_{ref,\,i}$

The three reference control signals are phase shift 120^0 each other with same amplitude. Two carrier waves are in phase each other with dc voltage offset. Two important parameters of the design process are amplitude modulation index $m_a = V_r/V_c$, where V_r is the amplitude of reference control signals, V_c is the peak amplitude of the carrier wave, and the frequency modulation index $m_f = f_c/f_r$ where f_c is the frequency of the carrier wave and fc is the carrier frequency.

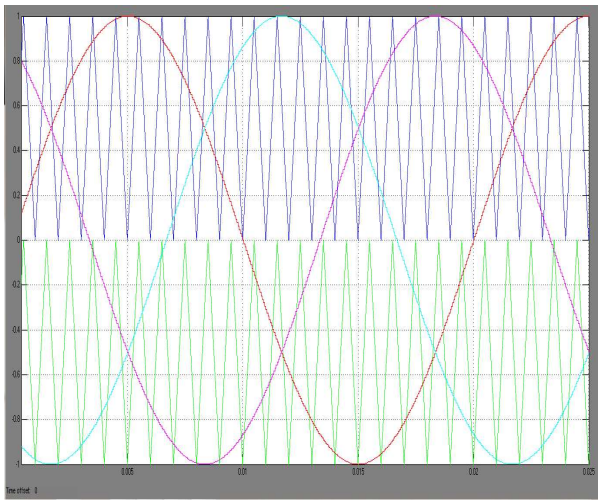

Fig 4. Control Pulse Generation in Three Level SPWM

V. SIMULATION RESULT

Simulation of various inverters using sinusoidal pulse width modulation was carried out with the help of "MATLAB 7.8". Simulation was carried out to observe the improvement in the line voltage THD and Line current THD for RL load as the inverter level increases from 2-level and 3-level. Following quantities have been observed.

1. Line voltage waveform
2. Line current and Line voltage waveform for RL load for two level inverter.
3. Line current and Line voltage waveform for RL load for three level inverter.
4. Substantial decrease in the THD as the frequency is increased.

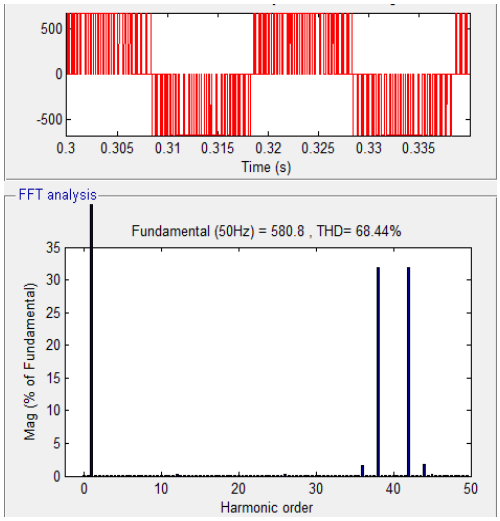

Fig 5. Harmonic Spectrum of Line Voltage of 2-level inverter for R= 15, L=24.2 mH

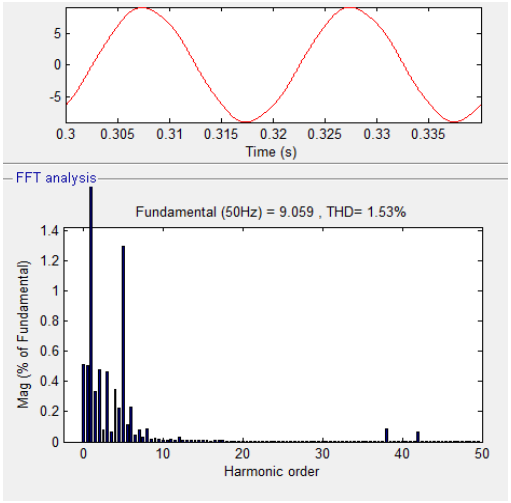

Fig 6. Harmonic spectrum of Line current of 2-level inverter for R= 15, L=24.2 mH

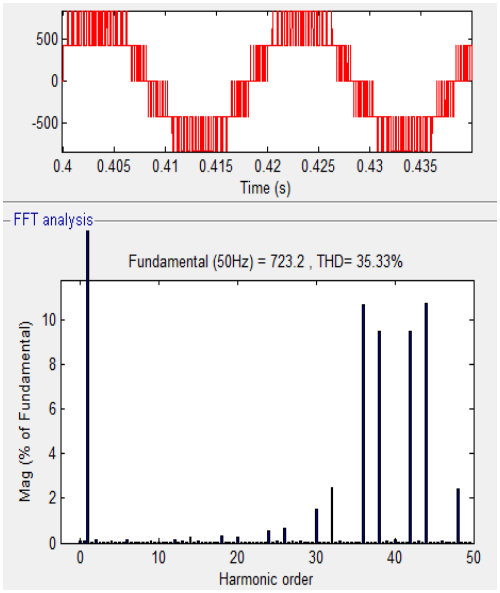

Fig 7. Harmonic spectrum Line Voltage of 3-level inverter for R= 15, L=24.2 mH

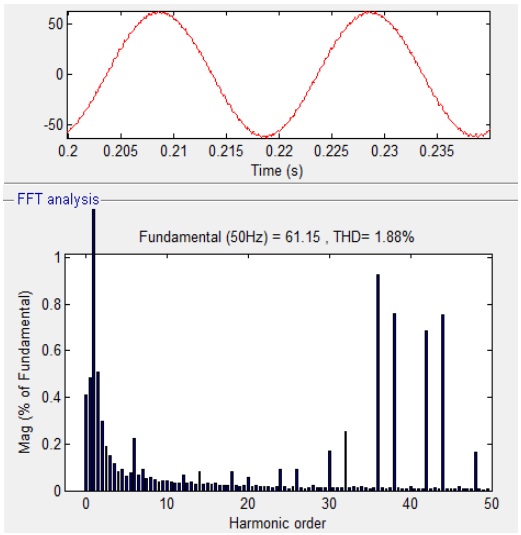

Fig 8. Harmonic of spectrum Line current of 3-level inverter for R= 15, L=24.2 mH

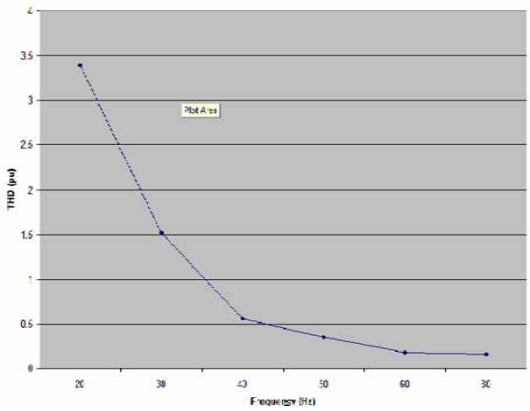

Fig. 9 Effect of Inverter o/p Frequency on Load Current THD for Fixed RL Load

VI. CONCLUSION

The simulation of the inverters namely conventional three and two level inverter was carried using sinusoidal pulse width modulation (SPWM) .it has shown that decrease in voltage and current THD in moving from two level inverter to three level inverter. This paper briefly explains theory of sinusoidal pulse width modulation (SPWM) for two and three level inverter and performance of both inverters was tested using RL load. It has shown that load current for three level inverter are much more sinusoidal and improvement in the line current waveform and decrease in the THD from two level to three level inverter and decrease in the THD as the frequency is increased.

REFERENCES

[1] J. S. Lai and F.Z. Peng "Multilevel Converters – A new breed of power converters" IEEE Trans. Ind Applicant , Vol. 32, May/June 1996.
[2] Jose Roderiguez, Jih-Sheng Lai and Fang Zheng Reng, "Multilevel Inverters" A survey of topologies ,control, and applications ",IEEE Trans. On Ind.Electronics, vol No.[4], August 2002.
[3] A. Nabae, I Takashashi, and H. Akagi, " A new neutral –point clamped PWM inverter," IEEE Trans. Ind Application Vol. No. IA-17,PP 518-523,Sept/oc 1981.
[4] P.K.Chaturvedi, S. Jain, Pramod Agrawal " Modeling , Simulation and

Analysis of Three level Neutral Point CLAMPED inverter using matlab/Simulink/Power System Blockst"
[5] Bor-Ren Lin & Hsin – Hung Lu " A Novel Multilevel PWM Control Scheme of the AC/DC/AC converter for AC Drives"IEEE Trans on ISIE, 1999. [6]
B. R. Lin & H- H Lu " multilevel AC/DC/AC Converter for AC Drives" IEEE Proceding electronics Power application, Vol 146, No. 4, July 1999.
[7] DAI Bin " A new control scheme for voltage Source Inverter Without DC Link Capacitor Under Abnormal Input Voltage Conditions" IEEE Tran.2009. [8]
K. Arab tehrani, H. Andriasioharana, I. Rasonarivo & F.M. Sargos " A Multilevel Inverter Model" IEEE Trans. 2008.
[9] Siriroj Sirisukprasert, Jih- Sheng Lai & Tina – Hua Liu "Optimum harmonics Reduction With A wide Range Of Modulation Indexes for Multilevel Converters" IEEE Trans Ind Application Electronics ,Vol 49 , No. 4, August 2002.
[10] G.Bhuvaneshwari and Nagaraju " Multilevel inverters – a comparative study" vol .51 No.2 march – april 2005.
[11] Siriroj Sirisukprasert " Optimum harmonics reduction".
[12] A. M. Massoud, S.J. Finney and B.W. Williams "Control Techniques for Multilevel Voltage Source Inverters" IEEE proce. 2003.
[13] B.R. Lin and H.H. Lu " Multilevel AC/DC/AC converter for AC drives" IEE E Proc.—Electr. Power Application, Vol. 146, No. 4, July 1999.
[14] M. A. EL- Barky, S.H. Arafah " Simulation and Implemetaion of Three Phase Three Level Inverter" SICE july 25- 27, 2001, nagoya..