A 23pW, 780ppm/°C Resistor-less Current Reference Using Subthreshold MOSFETs

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***Abstract*— This paper proposes a MOSFET-only, 20pA, 780ppm/ºC current reference that consumes 23pW. The ultra-low power circuit exploits subthreshold-biased MOSFETs and a complementary-to-absolute temperature (CTAT) gate voltage to compensate for temperature dependency. The design shows low supply voltage sensitivity of 0.58%/V and a load sensitivity of 0.25%/V.**

I. Introduction

Sub-nano ampere current references are of increased interest recently, as micro-scale sensor nodes and bio-implantable systems with limited power budgets gain popularity [1]. These systems use ultra-low-power mixed signal circuits such as oscillators and analog amplifiers, which require current references with low power overhead as key building blocks.

To motivate the need for an ultra-low power current reference with low temperature dependence, consider a recently reported 65nW CMOS temperature sensor [2]. This sensor uses multiple subthreshold-mode operational amplifiers, each of which consumes 100s of pA. The amplifiers make up 6% of total analog front-end power consumption at room temperature. However, due to the lack of a temperature-compensated current reference, amplifier power increases exponentially with temperature such that they consume 52% of total analog front-end power at 100ºC. Adopting the current reference circuit proposed in this paper would limit the amplifier and current reference overhead power to only 6% at 100ºC, reducing total analog front-end power from 56.2nW to 14.9nW at 100ºC.

Many conventional current reference circuits are variations of the β-multiplier current reference (Fig. 1(a)). However, this type of reference is unsuitable for sub-nA current generation as it requires an extremely large resistor of 1GΩ or more. Further, a start-up circuit is needed to prevent the circuit from becoming trapped in an undesired operating point, adding area overhead. The authors of [3] replace the resistor with a MOSFET to create a subthreshold version of the β-multiplier, however the circuit remains in the nW range (88nW@1.3V).

Other proposed current references employ a reference voltage and a resistor (Fig. 1(b)) [5,6], achieving a temperature coefficient (TC) as low as 24.9ppm/ºC [5]. However, those circuits consume µW's and their use of resistors complicate sub-nA current generation. Also, polysilicon resistors vary by up to ±25% [7]; this variability is independent of transistor process variation, potentially worsening process sensitivity.

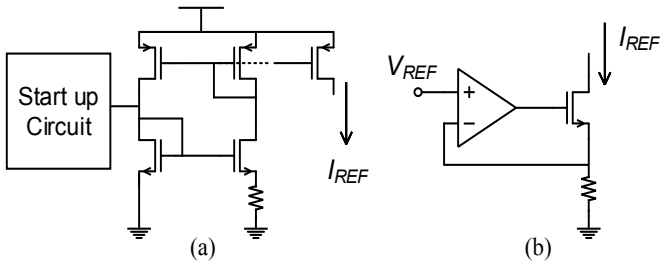

Fig. 1. Conventional current references based on: (a) β-multiplier; (b) voltage reference divided by resistance.

This paper proposes a new topology to generate a sub-nA (20pA) level reference current with very low power overhead. It shows 780ppm/ºC TC and consumes 23pW, which is >50× smaller than the lowest power consumption reported previously [4]. This work also describes techniques to improve supply voltage and load voltage regulation.

II. Proposed Circuit

In this section, an overall circuit diagram is first introduced, followed by a detailed explanation of each block. The proposed design has three components: an ultra-low-power line regulator, a CTAT gate voltage generator, and a cascoded subthreshold MOSFET output stage. In addition, an optional current level selector (CLS) can be incorporated to provide a tunable range of current magnitudes. Fig. 2 shows the implementation of the overall circuit, including the detailed structure of each of the three blocks in Fig. 3.

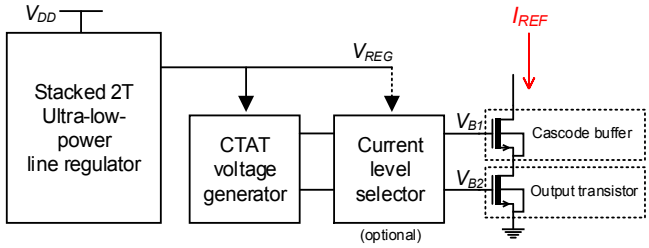

Fig. 2. Block diagram of the proposed current reference.

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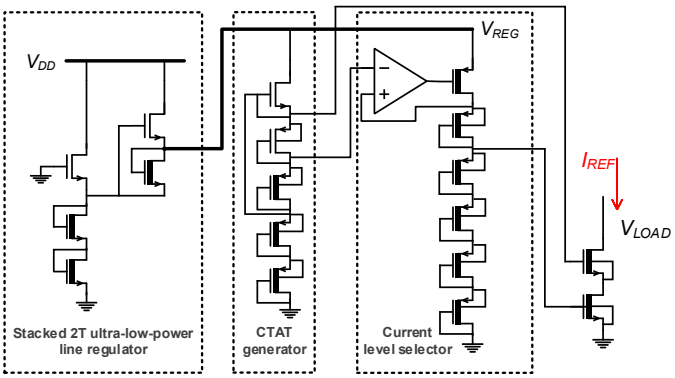

Fig. 3. Circuit diagram of the proposed current reference circuit.

A. Temperature Compensation

The basic idea of this work is to use a MOSFET subthreshold current as the reference current (I_{REF}). Subthreshold current is well known to increase exponentially as temperature (T) increases; this arises due to transistor threshold voltage (V_{th}) linearly decreasing with T, and V_{th} appearing in the exponential term of (1).

$$I_{REF} = \mu(T_r)\left(\frac{T}{T_r}\right)^{-1.5} C_{ox}\frac{W}{L}\left(\frac{kT}{q}\right)^2 e^{\left(\frac{q(V_{gs}-V_{th})}{mkT}\right)} \quad (1)$$

Meanwhile, gate to source voltage (V_{gs}) also appears in the exponential term. In this work, we first scale V_{gs} linearly with T to cancel out the exponential increase of I_{REF}, to the first order. The targeted V_{gs} is modeled by (2), where V_{gs0} is V_{gs} at 0K, V_{th0} is the threshold voltage at 0K, and κ_{vth} and κ_{vgs} are temperature coefficients. We then apply (2) to the current equation (1) to obtain a first-order compensated reference current equation (3). To simplify (3), the temperature-independent terms are combined into α_1 and α_2 in (4).

$$V_{gs} = V_{gs0} - \kappa_{V_{gs}}T,\ V_{th} = V_{th0} - \kappa_{V_{th}}T \quad (2)$$

$$I_{REF} = \alpha_1 T^{\frac{1}{2}} e^{\frac{\alpha_2}{T}} \quad (3)$$

$$\alpha_1 = \mu(T_r)C_{ox}\frac{W}{T_r^{-1.5}L}\frac{k^2}{q^2}e^{\frac{q(\kappa_{V_{th}}-\kappa_{V_{gs}})}{mk}},\ \alpha_2 = \frac{q(V_{gs0}-V_{th0})}{mk} \quad (4)$$

The first order exponential dependency on T is cancelled in this way, however second order effects remain. Using the proper technology dependent parameters and physical constants, Equation (3) is modeled in MATLAB to visually represent the remaining T dependency (Fig. 4).

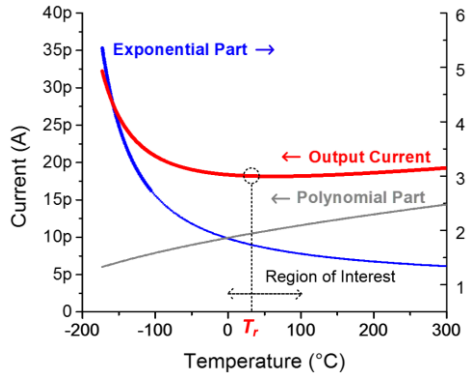

Fig. 4. MATLAB simulation of the current model given in Equations (1)-(4).

In (3), I_{REF} has two components; $\sqrt{T}$ and $exp(\alpha_2/T)$. The polynomial term increases, while the exponential term decreases with T, creating some cancellation of each other with respect to T. Note that, Fig. 4 spans from -200°C to 300°C to illustrate the broad tendency of each term. In addition, third order effects come into play, such as well leakage, but are found to be negligible in the range of 0°C to 80°C.

As shown in Fig. 4, the concave nature of I_{REF} guarantees the existence of a temperature point where I_{REF} is temperature-independent ($\partial I_{REF}/\partial T = 0$). To minimize the impact of the second order temperature dependency, we choose a target V_{gs} such that this temperature-independent point is set to 25°C (= T_r). We differentiate (3) with respect to T to obtain (5), which is the temperature dependency of I_{REF} at any T. We then set (5) to 0 at $T = T_r$, as shown in (6). Using (6), we obtain the required value of $V_{gs0|Tr}$ in (7), such that temperature dependence is minimized over a range of temperatures near 25°C.

$$\frac{\partial I_{REF}}{\partial T} = \alpha_1 e^{\frac{\alpha_2}{T}} T^{-\frac{1}{2}}\left(\frac{1}{2} - \alpha_2 T^{-1}\right) \quad (5)$$

$$T\left(\frac{\partial I_{REF}}{\partial T} = 0\right) = 2\alpha_2 = T_r \quad (6)$$

$$V_{gs0\,|\,T_r} = mkT_r/2q + V_{th0} \quad (7)$$

In (7), $V_{gs0|Tr}$ refers to the required gate voltage at 0K to set T_r as the temperature independent point. Note that the proposed circuit will control V_{gs}, hence both $V_{gs0|Tr}$ and κ_{vth} (in Equation (2)) can be tuned to achieve a target T range.

B. CTAT Voltage Generator

This section explains how V_{gs} can be generated to achieve (7), and also introduces several techniques to accomplish lower supply sensitivity and reduced power. The linear CTAT voltage is generated using a stack of diode-connected transistors with different sizes (Fig. 5(a)) [5,9].

This traditional CTAT generator is modified as seen in Fig. 5(b). High-Vth (HVT) devices are used to minimize power consumption while a native NMOS is added at the top of the stack to reduce supply sensitivity from 4,042%/V to 4.39%/V. An additional supply rejection stage, comprised of two-stacked 2T voltage reference [8] (Fig. 3, left), further decreases supply voltage sensitivity by a factor of 36× (Fig. 6). Fig. 5(c) shows the addition of two PMOS transistors, which increases the TC to the required value, from −0.72mV/°C to −1.26mV/°C (Fig. 7). Fig. 9 shows that $V_{CTAT\text{-}C}$ slope and temperature coefficient of the output current can be controlled by changing transistor width ratio of nominal-Vth (NVT) PMOS and HVT PMOS in CTAT generator.

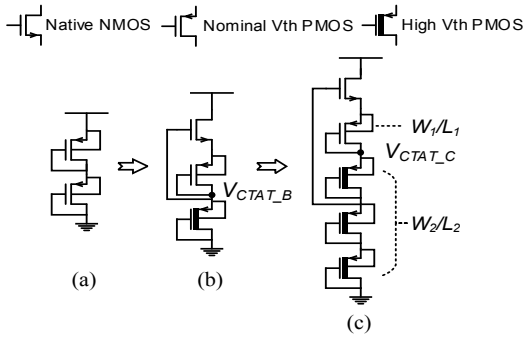

Fig. 5. (a) Conventional CTAT voltage generator. Modified designs: (b) for improved supply noise rejection; (c) additional MOSFETs for higher TC.

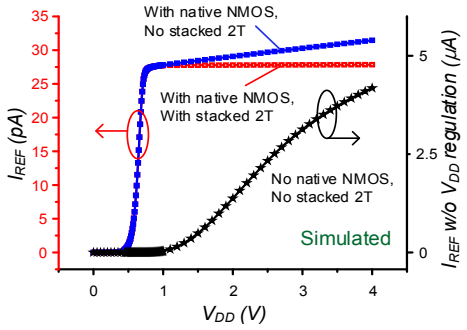

Fig. 6. Output current vs. V_{DD} with/without V_{DD} regulation techniques.

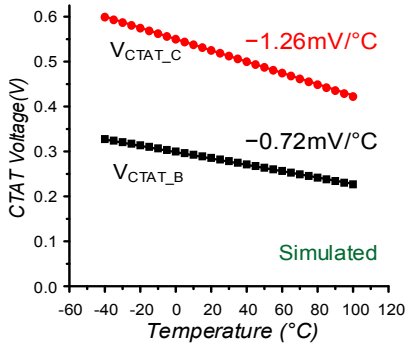

Fig. 7. CTAT voltage generated by diode-connected transistor stacks in Fig. 5.

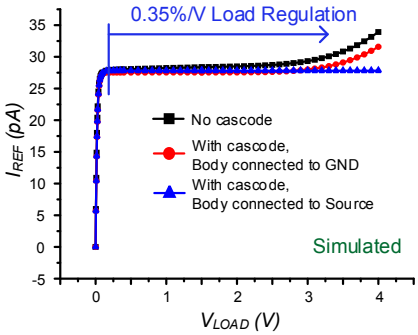

Fig. 8. Load sensitivity of output current using techniques in Fig. 5.

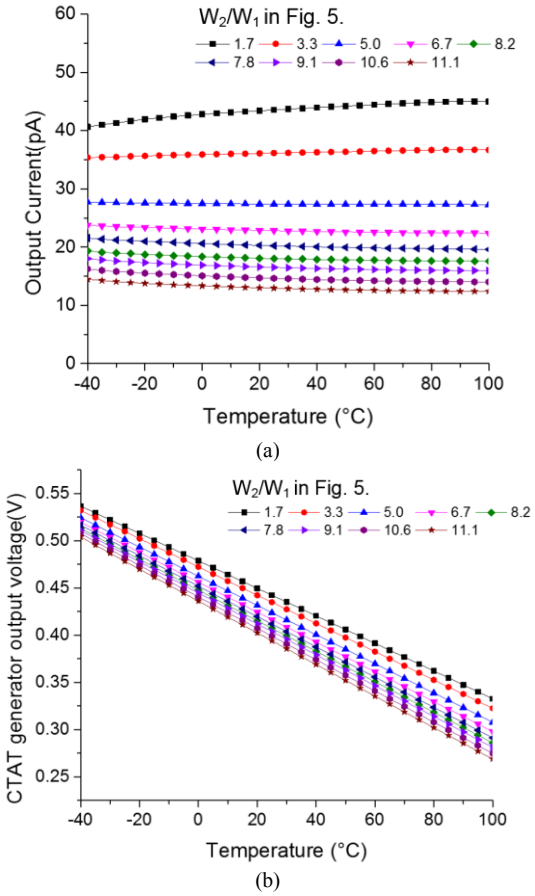

Fig. 9. Simulation result of (a) output current, (b) CTAT generator output voltage with different W_2/W_1 in CTAT generator stack of Fig. 5.

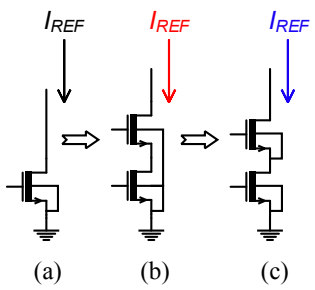

Fig. 10. Output stage configurations: (a) one subthreshold-biased NMOS; (b) with cascode buffer; (c) body tied to its own source.

The V_{th} of the output transistors ($V_{th,out}$) in Fig. 2 vary across process corners, resulting in considerable change in the reference current. This is mitigated by using short-channel HVT devices for the lower three transistors and long-channel NVT devices for the upper transistor in the CTAT generator (Fig. 5(c)). This results in the voltage levels of V_{B1} and V_{B2} to track that of the $V_{th,out}$ with a correlation coefficient of 0.9983. For example, at slow corner, V_{th} of short-channel HVT devices increases more than that of long-channel NVT devices; in the stack, V_{CTAT_C} increases as it can be seen as V_{th} divider, thus $V_{th,out}$ and V_{CTAT_C} moves in the same direction, alleviating the effect of global process variation.

C. Output Stage

Using the subthreshold current as I_{REF} provides an inherent advantage in the load sensitivity because it is nearly independent of V_{DS} as long as it exceeds 3-4kT/q [8]. However, drain-induced barrier lowering (DIBL) increases load sensitivity to 4.83%/V (simulation). To address this, we use a cascode stack on the output transistor to buffer the drain voltage of the output transistor (Fig. 10(b)), reducing load sensitivity to 3.48%/V. To further reduce load sensitivity, the cascode MOSFET body is tied to its own source to prevent substrate current induced body effect (Fig. 10(c)). This yields a load sensitivity of 0.35%/V from 0.1V to 4V (simulation, Fig. 8).

III. Measurement Results

The proposed current reference was fabricated in 0.18μm CMOS. Fig. 11 shows the measured output current across temperature, which maintains its desired level within 780ppm/°C from 0°C to 80°C. Fig. 12 shows measured line sensitivity of 0.58%/V for V_{DD} ranging from 1.2V to 4V. Load sensitivity measurement results are shown in Fig. 13, showing load sensitivity of 0.25%/V for V_{LOAD} between 0.27V and 3V. Fig. 14 is the photograph of the fabricated chip.

Fig. 15 shows previously reported current references in terms of TC, power consumption, and I_{REF}. The proposed current source consumes the lowest power among the shown current references and also enables the lowest regulated output current level. The output current levels of 10 different chips were measured, with results shown in Fig. 16, both with and without calibration. After calibration, the distribution has a mean current level of 20.79pA and standard deviation of 0.4pA.

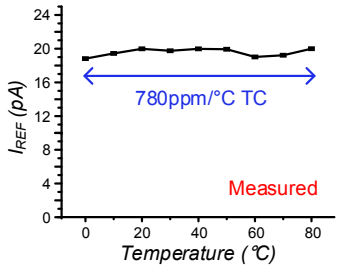

Fig. 11. I_{REF} across temperature.

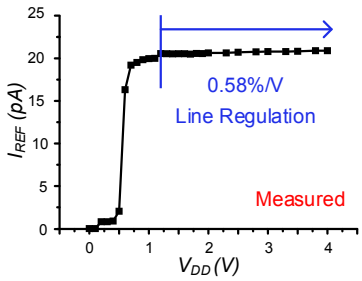

Fig. 12. I_{REF} across supply voltages.

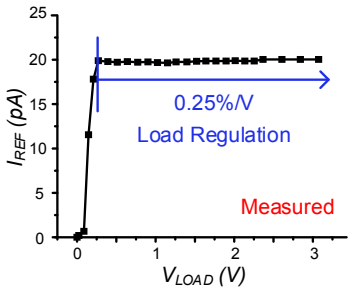

Fig. 13. I_{REF} across load voltages.

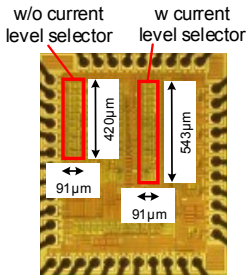

Fig. 14. Die photo.

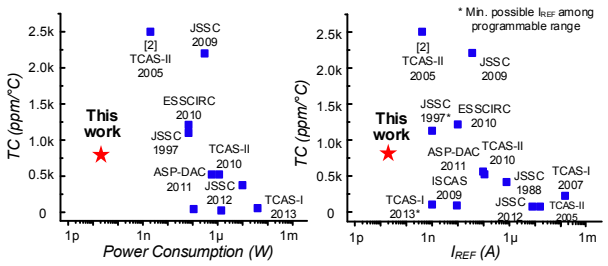

Fig. 15. Temperature coefficient of reported current reference circuits over power consumption (left) & I_{REF} (right).

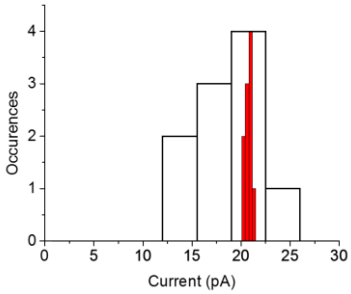

Fig. 16. Measured current distribution before calibration (black line) and after calibration (red).

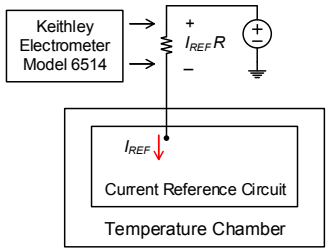

Fig. 17. Testing scheme for sub-nA current measurement.

Measuring sub-nA currents can be challenging, even with specialized equipment such as electrometers targeting very low current measurements. Hence, we use a scheme that converts current to voltage by generating an IR drop; this eases measurement as voltage can be characterized with very high accuracy and extremely high impedance (>200TΩ) with an electrometer. As shown in Fig. 17, current reference test chips are placed inside a temperature chamber and the output current is configured to flow through an off-chip resistor that is held at room temperature. This off-chip resistor is chosen to be 500MΩ such that the voltage drop across it is in the proper electrometer measurement range while ΔV_{LOAD} across temperature is negligible.

TABLE. I PERFORMANCE SUMMARY & COMPARISON.

	This Work	[3] ESSCIRC 2010	[4] TCAS-II 2005	[5] JSSC 2012	[6] JSSC 2008
Process (nm)	**180**	350	1,500	180	500
Temp. (°C)	**0 – 80**	-20 – 80	-20 – 70	0 – 100	0 – 80
V_{DD} (V)	**> 1.2**	> 1.3	> 1.1	1*/1.2**	2.3
I_{REF} (A)	**20p**	9.95n	410p	7.81µ	16 – 50µ
Power (W)	**23p**	88.5n	2n	1.4µ*/32.7µ**	>31µ
TC (ppm/°C)	**780**	1,190	2,500	24.9*	<130
Line Reg. (%/V)	**0.58**	0.046	6	0.13**	N/A
Load Reg. (%/V)	**0.25**	N/A	N/A	N/A	<1
Chip Area (μm^2)	**38.2k (w/o CLS) 48.4k (w/CLS)**	120k	46k	23k*/123k**	15k

* Core only ** with Bandgap Reference

IV. CONCLUSION

We propose a 23pW 780ppm/°C current reference circuit with line sensitivity of 0.58%/V and load sensitivity of 0.25%/V. This work can be adopted in micro-scale sensor applications to dramatically reduce analog power consumption across temperature.

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