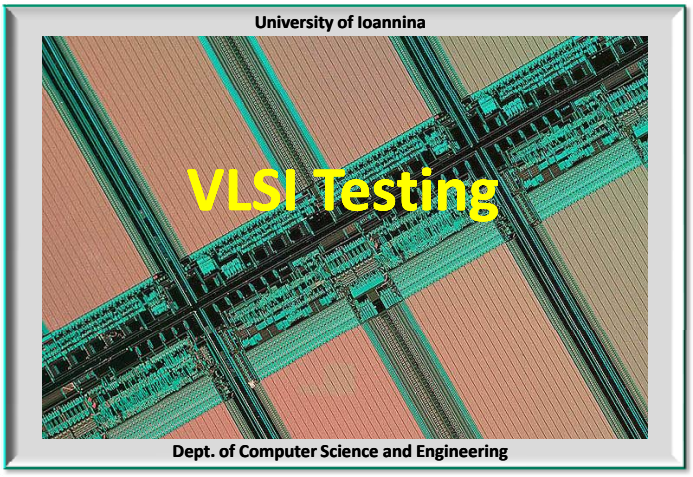
CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES



Y. Tsiatouhas

CMOS Integrated Circuit Design Techniques

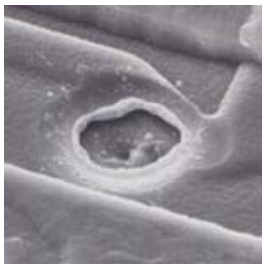
Overview

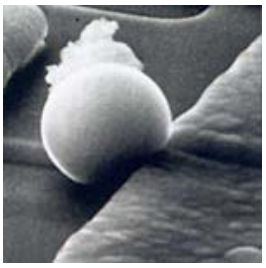
VLSI Systems
and Computer Architecture Lab

1. *VLSI testing*
2. *On-chip/off-chip, on-line/off-line testing*
3. *Fault models*
4. *Yield – Defect level – Fault coverage*
5. *Control/observation points*
6. *Path delay fault testing*
7. *Circuit partition/segmentation*

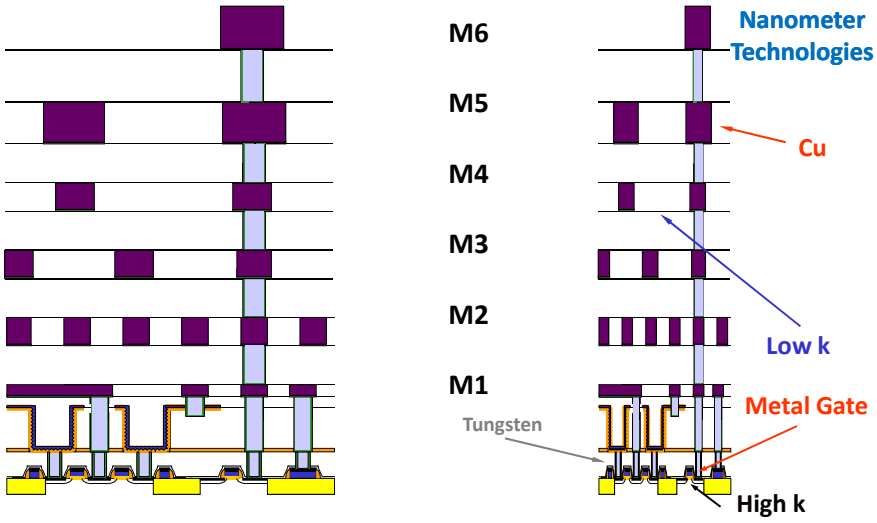
Testing

With the term Integrated Circuit (IC) or VLSI Testing we refer to those procedures that take place after chip fabrication in order to detect possible manufacturing defects.

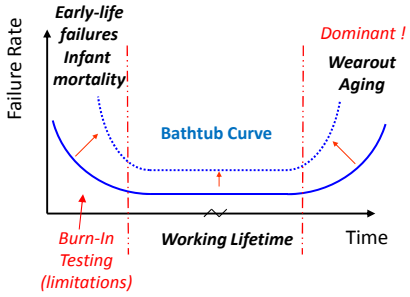




CMOS Technology Scaling



Testing Necessity



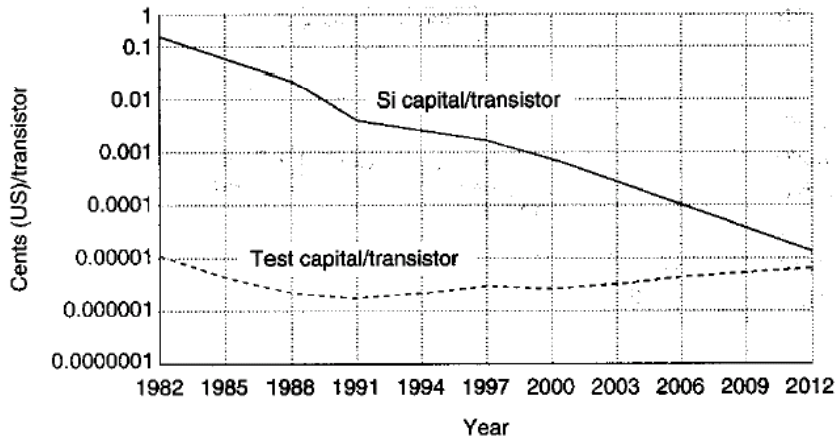
- Imperfections in chip fabrication may lead to manufacturing defects.

$$Y = \frac{\#\_of\_acceptable\_parts}{total\_\#\_of\_fabricated\_parts}$$

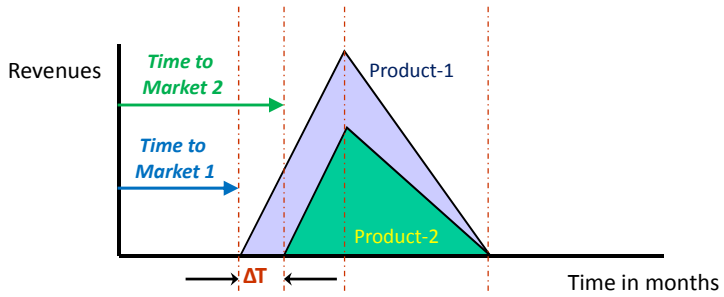
- The *manufacturing yield (Y)* (*κατασκευαστική απόδοση*) depends on the used technology, the silicon area and the layout design.
- Early in a technology development the yield is too low (even less than 10%) and continuously rises (even above 95%) as technology is getting mature.

Rule: The earlier a defect is detected the less the cost for the final product. The rule of ten says that the cost of detecting a defective device increases by an order of magnitude as we move from a manufacturing stage to the next (device → board → system)

The Cost of Testing



Reliability and Time to Market



- A reliable product with small time to market will provide higher revenues than a second product with a greater time to market.
  - Testing procedures at the minimum cost in time and resources are required!

Off-Chip and On-Chip Testing

Off chip testing: The test procedures are applied by external to the chip test equipments (Automatic Test Equipment – ATE or Tester).

On chip testing: Embedded, on-chip, resources are provided in order to support the testing procedures.

On-Line and Off-Line Testing

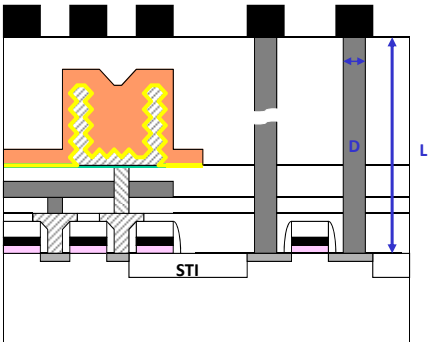
- **On-line testing**: Testing procedures are applied in the field of operation.
  - **Concurrent testing**: Testing is performed concurrently with the circuit operation in the field, during the normal mode.
  - **Periodic testing**: Testing is performed periodically, during idle times of the circuit operation.
- **Off-line testing**: Testing procedures are applied out of the field of operation, usually after fabrication (manufacturing testing).

Defects – Faults – Errors

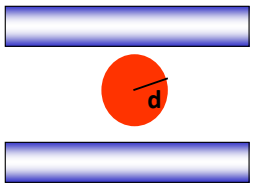
- ***Defects (Ελαττώματα):*** are circuit failures and malfunctions due to the manufacturing process (e.g. short-circuits, opens e.t.c.).
- ***Faults (Σφάλματα):*** model the influence of defects on the circuit operation (e.g. a line (node) is permanently stuck-at "1" or "0").
- ***Errors (Λάθη):*** are the incorrect logic responses of the circuit under the presence of faults.

Open and Short-Circuit Defects

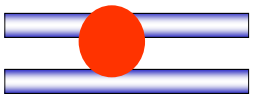
Contact aspect ratio: L/D = 7/1
0.18μm Technology



Early Technologies

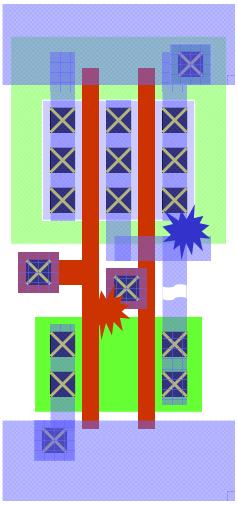


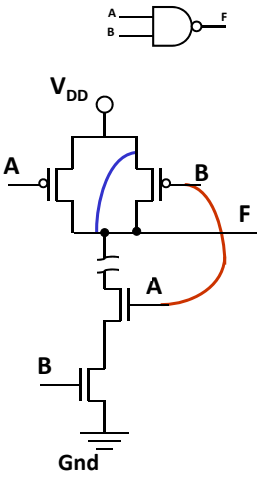
d = defect size



Nanometer Technologies

Fault Models





- **Stuck-At Faults (Μόνιμης Τιμής):** a circuit node is permanently fixed to a logic value.
- **Transistor Stuck-On Faults:** a transistor is permanently in a conducting state.
- **Transistor Stuck-Open Faults:** a transistor is permanently in a non-conducting state.
- **Bridging Faults:** short-circuits between adjacent nodes.
- **Delay Faults**: signal propagation delays (in one or more paths) that are outside the circuit specifications.

Permanent and Temporary Faults

- ***Permanent Faults (Μόνιμα Σφάλματα)*** are those faults that have a permanent impact on the circuit operation.
- ***Temporary Faults (Πρόσκαιρα Σφάλματα)*** are those faults that do not have a permanent impact on the circuit operation. They are categorized as:
  - ***Transient (Παροδικά)***: non-repeated faults due to random effects like power supply disturbances, electromagnetic interference, radiation e.t.c.
  - ***Intermittent (Διαλείποντα)***: repeated faults due to the degradation of the circuit parameters (wearout, aging).

Yield Loss and Yield Enhancement

- There are two types of yield loss in IC manufacturing:
  - ***Catastrophic yield loss***: due to random defects.
  - ***Parametric yield loss***: due to process variations.

- Yield enhancement techniques:
  - ***Design for Manufacturability***: layout design rule adaption in order to improve the manufacturability.
  - ***Design for Yield***: process improvements to enhance yield.
  - ***Design for Diagnosis***: techniques that provide access to proper information in order to find the root cause of a failure. This will help to improve the layout design and/or the manufacturing process.

Yield and Defect Level

The targets (from design and fabrication point of view) are:

↑ Yield (Y)= $\dfrac{\text{number of defect free ICs}}{\text{total number of fabricated ICs}}$

Mathematical model: $Y = \left[\left(1 - e^{-A \cdot D}\right) / A \cdot D\right]^2$

A = die area

D = defect density

⇓

↓ Defect Level (DL)= $\dfrac{\text{number of defective ICs that pass the test}}{\text{total number ICs that pass the test}}$

These are test escapes!

DL is measured in defective parts per million (DPM) – < 100 DPM ⇒ high quality

Fault Coverage

Given that the yield is a priori less than 1, it is a prerequisite of a testing procedure to provide the highest possible *fault coverage* (*κάλυψη σφαλμάτων*).

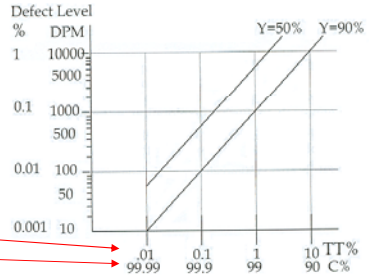
↑ Fault Coverage (T) = $\dfrac{\text{number of detected faults}}{\text{total number of possible faults}}$

⇓

Theoretical relation among defect level, fault coverage and yield:

$$DL = 1 - Y(1 - T)$$

$$DL = (1 - T)^{-\ln(Y)}$$ approximation for small values of DL



TT = (1-T)

C = stuck-at fault coverage

Fault Detection

The detection of faults in a circuit consisting of many hundred-millions up to few billions of transistors is an open issue. Possible approaches:

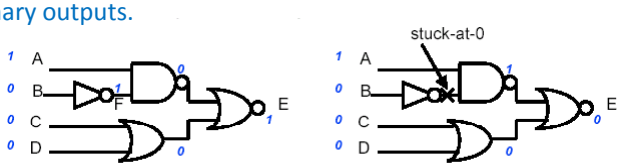
- Application of all possible input combinations and observation of the circuit responses.
  Impractical solution due to the huge number of all possible combinations.
- Use of efficient algorithms for the generation of a reduced set (***test set***) of input combinations (***test vectors***) along with the corresponding responses, which is capable to detect "all" possible faults of the fault model under consideration.
  Main strategy: "divide and conquer"
- Assist testing with embedded design for testability (DfT) techniques.
  Main strategy: "divide and conquer"

Desired fault coverage 100%.
In practice a fault coverage of 90–99.9% is achieved depending on the fault model and the circuit under test.

Testability

Testability is defined as a measure of the ability to detect the faults of the fault model under consideration in a *circuit under test* (*CUT*). It depends on the:

- ***Controllability (Ελεγξιμότητα):*** is a measure of the ability to set a node in a predefined logic state using proper primary input values (vectors).
- ***Observability (Παρατηρησιμότητα):*** is a measure of the ability to determine the logic state of a node by observing the circuit responses at the primary outputs.



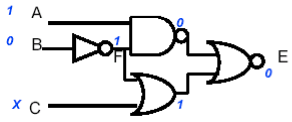
Fault free circuit *Circuit with stuck-at faults*

Fault detection is a process where a fault is sensitized by applying proper values at the primary inputs of the circuit, so that an error is generated at a circuit node, and afterwards this error is propagated to a primary output to be observed.

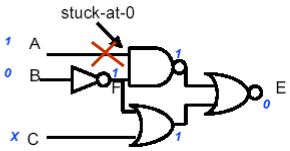
Re-convergent Fan-Out Points

The presence of *re-convergent fan-out points (σημείων επανασύγκλισης σημάτων)* makes fault detection a hard task. This is due to the fact that in such cases it is not always feasible to independently set proper values at various circuit nodes in order to sensitize a fault and/or propagate the generated error to a primary output.

In the example that follows, there is not any proper value for node B that will sensitize the fault and in parallel will permit the propagation of the generated error to the output E. The re-convergent fan-out point is node E.



Fault free circuit

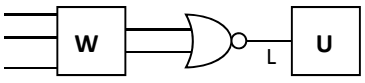


Circuit with stuck-at faults

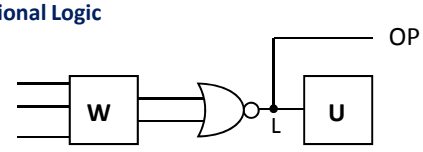
Control – Observation Points (I)

1

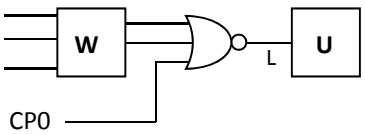
Combinational Logic



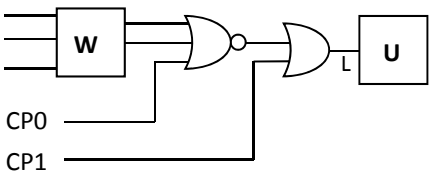
Original Circuit



Observation Point Insertion

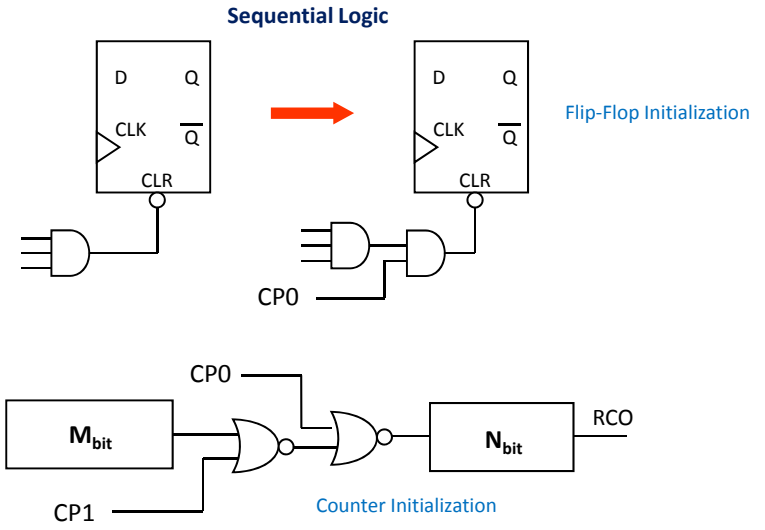


"0" Control Point Insertion



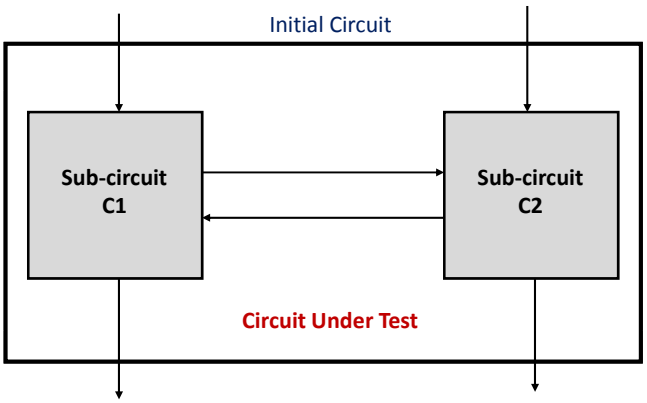
"0" and "1" Control Point Insertion

Control – Observation Points (II)



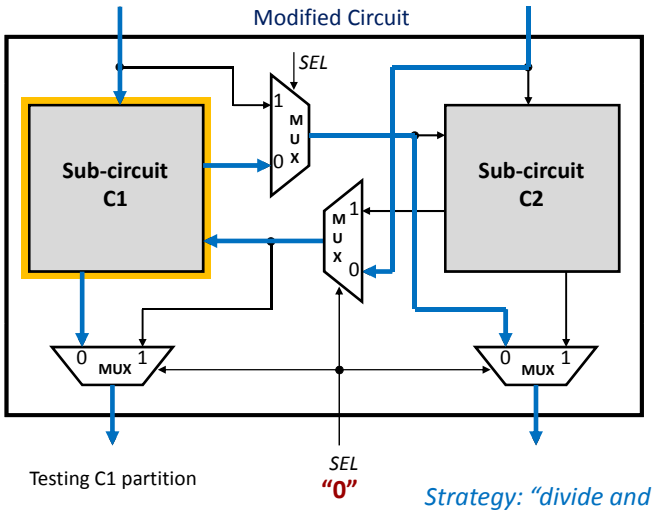
Circuit Partitioning (I)

2



Circuit Partitioning (II)

(Τμηματοποίηση Κυκλώματος)



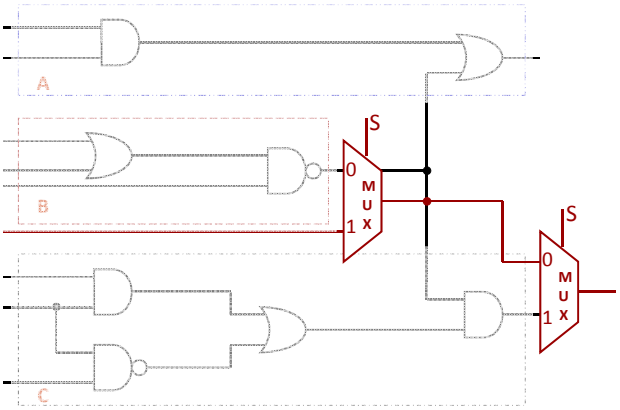
Strategy: "divide and conquer"

Circuit Segmentation

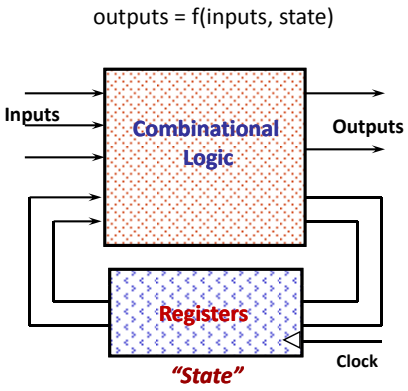
(Κατάτμηση Κυκλώματος)

S="0"
A & C are transparent

S="1"
B is transparent



Hard Task: Sequential Logic Testing



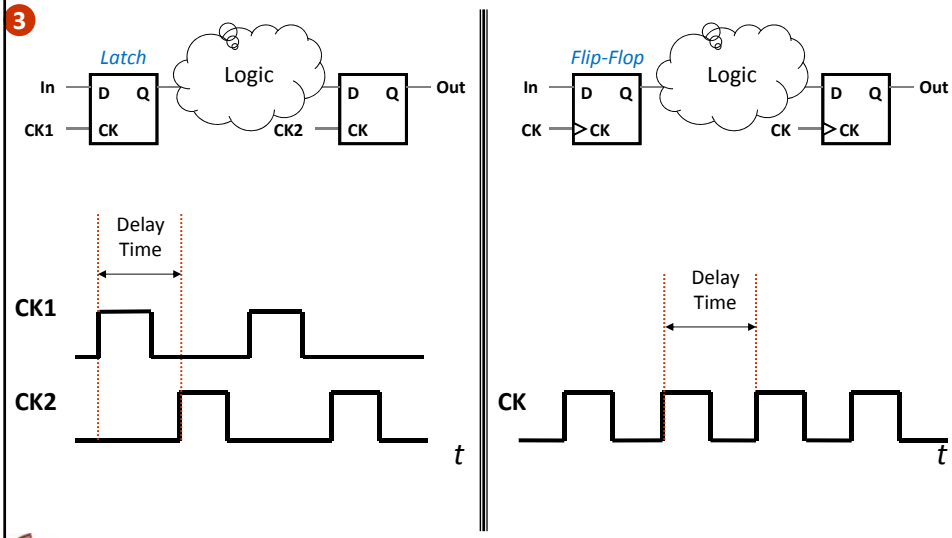
In sequential circuits the initial state (register's values) is not known by default . Consequently, the sensitization of faults and the propagation of the corresponding erroneous responses turns to be a hard task.

A solution is to use techniques for the proper initialization of the circuit state to known values.

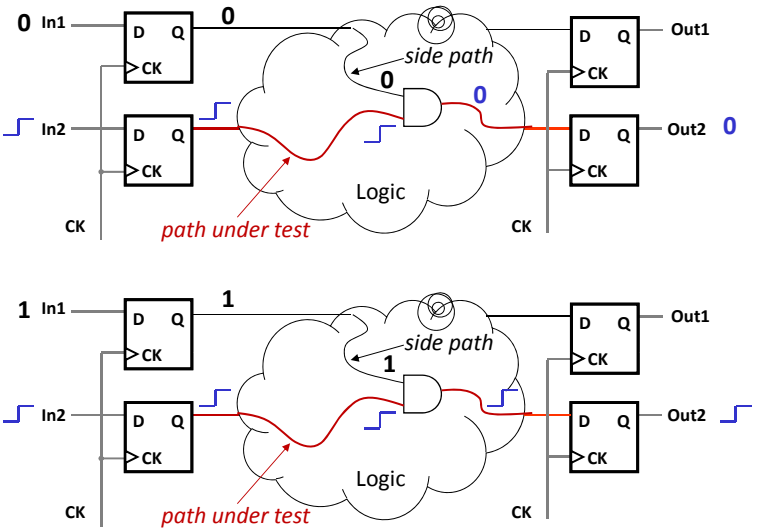
- Application of proper test vector sequences and/or the use of *Set*/*Reset* signals to setup the required state.
- Development of efficient techniques to set the initial state and observe the subsequent state after the response of the circuit.

Path Delay Fault Testing (I)

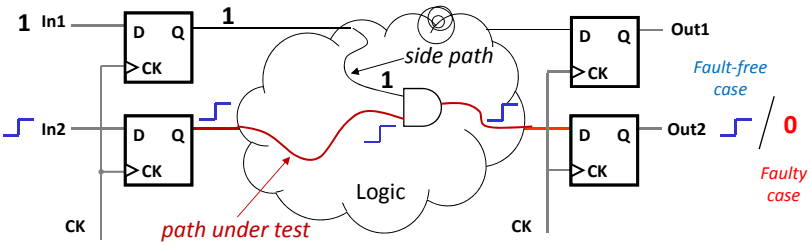
3



Path Delay Fault Testing (II)



Path Delay Fault Testing (III)



V1 = <10> ← Initializing test vector
V2 = <11> ← Path activation test vector

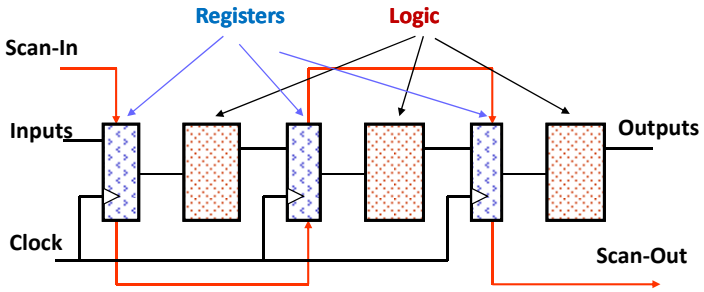
A path delay fault requires at least a pair of subsequent test vectors to be detected. The first test vector initializes the circuit while the second test vector activates the path under test.

Design for Testability

Design for testability (DFT) techniques are today a common practice to meet the reliability levels required in modern integrated circuits (ICs). According to this approach, proper testing circuitry is embedded along with the functional *circuit under test* (*CUT*) aiming to alleviate the testing process and enhance testability.

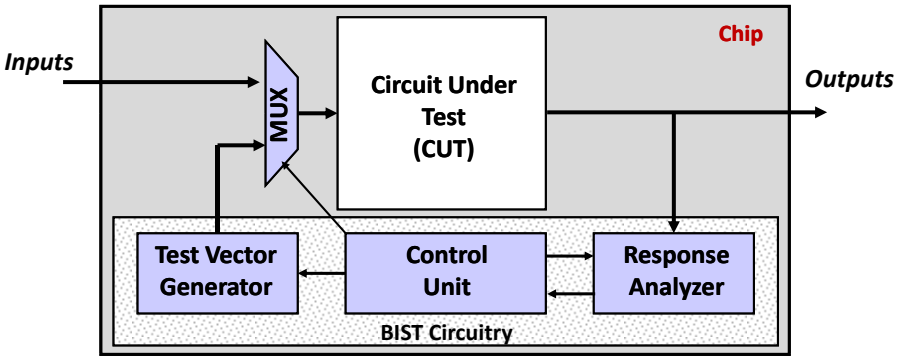
- Scan testing techniques (τεχνικές σειριακής σάρωσης).
  They provide full controllability and observability of the circuit's internal states.
- Built-In Self Test - BIST techniques (τεχνικές ενσωματωμένου αυτοελέγχου).
  Proper circuits are embedded in an IC to enable its self-testing. These circuits provide test vectors to the circuit under test (CUT) and monitor its responses to detect errors.
  BIST circuits can be also exploited for on-line testing.
- I_{DDQ} testing (or current monitoring) techniques.
  Power consumption is the criterion to discriminate defective from defect free ICs.
- Test standards.
  Existing test standards, like the IEEE 1149.1 and IEEE 1500, provide a common way to perform testing procedures in nanometer ICs.

Scan Testing



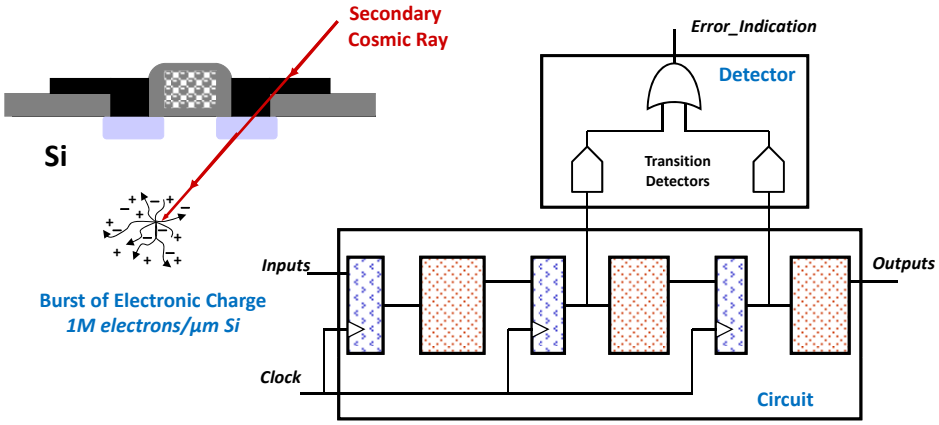
All the memory elements (latches or Flip-Flops) are properly connected to form a unified shift register (*scan register*). This way the internal state of the circuit is determined (controlled) by shifting in (*scan-in*) to the scan register the required test data to be applied to the combinational logic. Moreover, the existing internal state (previous logic response) can be observed by shifting out (*scan-out*) the data stored into the scan register.

Built-In Self Test (BIST)



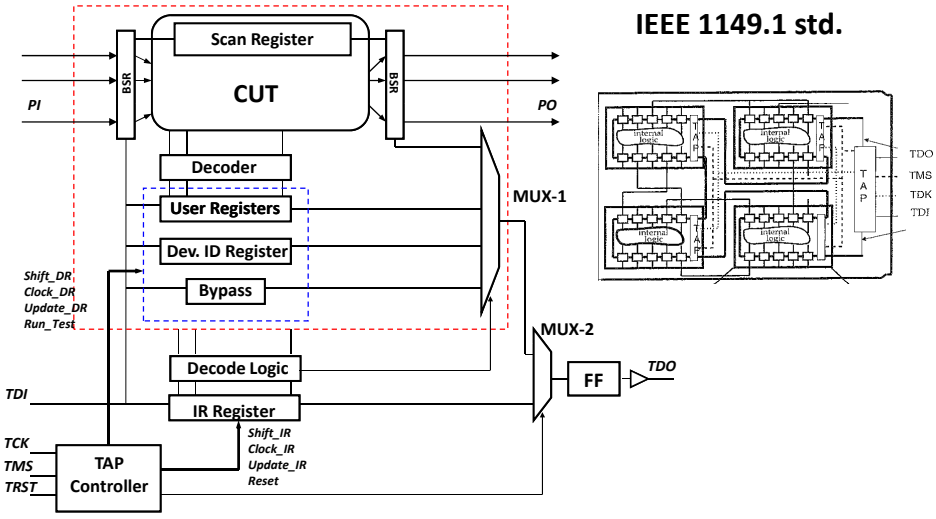
In built-in self testing, the test vectors are generated by an embedded circuit (*test vector/pattern generator*) under the control of the *BIST controller*. The circuit responses are compacted by the *response analyzer* and the final result (*signature*) after the completion of the testing procedure is compared with the expected result to make a decision. In case of discrepancy, the BIST controller provides a proper signal to indicate that the CUT is defective.

On-Line Testing



In on-line testing the circuit is under monitoring for error detection during its operation in the field. Many techniques exist to correct these errors (e.g. by a retry procedure) in order to provide *error tolerance* to the circuit under monitoring.

Testing Protocols



IEEE 1149.1 std.

The SoC Test Challenge