Device Reliability Report

Second Half 2018

UG116 (v10.10) March 22, 2019

XILINX

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/22/2019	10.10	Chapter 1, The Reliability Program Updated summary failure rates (Table 1-18) and soft error rates (Table 1-19 and Table 1-20) for 28 nm, 20 nm, and 16 nm process technologies. Chapter 2, Results by Product Family Updated tables with the latest test results. Chapter 3, Results by Package Type Updated tables with the latest test results. Added device type XCVU7P.
09/10/2018	10.9	Chapter 1, The Reliability Program Added devices for Spartan®-7 FPGAs to Table 1-15. Added a column for RF-ADC and RF-DAC HBM and CDM data to Table 1-17. Updated Table 1-18, Table 1-19, and Table 1-20. Chapter 2, Results by Product Family Updated tables with the latest test results. Added tables for *TH Test Results for Si Gate CMOS Device Types in the UltraScale Family* and the UltraScale+ family. Removed device types XC2Sxxx, XC3Sxxx, and XC3SDxxxA. Added Table 2-50, *HAST Test Results for Si Gate CMOS Device Type XC6Sxxx*. Removed the section *Unbiased High Accelerated Stress Test*. Chapter 3, Results by Package Type Updated tables with the latest test results. Added packages CPG196, SFV625, SFV784, FBV900, FBV484, FFG323, FFG324, FFG363, FFG1513, FFG1696, FFG1704, FFG1738, FFG1759, FFV901, FFV1136, FFV1148, FFV1152, FFV1153, FFV1154, FFV1156, FFV1156, FFV1157, and FFV1158. Removed packages CSG144, FFG900, FGG256, FGG320, FGG484, FGG400, FGG1156, FLV1517, FLV1924, FLV2104, HCG1932, PQG160, PQG208, PQG240, QFG32, and QFG48.
07/12/2018	10.8.2	Editorial updates only. No technical content updates.
05/03/2018	10.8.1	Chapter 2, Results by Product Family Corrected UltraScale and UltraScale+ device rows in Table 2-19.
03/22/2018	10.8	Chapter 1, The Reliability Program Added device XC7S50 to Table 1-15. Added PS-GTR transceivers to Table 1-17. Updated Table 1-18, Table 1-19, and Table 1-20. Chapter 2, Results by Product Family Updated tables with the latest test results. Chapter 3, Results by Package Type. Updated tables with the latest test results. HTS failures for device type XCVU9P in Table 3-56 changed to 0. Added test results for package FTG196 for device type XA7S50 (Table 3-57).
11/17/2017	10.7.1	Updated the SEU link above Table 1-19.

Date	Version	Revision
11/13/2017	10.7	Chapter 1, The Reliability Program Updated Table 1-7 and Table 1-18 for 0.016 µm devices. Added Table 1-17 for UltraScale+devices. Updated SEU and Soft Error Rate Measurements, Table 1-19, and Table 1-20. Chapter 2, Results by Product Family Updated tables for 0.016 µm devices. Updated Table 2-1 and Table 2-16. Added Table 2-18, Table 2-29, Table 2-46, and Table 2-63. Chapter 3, Results by Package Type. Adjusted Weibull plots for clarity and accuracy. Added device types (Table 3-31 and Table 3-56). FFV1927 was corrected to FFG1928. Updated FFG1928 characteristic life in Table 3-71.
07/11/2017	10.6.1	Made typographical changes.
07/10/2017	10.6	Chapter 1, The Reliability Program Updated ESD and LU test data. Added a definition of *obsolete*. Chapter 2, Results by Product Family Updated many tables and deleted tables for obsolete products. Added new tables for CMOS device types XC4Vxxx, XC5Vxxx, and XC6Vxxx, (Table 2-55 through Table 2-57). Added a note to Table 2-25. Chapter 3, Results by Package Type Updated many tables and deleted tables for obsolete products containing data more than 2 years old. Deleted data for non-hermetic packages BG352, BG432, and BG560 (device types XCV1000E, XCV1600E, and XCV300. Deleted data for package FB676 (device type XC7K410T). Deleted data for package SF363 (device type XC4VLX15). Deleted data for Pb-free packages BGG256 (device type XCS30XL), BGG352, BGG432, and BGG560 (device types XCV300E (Shrink), XCV600E (Shrink), and XCV1000E (Shrink)), CPG196 (device types XC6SLX4 and XC6SLX16), CPG236 (device type XC7A50T), FLG1155 (device type XC7V11580T), HCG1155 (device type XC7VH580T), and SFG363 (device type XC4VLX15). Added a note to Table 3-8 and Table 3-41.
04/04/2017	10.5.2	In Table 2-17, XCVU440 equivalent device hours were corrected to be 34,592.
12/19/2016	10.5.1	Updated the Figure 3-18 plot.

Date	Version	Revision
10/31/2016	10.5	Changed many tables to show test data for the first half of 2016. Added new product and package reliability data for XCVU440, XCVU190, XCVU125, XCVU095, and XCKU115 with respective packages of FFV1517, FFV1924, and FFV2104, FLV1517, FLV1924, and FLV2104, FLG2104, FLG2377, and FLG2892 (page 75). Removed the reliability data for these obsolete devices and packages: XCE06L24T, XC17SxxxA, XC17Vxxx, XCE0104, XC9572XL (PCG44 only), and PG120. Chapter 1, The Reliability Program Changed the title of Table 1-8 to ESD and Latch-up Data for PROMs, CPLDs, and Older FPGAs. Added devices to Table 1-16. Changed nomenclature for degrees Kelvin to K. Updated Table 1-18, Summary of the Failure Rates. Updated Table 1-19 and Table 1-20 data for the 28nm and 20nm nodes. (The former Table 1-18, Beam Testing and Real-Time Soft Error Rates, was divided into two tables: Experimental Beam Testing and Real-Time Soft Error Rates for CRAM and Experimental Beam Testing and Real-Time Soft Error Rates for BRAM.) Chapter 2, Results by Product Family Updated Table 2-1, Summary of HTOL Test Results and many tables. Updated CPLD Products. Chapter 3, Results by Package Type Updated tables for non-hermetic and hermetic packages. Added SFVA784 and SBVA784 to Board-Level Reliability Tests, Pb-Free BGA.
04/01/2016	10.4	Changed many tables to show test data for the second half of 2015. Chapter 1, The Reliability Program Updated Table 1-18 and Table 1-18. Chapter 2, Results by Product Family Updated most of the tables in this chapter. Added a footnote to Table 2-28: THB Test Results for Si Gate CMOS Device Type UltraScale FPGAs. Added Table 2-62: High-Temperature Storage Life Test Results for Si Gate CMOS Device Type UltraScale FPGAs. Chapter 3, Results by Package Type Updated Table 3-63: Summary of Test Results. Added FBVA900, FFVB2104, and FLVA1924 package types to Board-Level Reliability Tests, Pb-Free BGA, Table 3-64.
09/08/2015	10.3.1	Corrected two numbers in Table 1-18 20nm tech node row, FIT/Mb (Real-Time Soft Error Rate Per Event) column.
09/02/2015	10.3	Changed many tables to show test data for the first half of 2015. No devices were removed. The UltraScale™ FPGA KU040 device was added. Test results for new package FFVA1156 were added. FFV1927 package details were added to Board-Level Reliability Tests, Pb-Free BGA in Chapter 3.
03/09/2015	10.2.1	Corrected typo in Table 1-18 and Table 2-1 from 1.43,104 to 1,143,104.

Date	Version	Revision
02/11/2015	10.2	This report will now be issued biannually (twice a year). Changed many tables to show second quarter 2014 test data. Chapter 1, The Reliability Program Added UltraScale™ device data. Added Table 1-16: ESD and Latch-up Data for UltraScale Series. Chapter 2, Results by Product Family Added Table 2-27: THB Test Results for Si Gate CMOS Device Type XC2Vxxx. Deleted Table 2-29: THB Test Results for Si Gate CMOS Device Type XC2Sxxx. Deleted Table 2-39: TH Test Results for Si Gate CMOS Device Type XC3Sxxx. Deleted Table 2-40: TH Test Results for Si Gate CMOS Device Type XC3SxxxE. Deleted Table 2-41: TH Test Results for Si Gate CMOS Device Type XC3SxxxA. Deleted Table 2-42: TH Test Results for Si Gate CMOS Device Type XC3SDxxxA. Table 2-78: HASTU Test Results for Si Gate CMOS Device Type XC6Sxxx. Added Table 2-90: High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC6Sxxx. Table 2-91: High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC6Sxxx. Added Table 2-119: Summary of THB Test Results. Added Table 2-120: THB Test Results for Si Gate CMOS Device Type XC95xxxXL (replaced data for XC2Cxxx/A). Added Table 2-121: THB Test Results for Si Gate CMOS Device Type XC2Cxxx/A. Chapter 3, Results by Package Type Deleted package test results for PC44, PD8, and Table 3-29: Tests of Package Type DD8 (obsolete package). Added package test results for BGG256, FFVA1156, CPG236, FLG1155, FGG400, and added Figure 3-14: Cycles to Failure in the Second-Level Reliability Tests for FFG1928.
08/07/2014	10.1	Changed many tables to show second quarter 2014 test data. Chapter 1, The Reliability Program Updated Table 1-18 and Table 1-19. Updated SEU and Soft Error Rate Measurements, page 29. Chapter 2, Results by Product Family Data was updated in many tables. The Autoclave Test section was removed for CPLDs. HASTU has substituted Autoclave for the reliability monitor program. Chapter 3, Results by Package Type Added packages for PQ208, page 63 and FBG484, page 69.
05/02/2014	10.0	Changed many tables to show first quarter 2014 test data. Removed obsolete 0.22 µm Virtex® FPGA product data. Added package data for CLG400, FLG1926, FLG1928, and HCG1932. In Chapter 3, removed tables for packages CS280, CS484, FF1513, FF1517, PQ100, PQ160, PQ208, PQ240, CSG280, and PCG84. Added data for packages CLG400, FLG1926, FLG1928, and HCG1932. Added *Appendix A, Additional Resources and Legal Notices*.
03/18/2014	9.8	Replaced reliability data for package FFG1928, page 89. Added reliability data for package FLG1925, page 91. Revised the Revision History section for readability.

Date	Version	Revision
02/14/2014	9.7	Changed many tables to show fourth quarter, 2013 test data. Removed reliability data for the obsolete XCSxxxXL 0.25 µm device. Removed Spartan®-3 FPGA Autoclave data. HASTU has substituted Autoclave for the reliability monitor program. Chapter 1, The Reliability Program Updated Table 1-8 ESD and Latch-up Data for PROMs, CPLDs, and Older FPGAs, Table 1-15 ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 SoCs, Table 1-18 Summary of the Failure Rates, and Table 1-18 Beam Testing and Real-Time Soft Error Rates. Chapter 2, Results by Product Family Updated and moved existing tables. Updated test results in Temperature Cycling Test, page 42, High Accelerated Stress Test, and High Temperature Storage Life, page 47. Updated test results in Temperature Humidity with Bias Test, page 55, Unbiased High Accelerated Stress Test, page 65, and Data Retention Bake Test, page 57. Chapter 3, Results by Package Type Alphabetized Non-Hermetic packages SO20, VO20, VO48, PC44, PC84, PC20, PQ100, PQ160, PQ208, PQ240, TQ100, TQ144, VQ44, VQ100, HQ208, and HQ240. Removed package BGG256 from Reliability Data for Pb-Free Packages, page 67.
11/19/2013	9.6	Changed many tables to show third quarter, 2013 test data. Removed reliability data for the obsolete XC95xxx 0.5 µm device. Removed Spartan-3 FPGA Autoclave data. HASTU has substituted Autoclave for the reliability monitor program. Chapter 1, The Reliability Program Updated Table 1-7, Wafer Process Technology Family, Table 1-8, Product ESD and Latch-up Data, Table 1-15, ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 SoCs, Table 1-18, Summary of the Failure Rates, and Table 1-18, Real-Time Soft Error Rates. Added devices XC7V2000T, XC7VH580T, XC7VX1140T, and XC7Z100 to Table 1-15. Chapter 2, Results by Product Family Deleted the Autoclave Test section in Temperature Cycling Test, page 42. Chapter 3, Results by Package Type Added packages BG352, BG432, and BG560, page 66, FB676, page 68, FF484, page 60, FG320, page 62, FF900, page 60, BGG256, page 85, FBG900, page 70, FFG1513 and FFG1517, page 71, FFG1696, FFG1704, FFG1738, FFG1759, FFG1738 and FFG1760, page 72, FFV900 and FFV901, page 72, FLG1925, FLG1926, FLG1928, FLG1932, FLG2104, FLG2377, and FLG2892, page 75, and FSG48, page 75. Added FBG900, SBG484, FFG1928 and their plots to Board-Level Reliability Tests, Pb-Free BGA, page 84.

Date	Version	Revision
08/16/2013	9.5	Changed many tables to show second quarter, 2013 test data. Removed reliability data for the following obsolete devices: XC17(S)xxx/XL/E 0.6 µm XC4xxx/LE 0.5 µm XC4xxxE 0.5 µm XC4xxxXL 0.35 µm XCSxxx 0.35 µm XC4xxxXLA 0.25 µm XC95xxxXV 0.25 µm Chapter 1, The Reliability Program Updated Table 1-7, Wafer Process Technology Family, Table 1-8, Product ESD and Latch-up Data, Table 1-9, ESD and Latch-up Data for XC2VPxxx, Table 1-18, Summary of the Failure Rates, and Table 1-18, Real-Time Soft Error Rates. Added XC7VX980T to Table 1-15, ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 SoCs. Chapter 2, Results by Product Family Deleted tables for obsolete devices. Updated data in many tables. Added Table 2-23, THB Test Results for Si Gate CMOS Device Type XC3SxxxAN and Table 2-86, THB Test Results for Si Gate CMOS Device Type XC17SxxxA. Chapter 3, Results by Package Type Deleted these tables: Table 3-24, Tests of Package Type DD8 Table 3-25, Tests of Package Type Chip Scale CC44 Table 3-61, Test Results for Device Types XC7VX485T, XC7VX690T under heading FFG1927. Deleted PG132 and PG175 from Table 3-21, Tests of Package Type PG223. Deleted CB-100 and CB164 from and added CB196 to Table 3-22, Tests of Package Type CB228. Updated data in many tables. Added package CS484, page 73. Added packages FF1924, FF1926, FF1927, FF1928, FF1929, and FF1930, page 61. Added packages FFG1924, FFG1926, FFG1926, FFG1927, FFG1928, and FFG1930, page 72.

Date	Version	Revision
05/13/2013	9.4	Changed many tables to show first quarter, 2013 test data. Chapter 1, The Reliability Program Added 7 series devices XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T and Zynq-7000 SoC devices XC7Z010, XC7Z030, and XC7Z045 to Table 1-15, ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 SoCs. Updated data for 0.25 µm, 0.35 µm, and 0.5 µm process technologies in Table 1-18, Summary of the Failure Rates. Updated data for 40 nm, 45 nm, and 28 nm technology nodes in Table 1-18, Real-Time Soft Error Rates. Chapter 2, Results by Product Family Data in many tables was updated. Removed duplicate Table 2-17, HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XCE2Vxxx. Deleted Table 2-69, Temperature Cycling Test Results for Si Gate CMOS Device Type XC4xxxXLA. Added Table 2-67, Temperature Cycling Test Results for Si Gate CMOS Device Type XCE4VxXxxx. Chapter 3, Results by Package Type Data in many tables was updated. Added packages FFG1923, FFG1924, FFG1925, FFG1926, FFG1927, FFG1928, FFG1929, and FFG1930 and FFG1927 and their test results.
04/02/2013	9.3	Changed many tables to show fourth quarter, 2012 test data. Added Xilinx 7 series FPGAs and Zynq-7000 SoCs. Chapter 1, The Reliability Program Added XC7A100T, XC7A200T, XC7K70T, and XC7Z020 devices to Table 1-15 ESD and Latch-up Data for 7 Series FPGAs. Failure rate data changed in Table 1-16 Summary of the Failure Rates. Text and data changed in SEU and Soft Error Rate Measurements, page 29. Chapter 2, Results by Product Family Data in many tables was updated. Added Table 2-33 THB Test Results for Si Gate CMOS Device Type XCVxxx, Table 2-35 THB Test Results for Si Gate CMOS Device Type XC2Vxxx, Table 2-32 THB Test Results for Si Gate CMOS Device Type XC2SxxxE, Table 2-81 HAST Test Results for Si Gate CMOS Device Type XC4xxxE, and Table 2-104 HASTU Test Results for Si Gate CMOS Device Type XC4xxxXLA. Deleted Table 2-167, Summary of the Test Results for device XC2Cxxx/A from Temperature Humidity Test, page 68. Chapter 3, Results by Package Type Data in many tables was updated. Added packages CS144, CS324, CLG400 and CLG484, FBV676 and their respective test results in Table 3-9 Test Results for Device Types XCV50, XC2V80, Table 3-11 Test Results for Device Types XC6SLX45, XC6SLX45T, Table 3-29 Test Results for Device Types XC2V1000, XC2V1500, and Table 3-49 Test Results for Device Types XC5VLX50. Note: Table numbers are accurate as of the version 9.3 printing.

Date	Version	Revision
02/12/2013	9.2	Changed many tables to show the third quarter, 2012 test data. Added Xilinx 7 series FPGAs. Chapter 1, The Reliability Program Added XC7K160T, XC7K410T, XC7K420T, XC7K480T, XC7V585T, and XC7VX485T devices to Table 1-15, ESD and Latch-up Data for 7 Series FPGAs. Chapter 2, Results by Product Family Added Table 2-34, THB Test Results for Si Gate CMOS Device Type XCVxxxE, Table 2-95, HAST Test Results for Si Gate CMOS Device Type XCVxxxE, Table 2-103, HASTU Test Results for Si Gate CMOS Device Type XC4xxxE, Table 2-110, HASTU Test Results for Si Gate CMOS Device Type XCVxxxE, Table 2-111, HASTU Test Results for Si Gate CMOS Device Type XCVxxxE (Shrink), Table 2-120, HASTU Test Results for Si Gate CMOS Device Type XCE4VxXxxx, Table 2-125, High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC4xxxXLA, Table 2-126, High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XCSxxx, Table 2-141, High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XCE4VxXxxx, and Table 2-160, Autoclave Test Results for Si Gate CMOS Device Type XCFxxxS/P. Chapter 3, Results by Package Type Added packages FF665, FF672, FF676, FFG665, FFG672, and FFG896. Added Table 3-47, Test Results for Device Types XC5VLX30T and Table 3-56, Test Results for Device Type XC2V1000. Note: Table numbers are accurate as of the version 9.2 printing.

Date	Version	Revision
08/22/2012	9.1	Changed many tables to show the second quarter, 2012 test data. Chapter 1, The Reliability Program Added entries for devices XC6SLX4 and XC6SLX9. Removed obsolete reliability data for devices XC4VSX25, XC4VSX55, and XCV600E. Chapter 2, Results by Product Family Added entries for devices XC17S150A, XC3S250E, XC6VLX195T, XC7K410T, XC7VX485T, and XC9536. Removed obsolete reliability data for the following devices: XC17(S)xxx, XC17(S)xxx(X)L, XC17(S)xxxE, XC1702L, XC17S15A, XC17S200A, XC17S50XL, XC17Sxxx, XC17SxxxA, XC17SxxxXL, XC17Vxxx, XC18V01, XC18V02, XC18V04, XC18V512, XC18Vxxx, XC2C64, XC2S100E, XC2S150E, XC2V1500, XC2V3000, XC2VP100, XC2VP70, XC2VPxxx, XC2Vxxx, XC3S1000, XC3S100E, XC3S1400AN, XC3S200A, XC3SD1800A, XC3SDxxxA, XC3SxxxA, XC3SxxxAN, XC4013XLA, XC4VLX15, XC4VLX200, XC4VLX80, XC4VSX25, XC4VSX55, XC4xxxXLA, XC5VLX50T, XC6SLX150T, XC6SLX45, XC6SLX45T, XC6VLX130T, XC6VLX760, XC95144XL, XC95144XV, XC95288XV, XC95xxxXL, XC95xxxXV, XCF01S, XCF04S, XCF08P, XCF16P, XCF32P, XCFxxx, XCFxxxP, XCFxxxS, XCS20, XCS40XL, XCSxxx, XCSxxxXL, XCV1000E, XCV1600E, XCV400, XCV400E, XCV405E, XCV600E, XCV812E, XCVxxx (shrink), XCVxxxE, XCVxxxE (shrink) Chapter 3, Results by Package Type Added entries for devices XC7K410T and XC7VX485T. Removed obsolete reliability data for the following devices: XC17256E, XC17S100A, XC17S100XL, XC17S200A, XC17S50A, XC18V01, XC2C128, XC2C256, XC2S300E, XC2V1000, XC2V250, XC2V500, XC2V6000, XC2V80, XC2VP100, XC2VP50, XC2VP70, XC3S1500, XC3S4000, XC3S5000, XC4085XLA, XC4VLX100, XC4VLX25, XC5215, XC5VLX50, XC6SLX150T, XC6SLX16, XC6SLX45, XC6SLX45T, XC6VLX130T, XC6VLX240T, XC6VLX475T, XC6VLX760, XCE2VP50, XCF01S, XCF02S, XCF04S, XCF08P, XCF16P, XCF32P, XCR3064XL, XCS40XL, XCV1000E (shrink), XCV1600E, XCV2000E, XCV2000E (shrink), XCV300E (shrink), XCV600, XCV600E
05/08/2012	9.0	Changed many tables to show the first quarter, 2012 test data. Added Xilinx 7 series FPGAs.

Date	Version	Revision
01/27/2012	8.1	Updated Chapter 1, The Reliability Program Added XCE6VxXxxx to Table 1-7. Added XC5VSX240T to Table 1-12. Chapter 2, Results by Product Family Added XCE6VxXxxx to Table 2-1. Deleted XC2S150 from Table 2-8. Added XCV100 to Table 2-9. Added XC6SLX45 and XC6SLX100 to and deleted XC6SLX16 from Table 2-23. Added XC4VLX160 and XC4VFX12 and modified Note 1 in Table 2-24. Added Note 1 to Table 2-25 and Table 2-26. Inserted new table: Table 2-29. Added XC5VLX85T to table Table 2-45. Added XC6VLX365T to Table 2-46. Added XCS20XL to and deleted XCS10XL from Table 2-71. Added XC3S200AN to Table 2-84. Added XC6SLX4 to Table 2-85. Added XC2S100E to and deleted XC2S400E from Table 2-93. Added XCS20XL and XCSxxxX to Table 2-105. Added XC6SLX4 and XC6SLX9 to Table 2-117. Deleted XCR3064XL from Table 2-178. Added XC2C64 to Table 2-194. Added XCR3128XL to Table 2-214. Added XC2C64 to Table 2-215. Chapter 3, Results by Package Type Added HTS to Table 3-3 and Table 3-47. Added HAST to Table 3-56. Note: Table numbers are accurate as of the version 8.1 printing.
11/07/2011	8.0	Changed most tables to show the third quarter, 2011 test data. Chapter 1, The Reliability Program Updated Acceptance Criteria and added note 3 to Table 1-3. Chapter 2, Results by Product Family Added XCV600E to Table 2-12. Added XC2VP7 to and deleted XC2VP80 from Table 2-15. Deleted XC3S2000 from Table 2-18. Deleted XC4VLX15 from Table 2-24. Added XC6VLX130T to Table 2-28. Added XC4VLX80 to Table 2-43. Added XC2V6000 to Table 2-77. Deleted XC4VFX100 and XC4VLX85T from Table 2-85. Added XC5VLX330T device to Table 2-86. Added XC6VLX195T device to Table 2-87. Added XC6SLX25T to Table 2-99. Added XCV100 to Table 2-123. Added XC6SLX16 to Table 2-136. Added XC4VLX80 to Table 2-137. Deleted XC17S150XL from Table 2-146. Deleted XCF128X from Table 2-148. Deleted XC17S30XL from Table 2-152. Deleted XCF01S, XCF04S, XCF08P, and XCF128X from Table 2-155. Deleted XC17S30XL from Table 2-163. Deleted XC17V16 from Table 2-164. Deleted XC17S30XL from Table 2-169. Deleted XC17V16 from Table 2-170. Deleted XCF01S, XCF04S, XCF08P, and XCF128X from Table 2-172. Deleted XC95216 from Table 2-174. Added XCR3256XL and deleted XCR384XL and XCR3512XL from Table 2-192. Added XCR3256XL and deleted XCR384XL and XCR3512XL from Table 2-201. Added XCR3256XL and deleted XCR3128XL XCR3512XL from Table 2-213. Chapter 3, Results by Package Type Added HASTU to Table 3-11. Deleted HTS from Table 3-12. Deleted HASTU from Table 3-15. Deleted Temperature cycling –40 to +125°C row from Table 3-26. Added HASTU to Table 3-29. Added HTS to Table 3-43. Added HAST to Table 3-47. Added Temperature cycling -55 to +125°C row and HTS to Table 3-49. Added HTS to Table 3-66. Added Temperature humidity 85°C, 85% RH with bias row to Table 3-74. Note: Table numbers are accurate as of the version 8.0 printing.
08/02/2011	7.0	Changed most tables to show the **second** quarter, 2011 test data.
06/17/2011	6.0.1	Revised last sentence in SEU and Soft Error Rate Measurements, page 29 for clarity.

Date	Version	Revision
05/09/2011	6.0	Changed most tables to show the first quarter, 2011 test data.
02/01/2011	5.12	Changed most tables to show the fourth quarter, 2010 test data.
11/01/2010	5.11	Changed most tables to show the third quarter, 2010 test data.
08/10/2010	5.10	Changed most tables to show the second quarter, 2010 test data.
05/04/2010	5.9	Changed most tables to show the first quarter, 2010 test data.
03/15/2010	5.8	Changed most tables to show the fourth quarter, 2009 test data.
10/27/2009	5.7	Updated most tables to include third quarter, 2009 test data. Added alpha particle FIT/Mb data for Spartan®-6 and Virtex®-6 FPGAs to Table 1-14, page 19. Note: Table number is accurate as of the version 5.7 printing.
08/03/2009	5.6	Changed most tables to show the second quarter, 2009 test data.
06/15/2009	5.5	Added SF363 (Lot 2) data to Table 3-62, page 102. Replaced Figure 3-1, page 103, Figure 3-2, page 103, and Figure 3-3, page 104. Revised FFG1704 data in Table 3-64, page 108. Note: Table and Figure numbers are accurate as of the version 5.5 printing.
05/07/2009	5.4	Changed most tables to show the first quarter, 2009 test data. Added second paragraph to SEU and Soft Error Rate Measurements, page 29.
02/11/2009	5.3	Changed most tables to show the fourth quarter test data. Added single event upset and soft error rate data. See Table 1-14, page 19. Note: Table number is accurate as of the version 5.3 printing.
11/14/2008	5.2	Changed most tables to show the third quarter test data. Updated legal disclaimer.
08/15/2008	5.1	Changed most tables to show the second quarter test data.
07/07/2008	5.0	Changed most tables to show the first quarter test data.
02/06/2008	4.3	Changed most tables to show the fourth quarter test data.
10/31/2007	4.2	Changed most tables to show the third quarter test data.
09/18/2007	4.1.1	Corrected omission in this history table.
08/24/2007	4.1	Changed most tables to show the second quarter test data.
06/04/2007	4.0	Changed most tables to show the first quarter test data.
03/28/2007	3.3.2	Corrected typos in four tables.
02/20/2007	3.3.1	Corrected typos in three tables.
02/12/2007	3.3	Changed most tables to show the fourth quarter test data.
12/01/2006	3.2	Changed most tables to show the third quarter test data.
10/06/2006	3.1.2	Corrected values in tables 1-12, 2-87, 2-90, and 2-91.
08/29/2006	3.1.1	Changed typos in tables 2-91, 3-44, and 3-55.
08/11/2006	3.1	Changed most tables to show the second quarter test data.
06/20/2006	3.0.1	Corrected two transposed figures in Table 1-10.
05/05/2006	3.0	Changed most tables to show the first quarter test data.

Date	Version	Revision
02/24/2006	2.9	Updated most tables to reflect the fourth quarter test data.
11/17/2005	2.8	Updated most tables to include the third quarter test data.
08/19/2005	2.7	Changed most tables to show the second quarter test values.
05/20/2005	2.6	Corrected data in tables 2-61 and 3-32.
03/01/2005	2.5	Changed most tables to show the fourth quarter test values. Removed packaging information from Chapter 1 and added a reference to the packaging website.
01/04/2005	2.4	Added third quarter data.
08/18/2004	2.3	Added second quarter data.
05/24/2004	2.2	Changed Tables 1-1, 2-1, 2-15, 3-44, 3-46, 3-48, 3-50, 3-52 and a heading on page 75.
05/24/2004	2.1	Changed FIT rate on page 7 for 0.5 µm from 89 to 8.
05/10/2004	2.0	First quarter 2004 revision.
02/09/2004	1.0	Initial release in new template.

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Chapter 1

The Reliability Program

Overview

Xilinx publishes this report to provide customers with insight regarding the reliability of Xilinx® products. Reliability is defined as product performance to specification over time in response to varied (specified) environmental stress conditions. The goal of the reliability program is to achieve continuous improvement in the robustness of each product being evaluated.

As part of this program, finished product reliability is measured periodically to ensure that the product performance meets or exceeds reliability specifications. Reliability programs are executed in response to internal programs.

The reliability qualifications of new devices, wafer processes, and packages are designed to ensure that Xilinx products satisfy internal requirements before transfer into production. The reliability qualification and monitoring requirements are outlined in Table 1-1 through Table 1-18. The reliability stress tests are conducted according to the conditions specified in JEDEC Solid State Technology Association' s reliability test methods for packaged devices, JESD22, except Group B and D tests in which it follows DSCC test methods, MIL-STD-883.

Note: In this report, *obsolete* refers to Xilinx products for which a Product Discontinuation Notice (PDN) has been issued to cease the shipment and to data more than two years old that is no longer valid due to a process change.

Product Qualification

The reliability tests used for wafer process qualification are summarized in Table 1-1.

Table 1-1: **Wafer Process Qualification Tests**

Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
High-temperature operating life (HTOL)	$T_J \geq 125°C$, V_{DD} Max	1,000 hours	3	77	200 FIT(1) 50 FIT(2)
THB(3) or High-accelerated stress test (HAST)(3)	85°C, 85% RH, VDD	1,000 hours	3	25	0 failures
	130°C, 85% RH, V_{DD}	96 hours			
	110°C, 85% RH, V_{DD}	264 hours			
Temperature humidity (TH)(3) or Unbiased high accelerated stress test (HASTU)(3)	85°C, 85% RH	1,000 hours	3	25	0 failures
	130°C, 85% RH	96 hours			
	110°C, 85% RH	264 hours			
Temperature cycling (TC)(3)(4)(5)(6)	–65°C to +150°C	500 cycles	3	25	0 failures
	–55°C to+125°C	1,000 cycles			
	–40°C to +125°C	1,000 cycles			
Data Retention Bake(7) or High Temperature Storage (HTS)	$T_A = 150°C$	1,000 hours	3	25	0 failures
Program Erase(8)	$T_A = 25°C$	10,000 cycles	1	32	0 failures

Notes:

1. FIT is *failure in time*. Phase I production is released as the qualification data demonstrates, meeting the required 200 FIT failure rate and other test requirements.
2. Phase II production is released as the qualification data demonstrates, meeting the required 50 FIT failure rate and other test requirements.
3. Package preconditioning is performed prior to THB, HAST, temperature cycling, TH, and HASTU tests.
4. For plastic QFP packages: –65°C to +150°C and 500 cycles or –55°C to +125°C and 1,000 cycles.
5. For plastic BGA packages: –55°C to +125°C and 1,000 cycles.
6. For flip chip packages: –55°C to +125°C and 1,000 cycles or –40°C to +125°C and 1,000 cycles.
7. For CPLD and EPROM products.
8. This is not a mandatory test and only for CPLD and EPROM products.

Non-Hermetic and Hermetic Packages

Moisture sensitivity and reflow temperature information can be found in *Device Package User Guide* (UG112) [Ref 1].

The non-hermetic package/assembly qualification is outlined in Table 1-2. However, for hermetic package qualification, a full group B and D test per MIL-STD-833, *Test Methods*, is required.

Table 1-2: **Non-Hermetic Package/Assembly Qualification**

Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
THB(1) or HAST(1)	85°C, 85% RH, V_{DD}	1,000 hours	3	25	0 failures
	130°C, 85% RH, V_{DD}	96 hours			
	110°C, 85% RH, V_{DD}	264 hours			
Temperature cycling(1) (2) (3) (4)	–65°C to +150°C	500 cycles	3	25	0 failures
	–55°C to +125°C	1,000 cycles			
	–40°C to +125°C	1,000 cycles			
Autoclave(1) or temperature humidity unbiased(1) or HASTU(1)	121°C, 100% RH	96 hours	3	25	0 failures
	85°C, 85% RH	1,000 hours			
	130°C, 85% RH or 110°C, 85% RH	96 hours or 264 hours			
High-Temperature Storage (HTS)	T_A=150°C	1,000 hours	3	25	0 failures

Notes:

1. Package preconditioning is performed prior to THB, HAST, temperature cycling, autoclave, TH, and HASTU tests.
2. For plastic BGA packages: –55°C to +125°C and 1,000 cycles.
3. For flip chip packages: –55°C to +125°C and 1,000 cycles or –40°C to +125°C and 1,000 cycles.
4. For plastic QFP packages: –65°C to +150°C and 500 cycles or –55°C to +125°C and 1,000 cycles.

The qualification process for new devices is shown in Table 1-3.

Table 1-3: **Device Qualification**

Reliability Test	Conditions	Lot Quantity	Sample Size per Lot	Target Criteria
ESD	HBM(1)	1	3	1,000V
ESD	CDM(2)	1	3	250V(3)
Latch-up	Current injection	1	3	±100 mA

Notes:

1. HBM = Human Body Model.
2. CDM = Charge Device Model.
3. GT transceiver CDM level is specified per JEP157.

Reliability Monitor Program

The wafer process reliability monitor program is based on the maturity of the wafer process, the number of device hours, and the failure in time (FIT) rate. All processes are divided into one of two classes to determine how often the process is monitored annually. Class 1 processes are monitored every quarter; Class 2 processes are monitored every other quarter. FIT Rate calculations for both classes are based on approximately one million device hours (at T_J = 125°C) per fab if the data is available. Processes that are four years old or less are monitored every quarter regardless of the FIT rate. Mature processes older than four years are monitored based on the FIT Rate. Table 1-4 summarizes the classification criteria and monitoring frequency for both classes.

Table 1-4: **Monitoring Process Classes**

	Class 1	Class 2
Classification Criteria	Process Age ≤ 4 years or FIT > 26 (for FPGAs), 55 (for Flash PROM)	Process Age > 4 years and FIT < 26 (for FPGAs), 55 for Flash PROMs)
Monitor Frequency	4 times per year	2 times per year

The reliability tests used to monitor the wafer process are shown in Table 1-5.

Table 1-5: **Tests Used to Monitor Wafer Processes**

Reliability Test	Condition	Duration	Lot Quantity	Sample Size per Process per Family per Quarter
HTOL	T_j > 125°C, V_{DD} Max	1,000 hours	1	45
Data Retention Bake(1)	T_A = 150°C	1,000 hours	1	45

Notes:
1. For CPLD and PROM products.

The package reliability monitor program takes into consideration the following factors:

- Package construction (wire-bond lead frame, wire-bond BGA, or flip chip)
- Factory location (assembly site, or wafer fabrication site)
- Substrate vendor
- Die size
- Technology maturity
- Past history

Based on these factors and availability, representative packages are drawn from inventory for the stress tests defined in Table 1-6. These tests are typically conducted on a quarterly basis, but the number of tests can be reduced or eliminated based on the maturity of the package technology, understanding of failure mechanisms, and their dependency on the stress test.

Table 1-6: **Tests Used by the Reliability Package Monitor Program**

Reliability Test	Stress Conditions	Stress Duration	Sample Size	Frequency
THB(1) or HAST(1)	85°C, 85% RH, V_{DD}	1,000 hrs	45	WBLF(2) every even quarter WBBGA(3) every odd quarter Flip Chip (4) every quarter
	130°C, 85% RH, V_{DD}	96 hrs		
	110°C, 85% RH, V_{DD}	264 hrs		
Temperature cycling(1)(5)	–55°C to +125°C or –40°C to +125°C	1,000 cycles	45	WBLF every quarter WBBGA every quarter Flip Chip every quarter
Autoclave(1)(6) or Temperature humidity unbiased(1)(6) or HASTU(1)(6)	121°C, 100% RH	96 hrs	45	WBLF every odd quarter WBBGA every even quarter
	85°C, 85% RH	1,000 hrs		
	130°C, 85% RH or 110°C, 85% RH	96 hrs or 264 hrs		
HTS(7)	T_A=150°C	1,000 hrs	45	WBLF every quarter WBBGA every quarter

Notes:

1. Package preconditioning is performed prior to THB, HAST, temperature cycling, autoclave, TH, and HASTU tests.
2. For matured WBLF packages (PLCCs, SOICs, and DIPs packages), reliability monitoring is performed once a year.
3. For matured WBBGA packages (S-BGA Cavity-down BGA), reliability monitoring is performed once a year.
4. For flip chip packages, THB testing is performed every quarter and replaces the need for temperature humidity testing.
5. For plastic QFP and BGA packages: –55°C to +125°C and 1,000 cycles; for flip chip packages: –55°C to +125°C and 1,000 cycles or 40°C/+125°C and 1,000 cycles.
6. Refer to the device-specific qualification report for complete autoclave, temperature humidity, and HASTU reliability test data.
7. HTS stress is not applicable with flip chip package because the technology has no wire-bond IMC interface degradation.

Process Technology Family

Table 1-7 lists the Xilinx devices that support various process technologies.

Table 1-7: **Wafer Process Technology Family**

Process Technology	Device
16 nm	UltraScale+™ devices
20 nm	UltraScale™ devices
28 nm	7 series FPGAs and Zynq®-7000 SoCs
40 nm	XC6VxXxxx
45 nm	XC6Sxxx
65 nm	XC5VxXxxx, XCE5VxXxxx
90 nm	XC3Sxxx, XC3SxxxA, XC3SxxxAN, XC3SxxxE,XC3SDxxxA, XC4VxXxxx, XCE4VxXxxx
130 nm	XC2VPxxx, XCE2VPxxx
150 nm	XC18Vxxx, XCFxxxS/P
180 nm	XC2Cxxx
220 nm/180 nm	XC2Sxxx
350 nm/250 nm	XC95xxxXL
350 nm	XCRxxxXL

ESD and Latch-up Summary

ESD results are obtained according to specifications ANSI/ESDA/JEDEC JS-001-2010 and JEDEC JESD22-C101. Latch-up results are obtained by using specification EIA/JESD78. ESD tests are performed at 25°C. In general, the latch-up data for newer products such as Zynq-7000 SoCs, 7 series, Virtex®-4, Virtex®-5, Virtex®-6, Spartan®-3, and Spartan®-6 devices are collected at 125°C unless specified otherwise.

ESD and latch-up data are summarized by family in these tables:

- Table 1-8: PROMs, CPLDs, and older FPGAs
- Table 1-9: Virtex-II Pro devices
- Table 1-10 and Table 1-11: Virtex-4 devices
- Table 1-12: Virtex-5 devices
- Table 1-13: Spartan-6 devices
- Table 1-14: Virtex-6 devices

- Table 1-15: 7 series FPGAs and Zynq-7000 SoCs
- Table 1-16: UltraScale devices
- Table 1-17: UltraScale+ devices

Table 1-8: **ESD and Latch-up Data for PROMs, CPLDs, and Older FPGAs**

Device	Latch-up	Human Body Model	Charge Device Model
XC18Vxxx/XCFxx	+200 mA	+2,000V	+500V(1)
XCVxxxE	+210 mA	+1,000V to +2,500V(4)	+300V(3)
XC2Sxxx	+210 mA	+2,000V	+500V(4)
XC95xxxXL	+200 mA	+2,000V to +3,000V	+1,000V(5)
XCRxxxL	+200 mA	+2,000V to +3,000V	+500V(6)
XC2Cxxx	+200 mA	+2,000V	+500V
XC3Sxxx	+200 mA	+2,000V	+500V
XC3SxxxE	+200 mA	+2,000V	+500V
XC3SxxxA	+200 mA	+2,000V	+500V

Notes:

1. Measured on XC18V04 and XCF32P
2. Only XCV100E and XCV812E have ESD threshold below 2KV, (XCV100E passed at 1.5KV and XCV812E passed at 1KV)
3. Measured on XCV50E
4. Measured on XC2S200
5. Measured on XC9536XL
6. Measured on XCR3064XL

The ESD results in Table 1-9 do not include DXN and DXP temperature sensing pins.

Table 1-9: **ESD and Latch-up Data for XC2VPxxx**

Device	Latch-up ±200 mA	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		Regular I/O and Power	MGT	Regular I/O and Power	MGT
XC2VP2	Pass	±1,500V	±2,000V	±500V	±300V
XC2VP4	Pass	±2,000V	±1,500V	±500V	±300V
XC2VP7	Pass	±2,000V	±1,000V	±500V	±500V
XC2VP20	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP30	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP40	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP50	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP70	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP100	Pass	±2,000V	±1,000V	±500V	±300V

Table 1-10: **ESD and Latch-up Data for XC4VFXxxx**

Device	Latch-up	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		STDIO	MGT	STDIO	MGT
XC4VFX12	Pass	±2,000V	N/A	±450V	N/A
XC4VFX60	Pass	±2,000V	±1,000V	±500V	±300V
XC4VFX40	Pass	±2,000V	±1,000V	±500V	±300V
XC4VFX20	Pass	±2,000V	±1,000V	±500V	±300V
XC4VFX100	Pass	±2,000V	±1,000V	±450V	±300V
XC4VFX140	Pass	±2,000V	±1,000V	±500V	±300V

Table 1-11: **ESD and Latch-up Data for XC4VLXxxx and XC4VSXxxx**

Device	Latch-up	Human Body Model Passing Voltage	Charge Device Mode Passing Voltage
XC4VLX15	Pass	±2,000V	±500V
XC4VLX25	Pass	±2,000V	±450V
XC4VLX40	Pass	±2,000V	±450V
XC4VLX60	Pass	±2,000V	±400V
XC4VLX80	Pass	±2,000V	±450V
XC4VLX100	Pass	±2,000V	±350V
XC4VLX160	Pass	±2,000V	±450V
XC4VLX200	Pass	±2,000V	±350V
XC4VSX25	Pass	±2,000V	±500V
XC4VSX35	Pass	±2,000V	±450V
XC4VSX55	Pass	±2,000V	±400V

Table 1-12: **ESD and Latch-up Data for XC5VxXxxx/T**

Device	Latch-up	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		SelectIO(1)	GTP	SelectIO	GTP
XC5VLX20T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VLX30	Pass	±2,000V	N/A	±400V	N/A
XC5VLX30T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VLX50	Pass	±2,000V	N/A	±400V	N/A
XC5VLX50T	Pass	±2,000V	±1,000V	±400V	±250V(2)
XC5VLX85	Pass	±2,000V	N/A	±400V	N/A
XC5VLX85T	Pass	±2,000V	±1,000V	±400V	±250V(2)

Table 1-12: **ESD and Latch-up Data for XC5VxXxxx/T *(Cont'd)***

Device	Latch-up	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		SelectIO[1]	GTP	SelectIO	GTP
XC5VLX110	Pass	±2,000V	N/A	±400V[3]	N/A
XC5VLX110T	Pass	±2,000V	±1,000V	±400V[3]	±250V[2]
XC5VLX155	Pass	±2,000V	N/A	±400V	N/A
XC5VLX155T	Pass	±2,000V	±1,000V	±400V	±250V[4]
XC5VLX220	Pass[5]	±2,000V	N/A	±400V	N/A
XC5VLX220T	Pass[5]	±2,000V	±1,000V	±400V	±250V[4]
XC5VLX330	Pass[6]	±2,000V	N/A	±400V	N/A
XC5VLX330T	Pass[6]	±2,000V	±1,000V	±400V	±250V[2]
XC5VFX30T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VFX70T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VFX100T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VFX130T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VFX200T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VSX35T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VSX50T	Pass	±2,000V	±1,000V	±400V	±250V[2]
XC5VSX95T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VSX240T	Pass	±2,000V	±1,000V	±400V	±250V[2]
XC5VTX150T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VTX240T	Pass	±2,000V	±1,000V	±400V	±250V

Notes:

1. Human body model passing voltage for VBATT pin is 1,000V. This data is updated based on the data collected after the HBM tester was upgraded to remove the HBM-ESD trailing pulse.
2. If an internal AC coupling capacitor is used in the GTP receiver input (RX) pin, charge device model passing voltage is 200V. Compliance to ANSI/ESD S20.20 (ESD Association standard for the electrostatic discharge control program) is necessary.
3. Charge device model passing voltage for VBATT pin is 300V.
4. If an internal AC coupling capacitor is used in the GTP receiver input (RX) pin, the CDM level is 150V. Compliance to ANSI/ESD S20.20 (ESD Association standard for the electrostatic discharge control program) is necessary.
5. The D_IN and CS_B pins on XC5VLX220 and XC5VLX220T devices pass at 150 mA.
6. The D_IN, CS_B, and RDWR_B pins on XC5VLX300 and XC5VLX330T devices pass at 150 mA.

Table 1-13: **ESD and Latch-up Data for XC6Sxxx**

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO	GTP	SelectIO	GTP
XC6SLX4	Pass	±2,000V	N/A	±500V	N/A
XC6SLX9	Pass	±2,000V	N/A	±500V	N/A
XC6SLX16	Pass	±2,000V	N/A	±500V	N/A
XC6SLX25	Pass	±2,000V	N/A	±500V	N/A
XC6SLX25T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX45	Pass	±2,000V	N/A	±500V	N/A
XC6SLX45T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX75	Pass	±2,000V	N/A	±500V	N/A
XC6SLX75T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX100	Pass	±2,000V	N/A	±500V	N/A
XC6SLX100T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX150	Pass	±2,000V	N/A	±500V	N/A
XC6SLX150T	Pass	±2,000V	±2,000V	±500V	±450V

Table 1-14: **ESD and Latch-up Data for XC6VxXxxx**

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC6VLX75T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX130T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX195T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX240T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX365T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX550T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX760	Pass	±2,000V(1)	N/A	±500V(2)	N/A
XC6VSX315T	Pass	±2,000V(1)	±1,000V	±500V(2)	±200V
XC6VSX475T	Pass	±2,000V(1)	±1,000V	±500V(2)(3)	±250V
XC6VHX250T	Pass	±2,000V(1)	±1,000V	±500V(2)(3)	±250V
XC6VHX255T	Pass	±2,000V(1)	±1,000V	±500V(2)(3)	±250V
XC6VHX380T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V

Table 1-14: **ESD and Latch-up Data for XC6VxXxxx *(Cont'd)***

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC6VHX565T	Pass	±2,000V(1)	±1,000V	±500V(2)(3)	±250V

Notes:

1. If the system monitor function is used, HBM passing voltage is: ±1,000V for all of the devices.
2. If the system monitor function is used, CDM passing voltage for the AVDD, AVSS, VN, VP, VREFN, VREFP, DXN and DXP pins is: ±200V for XC6VLX130T, XC6VLX195T, XC6VLX240T, XC6VSX315T, XC6VHX250T, XC6VHX255T, and XC6VHX565T devices; ±150V for XC6VLX75T, XC6VLX365T, XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX380Tdevices. The DXN and DXP pins can withstand CDM voltages up to 500V without impacting the temperature sensing function.
3. The CDM passing voltage for the CCLK pin of the XC6VSX475T, XC6VHX250T, XC6VHX255T, and XC6VHX565T devices is 450V.

Table 1-15: **ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 SoCs**

Device	Latch-Up	HBM Passing Voltage(1)		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC7A12T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A15T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A25T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A35T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A50T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A75T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A100T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A200T	Pass	±1,000V	±1,000V	±350V	±250V
XC7S6	Pass	±1,000V(2)	N/A	±350V	N/A
XC7S15	Pass	±1,000V(2)	N/A	±350V	N/A
XC7S25	Pass	±1,000V	N/A	±350V	N/A
XC7S50	Pass	±1,000V	N/A	±350V	N/A
XC7S75	Pass	±1,000V	N/A	±350V	N/A
XC7S100	Pass	±1,000V	N/A	±350V	N/A
XC7K70T	Pass	±1,000V	±1,000V	±350V	±300V
XC7K160T	Pass	±1,000V	±1,000V	±350V	±300V
XC7K325T	Pass	±1,000V	±1,000V	±350V	±300V
XC7K355T	Pass	±1,000V	±1,000V	±350V	±300V
XC7K410T	Pass	±1,000V	±1,000V	±350V	±300V

Table 1-15: **ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 SoCs *(Cont'd)***

Device	Latch-Up	HBM Passing Voltage[1]		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC7K420T	Pass	±1,000V	±1,000V	±350V	±300V
XC7K480T	Pass	±1,000V	±1,000V	±350V	±300V
XC7V585T	Pass	±1,000V	±1,000V	±350V	±250V
XC7V2000T	Pass	±1,000V	±1,000V	±350V	±250V
XC7VH580T	Pass	±1,000V	±1,000V	±350V	±200V
XC7VH870T	Pass	±1,000V	±1,000V	±350V	±200V
XC7VX330T	Pass	±1,000V	±1,000V	±350V	±250V
XC7VX415T	Pass	±1,000V	±1,000V	±350V	±250V
XC7VX485T	Pass	±1,000V	±1,000V	±350V	±250V
XC7VX550T	Pass	±1,000V	±1,000V	±350V	±200V
XC7VX690T	Pass	±1,000V	±1,000V	±350V	±200V
XC7VX980T	Pass	±1,000V	±1,000V	±350V	±200V
XC7VX1140T	Pass	±1,000V	±1,000V	±350V	±200V
XC7Z007S	Pass	±1,000V	N/A	±350V	N/A
XC7Z010	Pass	±1,000V	N/A	±350V	N/A
XC7Z012S	Pass	±1,000V	±1,000V	±350V	±300V
XC7Z014S	Pass	±1,000V	N/A	±350V	N/A
XC7Z015	Pass	±1,000V	±1,000V	±350V	±300V
XC7Z020	Pass	±1,000V	N/A	±350V	N/A
XC7Z030	Pass	±1,000V	±1,000V	±350V	±300V
XC7Z035	Pass	±1,000V	±1,000V	±350V	±300V
XC7Z045	Pass	±1,000V	±1,000V	±350V	±300V
XC7Z100	Pass	±1,000V	±1,000V	±350V	±300V

Notes:

1. HBM passing voltage levels have been revised based on latest calibration data.
2. All pins pass ±1000V except for HR I/O pins which pass ±900V.

Table 1-16: **ESD and Latch-up Data for UltraScale Devices**

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage		
		SelectIO and Special Functions	Transceivers	SelectIO and Special Functions	Transceivers	
					GTH	GTY
XCKU025	Pass	±1,250V	±1,250V	±250V	±200V	N/A
XCKU035	Pass	±1,250V	±1,250V	±250V	±200V	N/A

Table 1-16: **ESD and Latch-up Data for UltraScale Devices *(Cont'd)***

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage		
		SelectIO and Special Functions	Transceivers	SelectIO and Special Functions	Transceivers	
					GTH	GTY
XCKU040	Pass	±1,250V	±1,250V	±250V	±200V	N/A
XCKU060	Pass	±1,250V	±1,250V	±250V	±200V	N/A
XCKU085	Pass	±1,250V	±1,250V	±250V	±150V	N/A
XCKU095	Pass	±1,250V	±1,250V	±250V	±200V	±150V
XCKU115	Pass	±1,250V	±1,250V	±250V	±150V	N/A
XCVU065	Pass	±1,250V	±1,250V	±250V	±200V	±150V
XCVU080	Pass	±1,250V	±1,250V	±250V	±200V	±150V
XCVU095	Pass	±1,250V	±1,250V	±250V	±200V	±150V
XCVU125	Pass	±1,250V	±1,250V	±250V	±200V	±150V
XCVU160	Pass	±1,000V	±1,000V	±250V	±200V	±150V
XCVU190	Pass	±1,000V	±1,000V	±250V	±200V	±150V
XCVU440	Pass	±1,250V	±1,250V	±250V	±200V	N/A

Table 1-17: **ESD and Latch-up Data for UltraScale+ Devices**

Device	Latch-Up	HBM Passing Voltage Levels					CDM Passing Voltage Levels				
		FPGA Logic and SelectIO Interface	Transceivers				FPGA Logic and SelectIO Interface	Transceivers			
			PS-GTR	GTH	GTY	RF-ADC RF-DAC		PS-GTR	GTH	GTY	RF-ADC RF-DAC
KU3P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	±150V	N/A	N/A	±150V	N/A
KU5P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	±150V	N/A	N/A	±150V	N/A
KU9P	Pass	±1,500V	N/A	±1,500V	N/A	N/A	±150V	N/A	±150V	N/A	N/A
KU11P	Pass	±1,500V	N/A	±1,500V	±1,500V	N/A	±150V	N/A	±150V	±150V	N/A
KU13P	Pass	±1,500V	N/A	±1,500V	N/A	N/A	±150V	N/A	±150V	N/A	N/A
KU15P	Pass	±1,500V	N/A	±1,500V	±1,500V	N/A	±150V	N/A	±150V	±150V	N/A
VU3P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	±150V	N/A	N/A	±150V	N/A
VU5P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	±150V	N/A	N/A	±150V	N/A
VU7P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	±150V	N/A	N/A	±150V	N/A
VU9P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	±150V	N/A	N/A	±150V	N/A
VU11P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	±150V	N/A	N/A	±150V	N/A
VU13P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	±150V	N/A	N/A	±150V	N/A
ZU2	Pass	±1,500V	±1,500V	N/A	N/A	N/A	±150V	±150V	N/A	N/A	N/A
ZU3	Pass	±1,500V	±1,500V	N/A	N/A	N/A	±150V	±150V	N/A	N/A	N/A
ZU4	Pass	±1,500V	±1,500V	±1,500V	N/A	N/A	±150V	±150V	±150V	N/A	N/A

Table 1-17: **ESD and Latch-up Data for UltraScale+ Devices *(Cont'd)***

Device	Latch-Up	HBM Passing Voltage Levels					CDM Passing Voltage Levels				
		FPGA Logic and SelectIO Interface	Transceivers				FPGA Logic and SelectIO Interface	Transceivers			
			PS-GTR	GTH	GTY	RF-ADC RF-DAC		PS-GTR	GTH	GTY	RF-ADC RF-DAC
ZU5	Pass	±1,500V	±1,500V	±1,500V	N/A	N/A	±150V	±150V	±150V	N/A	N/A
ZU6	Pass	±1,500V	±1,500V	±1,500V	N/A	N/A	±150V	±150V	±150V	N/A	N/A
ZU7	Pass	±1,500V	±1,500V	±1,500V	N/A	N/A	±150V	±150V	±150V	N/A	N/A
ZU9	Pass	±1,500V	±1,500V	±1,500V	N/A	N/A	±150V	±150V	±150V	N/A	N/A
ZU11	Pass	±1,500V	±1,500V	±1,500V	±1,500V	N/A	±150V	±150V	±150V	±150V	N/A
ZU15	Pass	±1,500V	±1,500V	±1,500V	N/A	N/A	±150V	±150V	±150V	N/A	N/A
ZU17	Pass	±1,500V	±1,500V	±1,500V	±1,500V	N/A	±150V	±150V	±150V	±150V	N/A
ZU19	Pass	±1,500V	±1,500V	±1,500V	±1,500V	N/A	±150V	±150V	±150V	±150V	N/A
ZU21DR	Pass	±1,500V	±1,500V	N/A	±1,500V	N/A	±150V	±150V	N/A	±150V	N/A
ZU25DR	Pass	±1,500V	±1,500V	N/A	±1,500V	±1,500V	±150V	±150V	N/A	±150V	±150V
ZU27DR	Pass	±1,500V	±1,500V	N/A	±1,500V	±1,500V	±150V	±150V	N/A	±150V	±150V
ZU28DR	Pass	±1,500V	±1,500V	N/A	±1,500V	±1,500V	±150V	±150V	N/A	±150V	±150V
ZU29DR	Pass	±1,500V	±1,500V	N/A	±1,500V	±1,500V	±150V	±150V	N/A	±150V	±150V

Failure Rate Determination

The failure rate is typically defined in FIT units. One FIT equals 1 failure per 1 billion device hours. For example, 5 failures expected out of 1 million components operating for 1,000 hours have a failure rate of 5 FIT. The following is the failure rate calculation method:

$$Failure\ Rate = \frac{x^2 10^9}{2(No.\ of\ Devices)(No.\ of\ Hours)(Acc.\ Factor)} \quad \textit{Equation 1-1}$$

where:

x^2 = Chi-squared value at a desired confidence level and (2f + 2) degrees of freedom, where f is the number of failures.

The acceleration factor is calculated using the Arrhenius relationship:

$$A = \exp\left\{\frac{E_a}{k}\cdot\left(\frac{1}{T_{J1}} - \frac{1}{T_{J2}}\right)\right\} \quad \textit{Equation 1-2}$$

where:

E_a = Thermal activation energy (0.7eV is assumed and used in failure rate calculation except EPROM in which 0.58 eV is used).

A = Acceleration factor

k = Boltzmann's constant, 8.617164 x 10^{-5} eV/K

T_{J1} = Use junction temperature in Kelvin (K = °C + 273.16)

T_{J2} = Stress junction temperature in Kelvin (K = °C + 273.16)

Failure Rate Summary

Table 1-18: **Summary of the Failure Rates**

Process Technology	Device Hours at TJ = 125°C	FIT (1)
16 nm	1,411,811	10
20 nm	1,054,884	13
28 nm	1,133,597	11
40 nm	1,133,274	10
45 nm	1,027,456	11
65 nm	2,036,838	6
90 nm	7,405,362	2
130 nm	2,256,834	5
150 nm	2,032,788	6
180 nm	1,086,123	11
220 nm/180 nm	1,003,249	12
350 nm/250 nm	1,187,017	10
350 nm	1,013,887	12

Notes:
1. FIT is calculated based on 0.7 eV (0.58 eV for EPROM), 60% C.L. and TJ of 55°C.

SEU and Soft Error Rate Measurements

Table 1-19 and Table 1-20 show the soft error rates caused by single event upsets (SEUs) affecting memory cells used as configuration memory and block RAM. Neutron cross-sections are determined from LANSCE beam testing according to JESD89A/89-3A. Soft error rates (in FIT/Mb) are determined from real-time (system level) measurements in various locations and altitudes and corrected for New York City, according to JESD89A/89-1A. Also refer to *Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits* (WP286) [Ref 2]. All data is current as of the date of this report.

An upset in any configuration bit does not create a soft functional error per se. The bit has to be one that is critical to the function in order for a soft functional error to occur. The

number of unused bits and non-critical bits reduces the effective soft error rate by what is known as the device vulnerability factor (DVF). The DVF for a typical design is 5% (one in 20 upsets, on average, cause a functional soft error). In the worst case, the DVF is never larger than one in ten, or never more than 10% of the upsets cause a soft functional error. Therefore, the functional soft error rate of a design running in a Xilinx FPGA is far lower than what is predicted by calculation from the data in Table 1-19 and Table 1-20. The significant factor contributing to low DVF is that most FPGA routing resources are unused within any particular implementation.

Xilinx offers a significant portfolio of SEU analysis and mitigation solutions to help you understand and interpret soft error rates and manage SEU rates in any given design. Consult your Xilinx sales and field support for assistance in understanding these capabilities, and visit our Single Event Upsets website to obtain the Xilinx SEU Estimator tool for modeling device-level SEU rates based on operating environment and the data in Table 1-19 and Table 1-20. The Xilinx SEU Estimator tool models total SEU rate in terrestrial environments by scaling the real-time data based on operating environment and adding the alpha particle data.

In Table 1-19 and Table 1-20, Tech Node is technology node, CRAM is configuration RAM, and BRAM is block RAM. The data in these tables is not a specification but is for reference only, under the stated conditions for each experiment.

Table 1-19: **Experimental Beam Testing and Real-Time Soft Error Rates for CRAM (1)**

Tech Node	Product Family	LANSCE Neutron Cross-section per Bit (2)		FIT/Mb (Thermal Neutrons)		FIT/Mb (Alpha Particle) (3)		FIT/Mb (4) (Real-Time Soft Error Rate Per Event)(5)(7)	
		CRAM	Error	CRAM	Error(6)	CRAM	Error(6)	CRAM	Error(6)
180 nm	Virtex-E	1.12×10^{-14}	±18%					181	±20%
150 nm	Virtex-II	2.56×10^{-14}	±18%					405	±8%
130 nm	Virtex-II Pro	2.74×10^{-14}	±18%					437	±8%
90 nm	Virtex-4	1.55×10^{-14}	±18%					263	±11%
90 nm	Spartan-3	2.40×10^{-14}	±18%					190	–50% +80%
90 nm	Spartan-3E, Spartan-3A	1.31×10^{-14}	±18%					104	–80% +90%
65 nm	Virtex-5	6.70×10^{-15}	±18%					165	–13% +15%
45 nm	Spartan-6	1.00×10^{-14}	±18%	21	–11% +13%	88	–50% +100%	177	–10% +11%
40 nm	Virtex-6	1.26×10^{-14}	±18%	0.7	–11% +13%	7	–45% +97%	105	–10% +11%

Table 1-19: **Experimental Beam Testing and Real-Time Soft Error Rates for CRAM *(Cont'd)*[1]**

Tech Node	Product Family	LANSCE Neutron Cross-section per Bit [2]		FIT/Mb (Thermal Neutrons)		FIT/Mb (Alpha Particle) [3]		FIT/Mb [4] (Real-Time Soft Error Rate Per Event)[5][7]	
		CRAM	Error	CRAM	Error[6]	CRAM	Error[6]	CRAM	Error[6]
28 nm	Artix-7, Spartan-7, and Zynq-7000	6.99×10^{-15}	±18%	29	–10% +10%	43	–41% +80%	76	–8% +9%
28 nm	Kintex-7 and Virtex-7	5.69×10^{-15}	±18%	1.1	–15% +18%	43	–41% +80%	50	-20% +26%
20 nm	UltraScale	2.55×10^{-15}	±18%	0.5	–13% +16%	9	–64% +374%	31	-14% +17%
16 nm	UltraScale+	2.67×10^{-16}	±18%	0.35	–16% +20%	0.1	–20% +20%	5	-27% +39%

Notes:

1. Experiments are performed at ambient temperature with typical power supply voltages.
2. Data from Los Alamos Neutron Science Center (LANSCE).
3. Spartan-6 and UltraScale+ FPGA alpha data is based on alpha foil testing and package alpha emissivity of 0.001 counts/cm2/hr. Virtex-6, 7 series, and UltraScale FPGA alpha data estimated using real-time underground cave testing.
4. One FIT equals 1 failure per 1 billion device hours. Mb = 1e6 memory bits.
5. Data compiled from Rosetta experiment which includes upsets from neutron, proton, and thermal neutron secondaries. Based on experimental methodology, upsets from alpha particles are not included. Modeling of the total SEU rate in terrestrial environments requires use of alpha particle data in addition to real-time data. Xilinx advises use of the SEU Estimator tool to model total SEU rates.
6. 90% confidence interval.
7. Soft error rates (in FIT/Mb) are determined from real-time (system level) measurements in various locations and altitudes and corrected for New York City, according to JESD89A/89-1A.

Table 1-20: **Experimental Beam Testing and Real-Time Soft Error Rates for BRAM [1]**

Tech Node	Product Family	LANSCE Neutron Cross-section per Bit [2]		FIT/Mb (Thermal Neutrons)		FIT/Mb (Alpha Particle)[3]		FIT/Mb [4] (Real-Time Soft Error Rate Per Event) [5][7]	
		BRAM	Error	BRAM	Error[3]	BRAM	Error[6]	BRAM	Error[6]
180 nm	Virtex-E	1.12×10^{-14}	±18%					181	±20%
150 nm	Virtex-II	2.64×10^{-14}	±18%					478	±8%
130 nm	Virtex-II Pro	3.91×10^{-14}	±18%					770	±8%
90 nm	Virtex-4	2.74×10^{-14}	±18%					484	±11%
90 nm	Spartan-3	3.48×10^{-14}	±18%					373	–50% +80%
90 nm	Spartan-3E, Spartan-3A	2.73×10^{-14}	±18%					293	–80% +90%

Table 1-20: **Experimental Beam Testing and Real-Time Soft Error Rates for BRAM *(Cont'd)*[1]**

Tech Node	Product Family	LANSCE Neutron Cross-section per Bit [2]		FIT/Mb (Thermal Neutrons)		FIT/Mb (Alpha Particle)[3]		FIT/Mb [4] (Real-Time Soft Error Rate Per Event) [5][7]	
		BRAM	Error	BRAM	Error[3]	BRAM	Error[6]	BRAM	Error[6]
65 nm	Virtex-5	3.96×10^{-14}	±18%					692	–13% +15%
45 nm	Spartan-6	2.20×10^{-14}	±18%	83	–11% +13%	172	–50% +100%	370	–10% +11%
40 nm	Virtex-6	1.14×10^{-14}	±18%	1.4	–11% +13%	120	–45% +97%	213	–10% +11%
28 nm	Artix-7, Spartan-7, and Zynq-7000	6.32×10^{-15}	±18%	41	–10% +10%	39	–41% +80%	73	–8% +9%
28 nm	Kintex-7 and Virtex-7	5.57×10^{-15}	±18%	1.8	–15% +18%	39	–41% +80%	44	-36% +62%
20 nm	UltraScale	4.43×10^{-15}	±18%	1.1	–13% +16%	16	–64% +374%	49	-32% +50%
16 nm	UltraScale+	9.82×10^{-16}	±18%	4.7	–12% +13%	0.2	–20% +20%	16	-26% +38%

Notes:

1. Experiments are performed at ambient temperature with typical power supply voltages.
2. Data from Los Alamos Neutron Science Center (LANSCE).
3. Spartan-6 and UltraScale+ FPGA alpha data is based on alpha foil testing and package alpha emissivity of 0.001 counts/cm^2/hr. Virtex-6, 7 series, and UltraScale FPGA alpha data is estimated using real-time underground cave testing.
4. One FIT equals 1 failure per 1 billion device hours. Mb = 1e6 memory bits.
5. Data compiled from Rosetta experiment which includes upsets from neutron, proton, and thermal neutron secondaries. Based on experimental methodology, upsets from alpha particles are not included. Modeling of the total SEU rate in terrestrial environments requires use of alpha particle data in addition to real-time data. Xilinx advises use of the SEU Estimator tool to model total SEU rates.
6. 90% confidence interval.
7. Soft error rates (in FIT/Mb) are determined from real-time (system level) measurements in various locations and altitudes and corrected for New York City, according to JESD89A/89-1A.

Results by Product Family

FPGA Products

High-Temperature Operating Life (HTOL) Test

The HTOL test is conducted under the conditions of $T_J \geq 125°C$ temperature, maximum V_{DD} and either dynamic or static operation. The FIT failure rate calculation in the following tables is based on the assumption of 0.7 eV activation energy and 60% confidence level (CL).

Summary

The failures listed in Table 2-1 are also listed in each family device table with failure analysis results in the footnotes.

Table 2-1: **Summary of HTOL Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC2Sxxx	13	0	528	902,135	1,003,249	12
XC2VPxxx	5	0	224	426,225	1,094,576	11
XCE2VPxxx	8	0	384	834,489	1,162,258	10
XC3Sxxx	10	0	445	802,610	1,017,942	12
XC3SxxxE	10	0	480	787,485	1,060,761	12
XC3SxxxA	9	0	474	788,582	1,048,905	12
XC3SxxxAN	10	0	639	776,036	1,048,055	11
XC3SDxxxA	7	0	293	565,731	1,020,458	12
XC4VxXxxx	6	0	304	611,012	1,208,215	10
XCE4VxXxxx	8	0	358	539,962	1,001,025	12
XC5VxXxxx	6	0	264	484,024	1,159,420	10
XCE5VxXxxx	4	0	294	339,000	877,418	13
XC6Sxxx	6	0	269	538,540	1,027,456	11

Table 2-1: **Summary of HTOL Test Results *(Cont'd)***

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC6VxXxxx	6	0	270	540,000	1,133,274	10
7 series FPGAs and Zynq-7000 SoCs	9	0	439	810,500	1,044,069	11
UltraScale™ devices	11	0	437	571,000	922,508	13
UltraScale+™ devices	7	0	408	611,000	1,180,065	10

Table 2-2: **HTOL Test Results for 220/180 nm Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC2S30	3	0	134	270,186	299,635	12
XC2S50	1	0	43	86,387	93,969	
XC2S100	5	0	225	293,310	330,300	
XC2S200	1	0	45	90,090	107,002	
XC2S150	3	0	81	162,162	172,342	
XC2Sxxx	13	0	528	902,135	1,003,249	

Table 2-3: **HTOL Test Results for 130 nm Si Gate CMOS Device Type XC2VPxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J > 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC2VP40	5	0	224	426,225	1,094,576	11
XC2VPxxx	5	0	224	426,225	1,094,576	

Table 2-4: **HTOL Test Results for 130 nm Si Gate CMOS Device Type XCE2VPxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at T_J > 125°C	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XCE2VP7	2	0	134	399,152	399,152	10
XCE2VP40	2	0	89	178,675	301,000	
XCE2VP50	3	0	139	234,662	410,490	
XCE2VP70	1	0	22	22,000	51,616	
XCE2VPxxx	8	0	384	834,489	1,162,258	

Table 2-5: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XC3S400	4	0	175	306,035	374,236	12
XC3S1000	4	0	180	361,080	463,462	
XC3S1500	2	0	90	135,495	180,244	
XC3Sxxx	10	0	445	802,610	1,017,942	

Table 2-6: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XC3S250E	2	0	90	183,060	221,112	12
XC3S500E	4	0	178	313,820	421,895	
XC3S700E	1	0	45	45,000	50,809	
XC3S1600E	3	0	167	245,605	366,945	
XC3SxxxE	10	0	480	787,485	1,060,761	

Table 2-7: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XC3SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XC3S1400A	9	0	474	788,582	1,048,905	12
XC3SxxxxA	9	0	474	788,582	1,048,905	

Table 2-8: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XC3SxxxAN**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC3S700AN	3	0	231	231,000	274,236	11
XC3S1400AN	7	0	408	545,036	773,818	
XC3SxxxAN	10	0	639	776,036	1,048,055	

Table 2-9: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XC3SDxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC3SD1800A	2	0	90	180,135	276,987	12
XC3SD3400A	5	0	203	385,596	743,471	
XC3SDxxxA	7	0	293	565,731	1,020,458	

Table 2-10: **HTOL Test Results for 45 nm Si Gate CMOS Device Type XC6Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC6SLX100T	1	0	45	90,000	239,814	11
XC6SLX45T	5	0	224	448,540	787,642	
XC6Sxxx	6	0	269	538,540	1,027,456	

Table 2-11: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XC4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC4VLX40	2	0	125	250,090	373,345	10
XC4VLX160	1	0	44	88,132	414,302	
XC4VFX20	2	0	90	182,565	267,152	
XC4VFX40	1	0	45	90,225	153,416	
XC4VxXxxx	6	0	304	611,012	1,208,215	

Table 2-12: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XCE4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCE4VLX40	3	0	133	223,522	362,809	12
XCE4VLX80	3	0	135	180,540	449,482	
XCE4VSX25	2	0	90	135,900	188,735	
XCE4VxXxx	8	0	358	539,962	1,001,026	

Table 2-13: **HTOL Test Results for 65 nm Si Gate CMOS Device Type XC5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC5VLX110T	6	0	264	484,024	1,159,420	10FIT
XC5VxXxxx	6	0	264	484,024	1,159,420	

Table 2-14: **HTOL Test Results for 65 nm Si Gate CMOS Device Type XCE5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCE05L11	3	0	249	249,000	630,879	13
XCE05L11T	1	0	45	90,000	246,539	
XCE5VxXxxx	4	0	294	339,000	877,418	

Table 2-15: **HTOL Test Results for 40 nm Si Gate CMOS Device Type XC6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC6VLX130T	1	0	45	90,000	188,879	10
XC6VLX240T	5	0	225	450,000	944,395	
XC6VxXxxx	6	0	270	540,000	1,133,274	

Table 2-16: **HTOL Test Results for 28 nm Si Gate CMOS Device Type in 7 Series FPGAs and Zynq-7000 SoCs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC7K325T	2	0	90	112,500	144,920	11
XC7Z030	1	0	80	160,000	206,109	
XC7Z020	6	0	269	538,000	693,040	
7 series FPGAs and Zynq-7000 SoCs	9	0	439	810,500	1,044,069	

Table 2-17: **HTOL Test Results for 20 nm Si Gate CMOS Device Type in UltraScale FPGAs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCKU040	5	0	256	390,000	678,175	13
XCKU115	3	0	47	47,000	63,445	
XCVU190	3	0	134	134,000	180,888	
UltraScale devices	11	0	437	571,000	922,508	

Table 2-18: **HTOL Test Results for 16 nm Si Gate CMOS Device Type in the UltraScale+ Family**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCZU3EG	3	0	240	320,000	618,037	10
XCZU9EG	2	0	90	135,000	260,735	
XCZU28DR	2	0	78	156,000	301,283	
UltraScale+ devices	7	0	408	611,000	1,180,065	

Temperature Humidity with Bias Test

The THB test is conducted under the conditions of 85°C and 85% RH and VDD bias. Package preconditioning is performed on the testing samples prior to the THB test.

The failures listed in Table 2-19 are also listed by device with failure analysis results in the footnotes.

Summary

Table 2-19: **THB Test Results for Si Gate CMOS Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2Cxxx	6	0	269	403,000
XC2VPxxx	4	0	180	180,000
XC3Sxxx	3	0	135	135,000
XC3SxxxE	12	0	539	696,500
XC3SxxxAN	3	0	81	140,400
XC4VxXxxx	3	0	66	99,000
XC5VxXxxx	7	0	310	245,000
XC6VxXxxx	4	0	180	157,500
7 series FPGAs	34	0	1,326	1,551,966
UltraScale devices	11	0	366	367,821
UltraScale+ devices	8	0	266	269,108

Data

Table 2-20: **THB Test Results for Si Gate CMOS Device Type XC2VPxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2VP40	4	0	180	180,000
XC2VPxxx	4	0	180	180,000

Table 2-21: **THB Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S400	3	0	135	135,000
XC3Sxxx	3	0	135	135,000

Table 2-22: **THB Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S100E	3	0	135	135,000
XC3S250E	5	0	224	224,000
XC3S1200E	4	0	180	337,500
XC3SxxxE	12	0	539	696,500

Table 2-23: **THB Test Results for Si Gate CMOS Device Type XC3SxxxAN**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S1400AN	3	0	81	140,400
XC3SxxxAN	3	0	81	140,400

Table 2-24: **THB Test Results for Si Gate CMOS Device Type XC4Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4VFX60	3	0	66	99,000
XC4Vxxx	3	0	66	99,000

Table 2-25: **THB Test Results for Si Gate CMOS Device Type XC5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC5VLX110T	4	0	180	180,000
XC5VLX155T	3	0	130	65,000
XC5VxXxxx	7	0	310	245,000

Table 2-26: **THB Test Results for Si Gate CMOS Device Type XC6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6VLX130T	1	0	45	45,000
XC6VLX240T	3	0	135	112,500
XC6VxXxxx	4	0	180	157,500

Table 2-27: **THB Test Results for Si Gate CMOS Device Types in 7 Series FPGA and Zynq-7000 SoC Families**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC7A200T	9	0	409	409,000
XC7K325T	12	0	268	269,842
XC7V2000T	4	0	107	107,042
XC7Z020	5	0	224	448,000
XC7S50	4	0	318	318,082
7 series FPGAs and Zynq-7000 SoCs	34	0	1,326	1,551,966

Table 2-28: **THB Test Results for Si Gate CMOS Device Types in the UltraScale Family**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCKU040	4	0	179	179,000
XCKU115	5	0	120	121,701
XCVU190	1	0	40	40,120
XCVU440	1	0	27	27,000
UltraScale devices	11	0	366	367,821

Table 2-29: **THB Test Results for Si Gate CMOS Device Types in the UltraScale+ Family**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCZU3EG	6	0	177	177,820
XCZU9EG	2	0	89	91,288
UltraScale+ devices	8	0	266	269,108

Temperature Humidity Test

The TH test is conducted under the conditions of 85°C and 85% RH Package preconditioning is performed on the testing samples prior to the TH test.

Summary

Table 2-30: **Summary of TH Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
7 series FPGAs and Zynq-7000 SoCs	7	0	544	544,000
UltraScale devices	1	0	44	44,000
UltraScale+ devices	5	0	240	460,000

Data

Table 2-31: **TH Test Results for Si Gate CMOS Device Types in 7 Series FPGAs and Zynq-7000 SoCs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC7S50	4	0	313	313,000
XC7Z030	3	0	231	231,000
7 series FPGAs and Zynq-7000 SoCs	7	0	544	544,000

Table 2-32: **TH Test Results for Si Gate CMOS Device Types in the UltraScale Family**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCKU115	1	0	44	44,000
UltraScale devices	1	0	44	44,000

Table 2-33: **TH Test Results for Si Gate CMOS Device Types in the UltraScale+ Family**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCZU3EG	5	0	240	460,000
UltraScale+ devices	5	0	240	460,000

Temperature Cycling Test

The temperature cycling test is conducted under the conditions of predefined maximum and minimum temperatures and in air-to-air environment. Package precondition is performed on the testing samples prior to the temperature cycling test.

Summary

Table 2-34: **Summary of Temperature Cycling Test Results**

Device	Lot Quantity	Failures	Device on Test	Total Device Cycles
XC2VPxxx	4	0	176	176,000
XC3Sxxx	4	0	180	180,000
XC3SxxxE	11	0	480	600,000
XC3SxxxA	4	0	180	180,000
XC3SxxxAN	7	0	189	283,500
XC6Sxxx	5	0	249	408,000
XC4VxXxxx	3	0	74	148,000
XC5VxXxxx	10	0	309	470,500
XC6VxXxxx	4	0	180	180,000
7 series FPGAs and Zynq-7000 SoCs	50	0	2,350	2,722,666
UltraScale devices	56	0	1,630	2,345,167
UltraScale+ devices	45	0	1,536	2,373,686

Data

Table 2-35: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC2VPxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2VP40	B: –55°C to +125°C	4	0	176	176,000
XC2VPxxx	B: –55°C to +125°C	4	0	176	176,000

Table 2-36: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S400	B: –55°C to +125°C	4	0	180	180,000
XC3Sxxx	B: –55°C to +125°C	4	0	180	180,000

Table 2-37: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S100E	B: –55°C to +125°C	3	0	135	135,000
XC3S250E	B: –55°C to +125°C	5	0	225	225,000
XC3S1200E	B: –55°C to +125°C	3	0	120	240,000
XC3SxxxE	B: –55°C to +125°C	11	0	480	600,000

Table 2-38: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S200A	B: –55°C to +125°C	4	0	180	180,000
XC3SxxxA	B: –55°C to +125°C	4	0	180	180,000

Table 2-39: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3SxxxAN**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S50AN	B: –55°C to +125°C	3	0	81	121,500
XC3S400AN	B: –55°C to +125°C	3	0	81	121,500
XC3S1400AN	B: –55°C to +125°C	1	0	27	40,500
XC3SxxxAN	B: –55°C to +125°C	7	0	189	283,500

Table 2-40: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC6Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC6SLX45T	B: –55°C to +125°C	4	0	159	318,000
XC6SLX150	B: –55°C to +125°C	1	0	90	90,000
XC6Sxxx	B: –55°C to +125°C	5	0	249	408,000

Table 2-41: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC4VxXxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC4VFX140	B: –55°C to +125°C	3	0	74	148,000
XC4VxXxxx	B: –55°C to +125°C	3	0	74	148,000

Table 2-42: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC5VxXxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC5VLX50T	B: –55°C to +125°C	3	0	75	150,000
XC5VLX110T	B: –55°C to +125°C	3	0	135	135,000
XC5VFX200T	B: –55°C to +125°C	4	0	99	185,500
XC5VXxXxxx	B: –55°C to +125°C	10	0	309	470,500

Table 2-43: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC6VxXxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC6VLX130T	B: –55°C to +125°C	1	0	45	45,000
XC6VLX240T	B: –55°C to +125°C	3	0	135	135,000
XC6VxXxxx	B: –55°C to +125°C	4	0	180	180,000

Table 2-44: **Temperature Cycling Test Results for Si Gate CMOS Device Types in 7 Series FPGAs and Zynq-7000 SoCs**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC7A100T	B: –55°C to +125°C	7	0	315	360,000
XC7A200T	B: –55°C to +125°C	5	0	225	225,000
XC7K325T	B: –55°C to +125°C	5	0	225	225,000
XC7S15	B: –55°C to +125°C	3	0	243	243,000
XC7S50	B: –55°C to +125°C	4	0	331	332,066
XC7S100	B: –55°C to +125°C	6	0	239	340,100
XC7V2000T	B: –55°C to +125°C	7	0	190	286,500
XC7X690T	B: –55°C to +125°C	1	0	27	27,000

Table 2-44: **Temperature Cycling Test Results for Si Gate CMOS Device Types in 7 Series FPGAs and Zynq-7000 SoCs *(Cont'd)***

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC7Z020	B: –55°C to +125°C	5	0	204	363,000
XC7Z030	B: –55°C to +125°C	3	0	231	231,000
XC7Z100	B: –55°C to +125°C	1	0	45	45,000
7 series FPGAs and Zynq-7000 SoCs	B: –55°C to +125°C	50	0	2,350	2,722,666

Table 2-45: **Temperature Cycling Test Results for Si Gate CMOS Device Types in UltraScale FPGAs**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCKU040	B: –55°C to +125°C	7	0	314	471,000
XCKU095	B: –55°C to +125°C	2	0	89	133,500
XCVU095	B: –55°C to +125°C	5	0	222	298,000
XCKU115	G: -40°C to +125°C	18	0	444	569,145
XCVU125	G: -40°C to +125°C	6	0	129	187,800
XCVU160	G: -40°C to +125°C	1	0	44	37,792
XCVU190	G: -40°C to +125°C	3	0	100	200,550
XCVU440	G: -40°C to +125°C	14	0	288	447,200
UltraScale devices	B: –55°C to +125°C G: -40°C to +125°C	56	0	1,630	2,345,167

Table 2-46: **TC Test Results for Si Gate CMOS Device Types in the UltraScale+ Family**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCZU3EG	B: –55°C to +125°C	16	0	755	1,296,000
XCZU9EG	B: –55°C to +125°C	8	0	360	517,500
XCZU15EG	B: –55°C to +125°C	1	0	44	52,800
XCKU15P	B: –55°C to +125°C	8	0	197	219,228
XCVU9P	G: -40°C to +125°C	12	0	180	288,158
UltraScale+ devices	B: –55°C to +125°C G: -40°C to +125°C	45	0	1,536	2,373,686

High Accelerated Stress Test

The HAST test is conducted under the conditions of 130°C, 85% RH and V_{DD} bias or 110°C, 85% RH and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the HAST test.

Summary

Table 2-47: **Summary of HAST Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3SxxxA	4	0	180	47,520
XC3SxxxAN	3	0	81	42,768
XC6Sxxx	6	0	330	154,440
7 series FPGAs and Zynq-7000 SoCs	8	0	359	118,272

Data

Table 2-48: **HAST Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S200A	110°C, 85% RH	4	0	180	47,520
XC3SxxxA	110°C, 85% RH	4	0	180	47,520

Table 2-49: **HAST Test Results for Si Gate CMOS Device Type XC3SxxxAN**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S1400AN	110°C, 85% RH	3	0	81	42,768
XC3SxxxxAN	110°C, 85% RH	3	0	81	42,768

Table 2-50: **HAST Test Results for Si Gate CMOS Device Type XC6Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6SLX9	110°C, 85% RH	1	0	75	38,600
XC6SLX25T	110°C, 85% RH	1	0	75	19,800
XC6SLX45T	110°C, 85% RH	4	0	180	95,040
XC6Sxxx	110°C, 85% RH	6	0	330	154,440

Table 2-51: **HAST Test Results for Si Gate CMOS Device Types in 7 Series FPGAs and Zynq-7000 SoCs**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC7A100T	110°C, 85% RH	7	0	314	94,512
XC7Z020	110°C, 85% RH	1	0	45	23,760
7 series FPGAs and Zynq-7000 SoCs	110°C, 85% RH	8	0	359	118,272

High Temperature Storage Life

The High-Temperature Storage Life test is conducted under the conditions of 150°C and with the device unbiased.

Summary

Table 2-52: **Summary of High-Temperature Storage Life Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3Sxxx	2	0	89	89,000
XC3SxxxE	11	0	495	585,500
XC3SxxxA	4	0	180	180,000
XC3SxxxAN	9	0	241	482,000
XC4Vxxx	3	0	75	150,000
XC5Vxxx	8	0	220	382,500
XC6Sxxx	3	0	134	268,000
XC6Vxxx	3	0	134	134,000
7 series FPGAs and Zynq-7000 SoCs	33	0	1,234	1,594,495
UltraScale devices	26	0	861	1,299,865
UltraScale+ devices	17	0	413	766,181

Data

Table 2-53: **High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S400	2	0	89	89,000
XC3Sxxx	2	0	89	89,000

Table 2-54: **High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S100E	3	0	135	135,000
XC3S250E	5	0	225	202,500
XC3S1200E	3	0	135	225,000
XC3SxxxE	11	0	495	585,000

Table 2-55: **High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC4Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4VFX140	3	0	75	150,000
XC4Vxxx	3	0	75	150,000

Table 2-56: **High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC5Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC5VFX200T	4	0	100	187,500
XC5VLX110	1	0	45	45,000
XC5VLX50T	3	0	75	150,000
XC5Vxxx	8	0	220	382,500

Table 2-57: **High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC6Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6VLX240T	3	0	134	134,000
XC6Vxxx	3	0	134	134,000

Table 2-58: **High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S200A	4	0	180	180,000
XC3SxxxA	4	0	180	180,000

Table 2-59: **High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC3SxxxAN**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S50AN	3	0	81	162,000
XC3S400AN	3	0	81	162,000

Table 2-59: **High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC3SxxxAN**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S1400AN	3	0	79	158,000
XC3SxxxAN	9	0	241	482,000

Table 2-60: **High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC6Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6SLX45T	3	0	134	268,000
XC6Sxxx	3	0	134	268,000

Table 2-61: **High-Temperature Storage Life Test Results for Si Gate CMOS Device Types in 7 Series FPGAs and Zynq-7000 SoCs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC7A100T	7	0	314	314,000
XC7A200T	5	0	225	225,000
XC7VX980T	3	0	75	90,000
XC7Z020	6	0	270	540,000
XC7Z030	1	0	45	45,000
XC7V2000T	4	0	120	195,000
XC7S50	7	0	185	185,495
7 series FPGAs and Zynq-7000 SoCs	33	0	1,234	1,594,495

Table 2-62: **High-Temperature Storage Life Test Results for Si Gate CMOS Device Type UltraScale FPGAs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCKU040	7	0	314	314,000
XCKU115	15	0	451	747,865
XCVU190	2	0	50	125,000
XCVU440	2	0	46	113,000
UltraScale FPGAs	26	0	861	1,299,865

Table 2-63: **High-Temperature Storage Life Test Results for Si Gate CMOS Device Type UltraScale+ Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCZU3EG	3	0	99	198,000
XCZU9EG	3	0	134	223,000

Table 2-63: **High-Temperature Storage Life Test Results for Si Gate CMOS Device Type UltraScale+ Devices *(Cont'd)***

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCVU9P	11	0	180	345,181
UltraScale+ devices	17	0	413	766,181

Flash PROM Products

HTOL Test

The HTOL test is conducted under the conditions of $T_J \geq 125°C$ temperature, maximum V_{DD}, and either dynamic or static operation. The FIT failure rate calculation in the following tables is based on the assumption of 0.7 eV activation energy and 60% confidence level (CL).

Summary

Table 2-64: **Summary of HTOL Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC18Vxxx	16	0	715	760,225	1,004,700	12
XCFxxxS/P	19	0	948	925,500	1,028,088	12

Data

Table 2-65: **HTOL Test Results for 0.15 µm Si Gate CMOS Device Type 18Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC18V02	6	0	265	265,000	303,152	12
XC18V04	9	0	405	405,000	609,828	
XC18V512	1	0	45	90,225	91,720	
XC18Vxxx	16	0	715	760,225	1,004,700	

Table 2-66: **HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCF04S	2	0	121	121,000	185,435	12
XCF08P	4	0	180	180,000	180,000	
XCF16P	3	0	135	135,000	135,000	
XCF32P	9	0	467	467,000	467,000	
XCF128X	1	0	45	22,500	22,500	
XCFxxxS/P	19	0	948	925500	1,028,088	

Temperature Humidity with Bias Test

The THB test is conducted under the conditions of 85°C, 85% RH, and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the THB test.

Summary

Table 2-67: **Summary of THB Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCFxxxS/P	8	0	360	600,480

Table 2-68: **THB Test Results for Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCF16P	1	0	45	75,060
XCF32P	7	0	315	525,420
XCFxxxS/P	8	0	360	600,480

Temperature Cycling Tests

The temperature cycling test is conducted under the conditions of predefined maximum and minimum temperatures and in an air-to-air environment. Package precondition is performed on the testing samples prior to the temperature cycling test.

Summary

Table 2-69: **Summary of Temperature Cycling Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCFxxxS/P	6	0	270	441,180

Data

Table 2-70: **Temperature Cycling Test Results for Si Gate CMOS Device Type XCFxxxS/P**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCF32P	C: –65°C to +150°C	6	0	270	441,180
XCFxxxS/P	C: –65°C to +150°C	6	0	270	441,180

Autoclave Test

The autoclave test is conducted under the conditions of 121°C, 100% RH (unbiased), and 29.7 PSI. Package preconditioning is performed on the testing samples prior to the autoclave stress test.

Summary

Table 2-71: **Summary of Autoclave Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCFxxxS/P	6	0	270	25,920

Data

Table 2-72: **Autoclave Test Results for Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCF32P	6	0	270	25,920
XCFxxxS/P	6	0	270	25,920

Program/Erase Endurance Test

The Program/Erase Endurance test is conducted under nominal voltage and room temperature.

Qualification Data

Table 2-73: **Program/Erase Endurance Test Results for Si Gate CMOS Device Type XC18Vxxx/XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC18V04	1	0	32	640,000
XCF08P	1	0	16	320,000
XCF16P	2	0	93	1,860,000
XCF32P	2	0	93	1,860,000

Data Retention Bake Test

The data retention bake test is conducted at 150°C ambient temperature. The devices are programmed prior to the bake test.

Summary

Table 2-74: **Summary of Data Retention Bake Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCFxxxS/P	6	0	270	450,360

Data

Table 2-75: **Data Retention Bake Test Results for Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCF32P	6	0	270	450,360
XCFxxxS/P	6	0	270	450,360

CPLD Products

HTOL Tests

The HTOL test is conducted under the conditions of T_J > 125°C temperature, maximum V_{DD}, and either dynamic or static operation. The FIT calculations in Table 2-76 through Table 2-79 are based on the assumption of 0.7 eV activation energy and 60% confidence level.

Summary

Table 2-76: **Summary of HTOL Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC95xxxXL	11	0	472	910,747	1,187,047	10
XCRxxxXL	12	0	538	1,011,913	1,013,887	12
XC2Cxxx/A	12	0	538	1,080,544	1,086,123	11

Data

Table 2-77: **HTOL Test Results for 0.35 µm Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC95144XL	3	0	132	266,207	461,918	10
XC95288XL	2	0	90	180,810	316,098	
XC9572XL	6	0	250	463,730	409,002	
XC95xxxXL	11	0	472	910,747	1,187,017	

Table 2-78: **HTOL Test Results for 0.35 µm Si Gate CMOS Device Type XCRxxxXL**

Devices	Lot Quantity	Failures	Device on Test	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCR3064XL	1	0	45	225,00	227,37	12
XCR3128XL	3	0	135	270,855	271,487	
XCR3256XL	4	0	176	351,868	253,614	
XCR3384XL	3	0	134	270,114	270,114	
XCR3512XL	1	0	48	96,576	96,576	
XCRxxxXL	12	0	538	1,011,913	1,013,887	

Table 2-79: **HTOL Test Results for 0.18 µm Si Gate CMOS Device Type XC2Cxxx/A**

Devices	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC2C128	8	0	359	719,483	724,176	11
XC2C256	2	0	89	179,981	180,275	
XC2C384	1	0	45	90,090	90,990	
XC2C512	1	0	45	90,090	90,682	
XC2Cxxx/A	12	0	538	1,080,544	1,086,123	

Temperature Humidity with Bias Test

The THB test is conducted under the conditions of 85°C, 85% RH, and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the THB test.

Summary

Table 2-80: **Summary of THB Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95xxxXL	5	0	224	448,000
XC2Cxxx/A	6	0	269	403,000

Data

Table 2-81: **THB Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC9572XL	5	0	224	448,000
XC95xxxXL	5	0	224	448,000

Table 2-82: **THB Test Results for Si Gate CMOS Device Type XC2Cxxx/A**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2C128	4	0	179	358,000
XC2C64A	2	0	90	45,000
XC2Cxxx/A	6	0	269	403,000

Temperature Cycling Test

The temperature cycling test is conducted under the conditions of predefined maximum and minimum temperatures and in air-to-air environment. Package precondition is performed on the testing samples prior to the temperature cycling test.

Summary

Table 2-83: **Summary of Temperature Cycling Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC95xxxXL	4	0	165	330,000
XC2Cxxx/A	6	0	250	383,000

Data

Table 2-84: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC9572XL	B: –55°C to +125°C	4	0	165	330,000
XC95xxxXL	B: –55°C to +125°C	4	0	165	330,000

Table 2-85: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC2Cxxx/A**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2C64A	B: –55°C to +125°C	2	0	90	63,000
XC2C128	B: –55°C to +125°C	4	0	160	320,000
XC2Cxxx/A	B: –55°C to +125°C	6	0	250	383,000

Program/Erase Endurance Test

The Program/Erase Endurance test is conducted under nominal voltage and predefined temperature.

Qualification Data

Table 2-86: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxxXL (Test Condition at–40°C)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95144XL	1	0	21	420,000

Table 2-87: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxxXL (Test Condition at 70°C)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95144XL	1	0	32	320,000

Table 2-88: **Erase Endurance Test Results for Si Gate CMOS Device Type XCRxxxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCR3128XL	1	0	10	10,000
XCR3032XL	2	0	57	684,000

Data Retention Bake Test

The Data Retention Bake Test is conducted at 150°C. The devices are programmed prior to the bake test.

Summary

Table 2-89: **Summary of Data Retention Bake Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC95xxxXL	5	0	224	448,000
XCRxxxXL	4	0	180	180,000
XC2Cxxx/A	5	0	223	356,000

Data

Table 2-90: **Data Retention Bake Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC9572XL	5	0	224	448,000
XC95xxxXL	5	0	224	448,000

Table 2-91: **Data Retention Bake Test Results for Si Gate CMOS Device Type XCRxxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCR364XL	1	0	45	45,000
XCR3128XL	1	0	45	45,000
XCR3256XL	2	0	90	90,000
XCRxxxXL	4	0	180	180,000

Table 2-92: **Data Retention Bake Test Results for Si Gate CMOS Device Type XC2Cxxx/A**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2C128	3	0	133	266,000
XC2C64A	2	0	90	90,000
XC2Cxxx/A	5	0	233	356,000

Results by Package Type

Reliability Data for Non-Hermetic Packages

CP56

Table 3-1: **Test Results for Device Type XCR3064XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HTS	1	0	45	45,000

CP132

Table 3-2: **Test Results for Device Types XC2C256 and XC3S250E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	12	0	633	890,900
Temperature humidity 85°C, 85% RH with bias	7	0	420	340,000
HASTU	6	0	321	126,720
HTS	9	0	306	387,000

CS144

Table 3-3: **Test Results for Device Types XC95144XL and XC2S30**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HASTU	5	0	294	155,232
HTS	2	0	52	104,000
Temperature cycling –55°C to +125°C	6	0	316	569,900

CS324

Table 3-4: **Test Results for Device Types XC6SLX45, XC6SLX45T, and XC6SLX9**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	3	0	240	480,000
HAST	8	0	412	158,136
HASTU	1	0	80	42,240
HTS	2	0	54	108,000

FF484

Table 3-5: **Test Results for Device Type XC6SLX45T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HAST	1	0	45	11,880

FF672

Table 3-6: **Test Results for Device Type XC4VFX60**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	6	0	147	241,200
Temperature humidity 85°C, 85% RH with bias	3	0	66	99,000
HTS	3	0	66	79,200

FF900

Table 3-7: **Test Results for Device Type XC7K325T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature humidity 85°C, 85% RH with bias	5	0	129	204,000

FF1136, FF1148, FF1152, FF1156, FF1157, and FF1158

Table 3-8: **Test Results for Device Types XC5VLX110T and XC7A200T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	45,000
Temperature humidity 85°C, 85% RH with bias	2	0	125	85,000
HTS	1	0	45	45,000

FF1696, FF1704, FF1738, FF1759, FF1760, and FF1761

Table 3-9: **Test Results for Device Types XC5VLX330, XC5VFX200T, and XC6VLX550T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	16	0	403	397,800
HTS	12	0	300	397,500

FF1923, FF1924, FF1925, FF1926, FF1927, FF1928, FF1929, and FF1930

Table 3-10: **Test Results for Device Types XC6VHX565T and XC7VX980T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HTS	3	0	75	90,000
Temperature cycling –55°C to +125°C	8	0	211	316,500

FG256

Table 3-11: **Test Results for Device Types XC2S50, XC2S150, and XC2S200**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	6	0	180	193,500

Table 3-11: **Test Results for Device Types XC2S50, XC2S150, and XC2S200 *(Cont'd)***

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HTS	7	0	204	45,000
HASTU	7	0	207	54,648

FG320

Table 3-12: **Test Results for Device Type XC3S1600E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	3	0	75	75,000
HASTU	3	0	75	19,800
HTS	3	0	75	125,000

FG324, FG456, and FG484

Table 3-13: **Test Results for Device Types XC2S200, XC3S400, XC3S1600E, XC6SLX100, XC6SLX45T, and XC7A100T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	30	0	1586	2,535,000
THB	4	0	180	180,000
HAST	15	0	597	204,864
HASTU	12	0	731	181,368
HTS	19	0	767	1,013,000

FG676

Table 3-14: **Test Results for Device Types XC3S1400A and XC3SD3400A**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	4	0	152	205,500
HAST	1	0	80	21,120
THB	3	0	81	140,400
HTS	4	0	124	203,000

FS48

Table 3-15: **Test Results for Device Types XCF08P, XCF16P, and XCF32P**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –65°C to +150°C	1	0	45	75,060
Temperature humidity 85°C, 85% RH with bias	1	0	45	75,060
PP	1	0	45	4,320
HTS	1	0	45	75,060

FT256

Table 3-16: **Test Results for Device Types XCR3512XL, XC2S100E, XC3S50A, XC3S1200E, XC3S400AN, XC3S200, and XC6SLX9**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	21	0	1052	1,574,000
Temperature humidity 85°C, 85% RH with bias	5	0	260	452,500
HASTU	2	0	160	84,480
HAST	8	0	304	101,640
HTS	14	0	645	1,020,000

PQ208

Table 3-17: **Test Results for Device Types XC2S150 and XC2S200E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	3	0	81	121,500
HASTU	4	0	125	54,120
HTS	3	0	99	153,000

TQ100 and TQ144

Table 3-18: **Test Results for Device Types XC2S100, XC3S50AN, XC2C384, XC95144XL, XCR3384XL, and XC6SLX9**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	13	0	553	846,550
THB	6	0	321	480,000
HASTU	5	0	241	21,384
HTS	8	0	225	405,000

VO20 and VO48

Table 3-19: **Test Results for Device Types XCF08P, XCF32P, XC18V01, XC18V02, and XC18V04**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –65°C to +150°C	2	0	90	144,000
Temperature humidity 85°C, 85% RH with bias	2	0	90	150,120
PP	2	0	90	8,640
HTS	1	0	45	75,060

VQ44, VQ64, and VQ100

Table 3-20: **Test Results for Device Types XC9572XL, XC2C128, XC3S100E, XC2C256, and XC3S250E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	23	0	1,161	995,000
Temperature humidity 85°C, 85% RH with bias	20	0	987	1,126,000
HTS	16	0	717	939,000
HASTU	5	0	330	150,480

Reliability Data for Hermetic Packages

Reliability Data for PGA Packages

Table 3-21: **Tests of Package Type PG223**

Code	Test	Sample Quantity	Failures	Total Device Cycles
B2	Resistance to solvents	15	0	
B3	Solderability	15	0	
B5	Bond strength	24	0	
D1	Physical dimension	30	0	
D2	Lead integrity	30	0	
	Seal			
D3	Thermal shock	30	0	450
	Temperature cycle			
	Seal			
	Visual examination			
	End-point electrical			
	Parametrics			
D4	Mechanical shock	30	0	
	Vibration, variable frequency			
	Constant acceleration			
	Seal			
	Visual examination			
	End-point electrical parameters			
D5	Salt atmosphere	30	0	
	Seal			
	Visual examination			
D6	Internal water-vapor content	30	0	
D7	Adhesion of lead finish	30	0	
D8	Lid torque	15	0	

Reliability Data for CB Packages

Table 3-22: **Tests of Package Type CB228**

Code	Test	Sample Quantity	Failures	Total Device Cycles
B2	Resistance to solvents	48	0	
B3	Solderability	27	0	
B5	Bond strength	36	0	
D1	Physical dimension	60	0	
D2	Lead integrity	60	0	
	Seal			
D3	Thermal shock	60	0	
	Temperature cycle			
	Seal			
	Visual examination			
	End-Point electrical			
	Parametrics			
D4	Mechanical shock	60	0	
	Vibration, variable frequency			
	Constant acceleration			
	Seal			
	Visual examination			
	End-point electrical parameters			
D5	Salt atmosphere	60	0	
	Seal			
	Visual examination			
D6	Internal water-vapor content	60	0	
D7	Adhesion of lead finish	60	0	
D8-LID	Lid Torque	30	0	
HTOL	Life Test	45	0	

Reliability Data for CF1144 Package

Table 3-23: **Tests of Package Type CF1144**

Code	Test	Sample Quantity	Failures	Total Device Cycles
D3	Thermal shock	15	0	225
	Parametrics			
D4	Mechanical shock	15	0	
	High temperature storage	22	0	2,112
	Temperature cycling 65 to +155°C	15	0	1,500
	HAST (130°C, 85% RH)	18	0	1,728
TCB	Temperature cycling –55 to +125°C	14	0	29,260

Reliability Data for CG717 Package

Table 3-24: **Tests of Package Type CG717**

Code	Test	Sample Quantity	Failures	Total Device Cycles
	Thermal shock	15	0	225
	Mechanical shock	15	0	
	Vibration	15	0	225
	High temperature storage	22	0	2,112
	Temperature cycling 65 to +155°C	15	0	1,500
	HTOL	44	0	44,000

Reliability Data for Pb-Free Packages

CLG400 and CLG484

Table 3-25: **Test Results for Device Type XC7Z020**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	5	0	204	363,000
HAST	1	0	45	23760
HTS	6	0	270	540,000
THB	5	0	224	448,000

CPG132

Table 3-26: **Test Results for Device Type XC3S250E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	4	0	180	180,000
Temperature humidity 85°C, 85% RH with bias	4	0	180	180,000
HTS	4	0	180	180,000

CPG196

Table 3-27: **Test Results for Device Type XC7S15**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	3	0	243	243,000

CSG324

Table 3-28: **Test Results for Device Types XC6SLX9, XC6SLX25T, and XC7S50**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	3	0	249	249,000
HAST	2	0	150	59,400
Temperature humidity 85°C, 85% RH with bias	3	0	236	236,000
TH	3	0	231	231,000
HTS	6	0	135	135,495

CSG484

Table 3-29: **Test Results for Device Type XC6SLX150T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	90	90,000

FBG484

Table 3-30: **Test Results for Device Type XC7Z030**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	77	77,000

SBV484

Table 3-31: **Test Results for Device Type XCZU3EG**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature Cycling –55 to +125°C	12	0	415	616,000
HTS	2	0	46	92,000
TH	5	0	240	460,000

SFV625

Table 3-32: **Test Results for Device Type XCZU3EG**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HTS	1	0	53	106000
TC	4	0	340	680000
THB	4	0	97	97380

SFV784

Table 3-33: **Test Results for Device Types XCKU040, XCZU3EG, and XCZU5EV**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
THB	2	0	80	80440

FBG676

Table 3-34: **Test Results for Device Type XC7K325T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	21	21,000

FBG900

Table 3-35: **Test Results for Device Type XC7K325T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	4	0	180	180,000
Temperature humidity 85°C, 85% RH with bias	3	0	133	134,032

FBV900

Table 3-36: **Test Results for Device Type XC7K325T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
THB	2	0	154	154,000

FBV676

Table 3-37: **Test Results for Device Type XCKU040**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	6	0	165	205,752

FBV484

Table 3-38: **Test Results for Device Types XC7A200T and XC7Z030**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HTS	1	0	45	45,000
TC	2	0	154	154,000
TH	3	0	231	231,000
THB	2	0	154	154,000

FFG323, FFG324 and FFG363

Table 3-39: **Test Results for Device Type XC5VLX50**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
HTS	3	0	75	150,000
TC	3	0	75	150,000

FFG665, FFG668, FFG672, and FFG676

Table 3-40: **Test Results for Device Type XC7K325T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	1	0	45	45,000

FFG1136, FFG1148, FFG1152, FFG1153, FFG1154, FFG1155, FFG1156, FFG1157, and FFG1158

Table 3-41: **Test Results for Device Types XC2VP40, XC5VLX110T, XC5VLX155T, XC6VLX130T, XC6VLX240T, and XC7A200T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	15	0	671	671,000
HTS	8	0	359	359,000
Temperature humidity 85°C, 85% RH with bias	19	1(1)	755	729,000

Notes:

1. One failure after THB was a random defect caused by foreign material adhering to the substrate. A corrective action is in place.

FFG1513 and FFG1517

Table 3-42: **Test Results for Device Type XC4VFX140**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	3	0	74	148,000
HTS	3	0	75	150,000

FFG1696, FFG1704, FFG1738, FFG1759, FFG1738 and FFG1760

Table 3-43: **Test Results for Device Type XC5VFX200T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	4	0	99	185,500
HTS	4	0	100	187,500

FFG1923, FFG1924, FFG1925, FFG1926, FFG1927, FFG1928, FFG1929, and FFG1930

Table 3-44: **Test Results for Device Type XC7VX980T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HTS	3	0	75	90,000
Temperature cycling –55 to +125°C	3	0	75	90,000

FFV900 and FFV901

Table 3-45: **Test Results for Device Types XCZU9EG and XCZU15EG**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	5	0	224	300,300

FFV1136, FFV1148, FFV1152, FFV1153, FFV1154, FFV1156, FFV1156, FFV1157, and FFV1158

Table 3-46: **Test Results for Device Types XC7V690T, XCKU040, XCKU15P, XCZU9EG, XCZU28DR, and XCZU7EV**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	20	0	718	987,228
Temperature humidity 85°C, 85% RH with bias	6	0	268	270,288
HTS	10	0	448	537,000

FFV1517, FFV1924, and FFV2104

Table 3-47: **Test Results for Device Types XCKU095, XCVU095, and XCVU3P**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
TCB	7	0	311	431,500

FGG324 and FGG456

Table 3-48: **Test Results for Device Type XC3S400**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	4	0	180	180,000
Temperature humidity 85°C, 85% RH with bias	3	0	135	135,000
HTS	2	0	89	89,000

FGG484

Table 3-49: **Test Results for Device Types XC6SLX45T, XC7S100, and XC7A100T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	14	0	578	838,100
HAST	11	0	494	189,552
HTS	7	0	313	447,000

FGG676

Table 3-50: **Test Results for Device Types XC3S1400A, XC3S1400AN, and XC7A100T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	3	0	135	135,000
HTS	3	0	135	135,000

FGG1156

Table 3-51: **Test Results for Device Type XC7A200T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	1	0	45	45,000
HTS	1	0	45	45,000

FHG1761, FHG2104

Table 3-52: **Test Results for Device Type XC7V2000T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	7	0	190	286,500
Temperature humidity 85°C, 85% RH with bias	4	0	107	107,042
HTS	4	0	120	195,000

FLV1517, FLV1924, and FLV2104

Table 3-53: **Test Results for Device Types XCKU115, XCVU125, and XCVU7P**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature humidity 85°C, 85% RH with bias	5	0	120	121,701
Temperature humidity 85°C, 85% RH	1	0	44	44,000
HTS	15	0	451	747,865
Temperature cycling –40 to +125°C	24	0	573	756,945

FLG1925, FLG1926, FLG1928, FLG1932, FLG2104, FLG2377, and FLG2892

Table 3-54: **Test Results for Device Types XCVU440, XCVU190, XCVU160, and XCVU9P**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –40 to +125°C	19	0	477	776,622
Temperature humidity 85°C, 85% RH with bias	2	0	67	67,120
HTS	5	0	141	328,000

FSG48

Table 3-55: **Test Results for Device Types XCF08P, XCF16P, and XCF32P**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –65°C to +150°C	1	0	45	75,060
Temperature humidity 85°C, 85% RH with bias	1	0	45	75,060
PP	1	0	45	4,320
HTS	1	0	45	75,060

FSG2104

Table 3-56: **Test Results for Device Type XCVU9P**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	11	0	135	197,258
HTS	10	0	135	255,181

FTG196

Table 3-57: **Test Results for Device Type XC7S50**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	1	0	82	83,066
Temperature humidity 85°C, 85% RH with bias	1	0	82	82,082
TH	1	0	82	82,000
HTS	1	0	50	50,000

FTG256

Table 3-58: **Test Results for Device Types XC3S1200E and XC3S200A**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	7	0	300	420,000
Temperature humidity 85°C, 85% RH with bias	4	0	180	337,500
HAST	4	0	180	47,520
HTS	7	0	315	405,000

SOG20

Table 3-59: **Test Results for Device Type XC18V01**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	1	0	45	45,000
HTS	1	0	45	45,000

TQG144

Table 3-60: **Test Results for Device Types XC3S50AN and XC9572XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	3	0	81	121,500
HASTU	3	0	81	21,384
HTS	3	0	81	162,000

VQG44, VQG64, and VQG100

Table 3-61: **Test Results for Device Types XC9572XL, XC2C128, XC2C64A, XC3S100E, and XC3S250E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	15	0	645	948,000
Temperature humidity 85°C, 85% RH with bias	15	0	673	986,000
HASTU	2	0	90	23,760
HTS	15	0	672	984,000

Board-Level Reliability Tests, SnPb Eutectic

FG676, FG680, FG900, FG1156, BF957, FF672, FF896, FF1152, FF1704, SF363, and CF1144

Table 3-62: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FG676	27 x 27	676	1.00	0.60	0.46	SMD	17.8 x 17.8 x 0.3	0.56 thick, 4-layer
FG680	40 x 40	680	1.00	0.60	0.46	SMD	20.3 x 20.3 x 0.3	0.98 thick, 3-layer
FG900	31 x 31	900	1.00	0.60	0.46	SMD	17.0 x 17.0 x 0.3	0.56 thick, 4-layer
FG1156	35 x 35	1,156	1.00	0.60	0.46	SMD	23 x 21 x 0.3	0.56 thick, 4-layer
BF957	40 x 40	957	1.27	0.75	0.61	SMD	22 x 20 x 0.7	1.152 thick, 6-layer
FF672	27 x 27	672	1.00	0.60	0.53	SMD	12 x 10 x 0.7	1.152 thick, 6-layer
FF896	31 x 31	896	1.00	0.60	0.53	SMD	10 x 10 x 0.7	1.152 thick, 6-layer

Table 3-62: **Package Details (All Dimensions in mm) *(Cont'd)***

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FF1152	35 x 35	1,152	1.00	0.60	0.53	SMD	22 x 20 x 0.7	1.152 thick, 6-layer
FF1704	42.5 x 42.5	1,704	1.00	0.60	0.53	SMD	26 x 22 x 0.7	1.152 thick, 6-layer
SF363	17 x 17	363	0.8	0.50	0.40	SMD	10 x 10 x 0.3	0.60 thick, 4-layer
CF1144	35 x 35	1,144	1.00	0.52	0.80	SMD	22 x 20 x 0.7	1.59 thick, 10-layer

Mother Board Design and Assembly Details

- 8-layer, FR-4, 220 x 140 x 2.3622 mm size, HASL finish
- 0.5 mm pad diameter/0.65 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power/GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.1524 mm laser cut stencil, 0.50 mm aperture, alpha metals WS609 paste

Test Condition

- 0°C – 100°C, 10-minutes dwell, 5-minute ramps, 2 cycles/hour

Failure Criteria

- Continuous scanning of daisy chain nets (every 2 minutes)
- **OPEN**: Resistance of net > threshold resistance (300Ω)
- **FAIL**: At least 2 opens within one cycle, log 15 failures for each net

Table 3-63: **Summary of Test Results**

Package	Cycles Completed	# Tested	# Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FG676	7,027	30	30	4,686	6,012
FG680	4,000	30	0	NA	NA
FG900	7,027	28	28	4,405	5,344
FG1156	5,000	32	25	2,786	4,892
BF957	4,145	35	35	1,958	3,662
FF672	5,840	30	30	3,764	4,881
FF896	7,027	12	10	5,607	6,783
FF1152	4,158	30	30	2,668	3,822
SF363 (Lot 1)	2,370	24	21	1,642	2,048

Table 3-63: **Summary of Test Results *(Cont'd)***

Package	Cycles Completed	# Tested	# Failed	First Failure (Cycle)	Characteristic Life (Cycle)
SF363 (Lot 2)	2,288	24	24	1,555	1,999
FF1704	4,150	35	35	3,003	3,389
CF1144	5,000	21	0	NA	NA

Weibull Plots

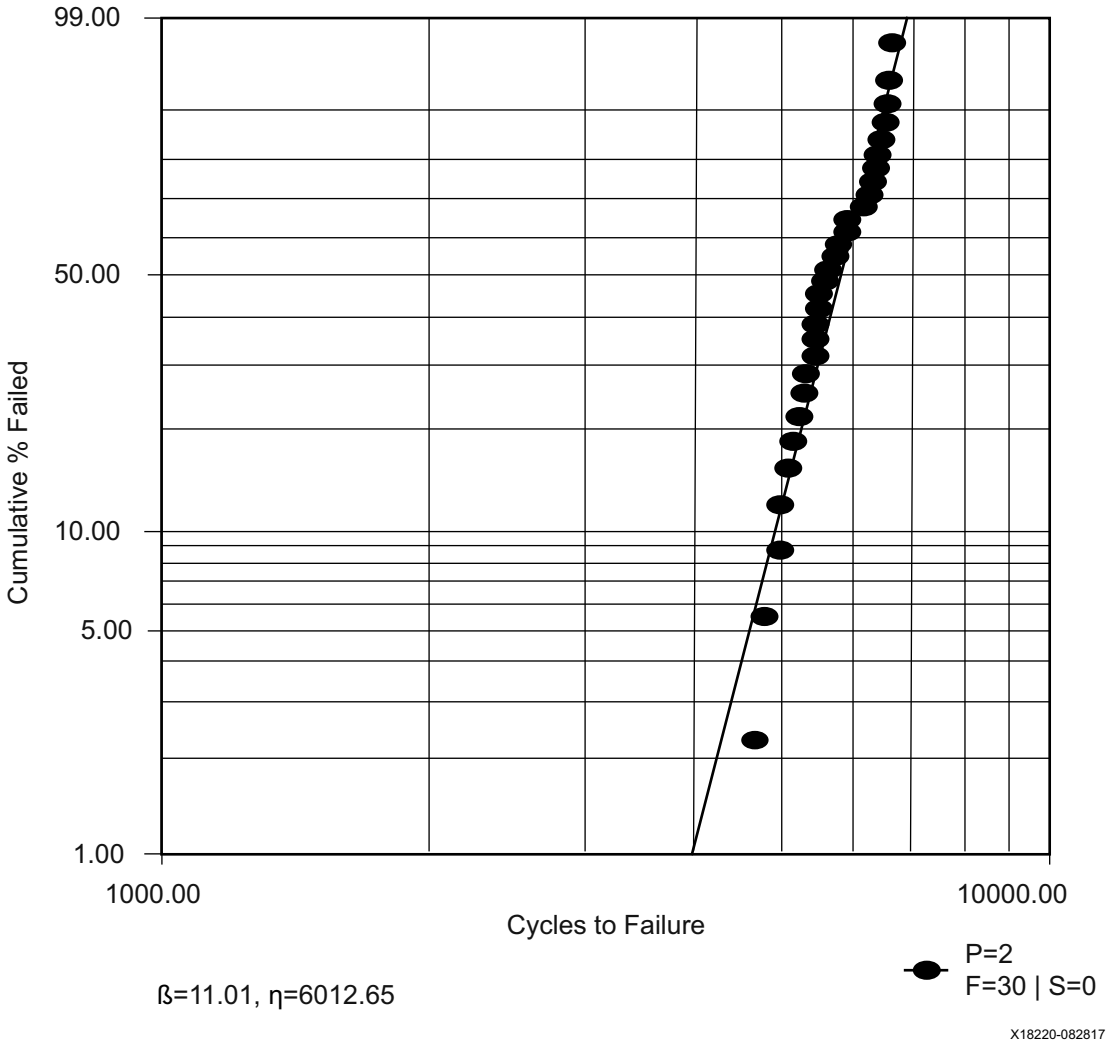

Figure 3-1: **Cycles to Failure in the Second-Level Reliability Tests for FG676**

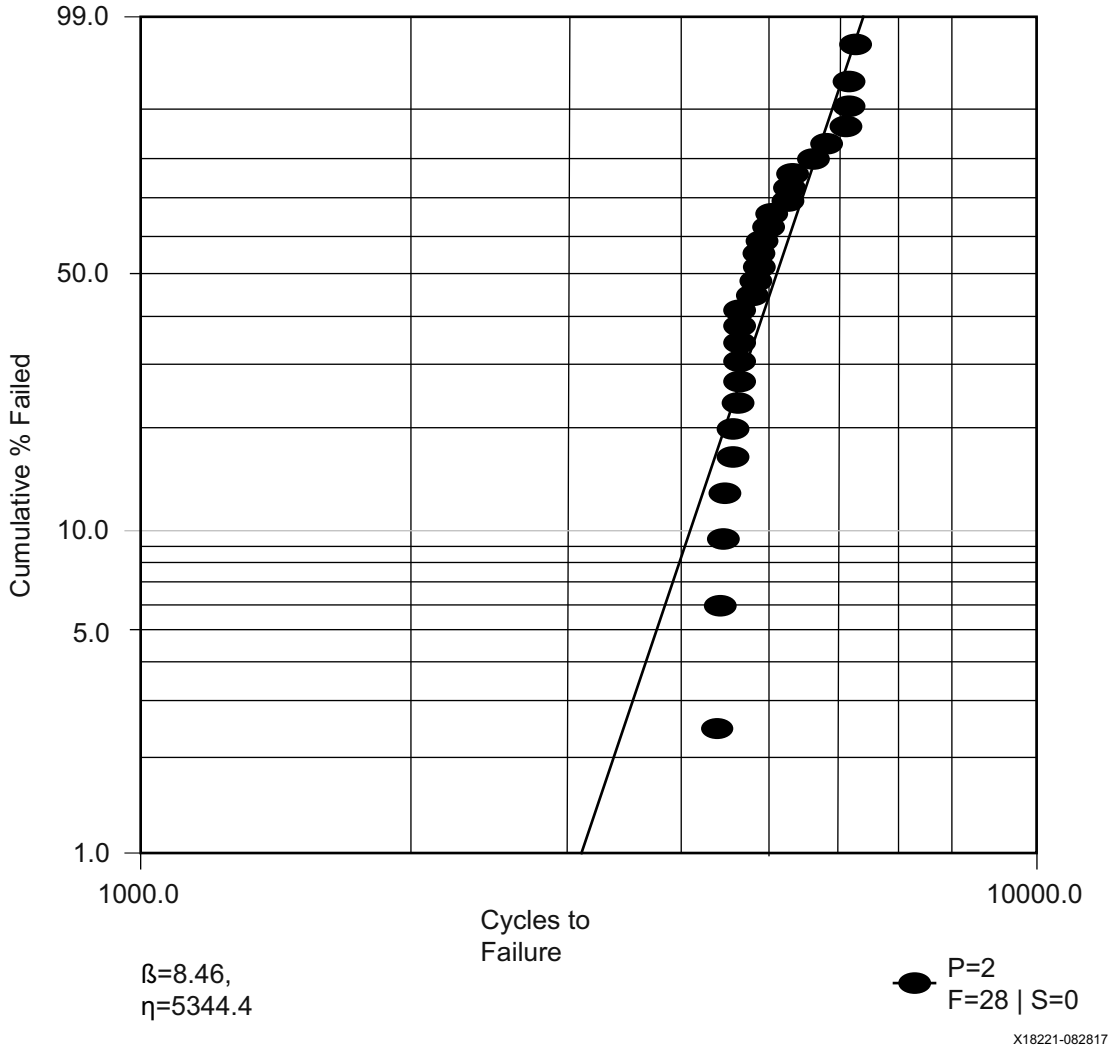

Figure 3-2: **Cycles to Failure in the Second-Level Reliability Tests for FG900**

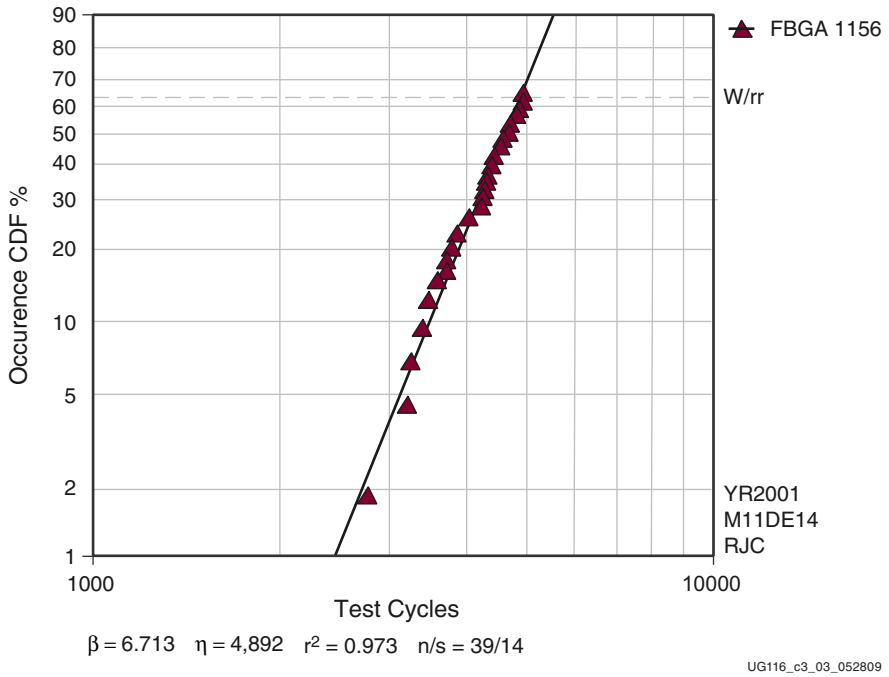

Figure 3-3: **Cycles to Failure in the Second-Level Reliability Tests for FG1156**

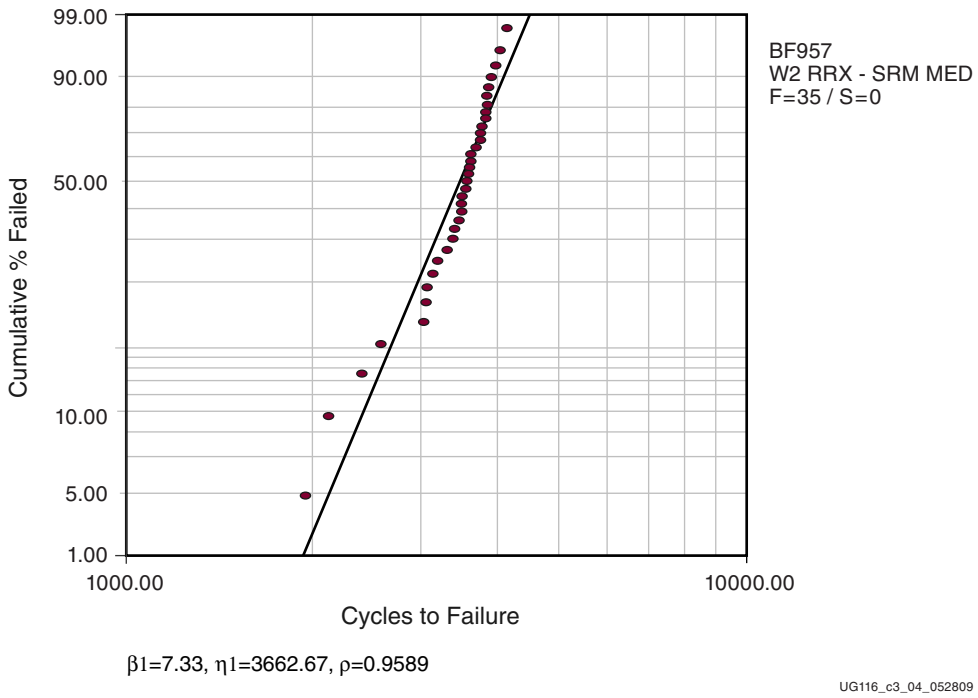

Figure 3-4: **Cycles to Failure in the Second-Level Reliability Tests for BF957**

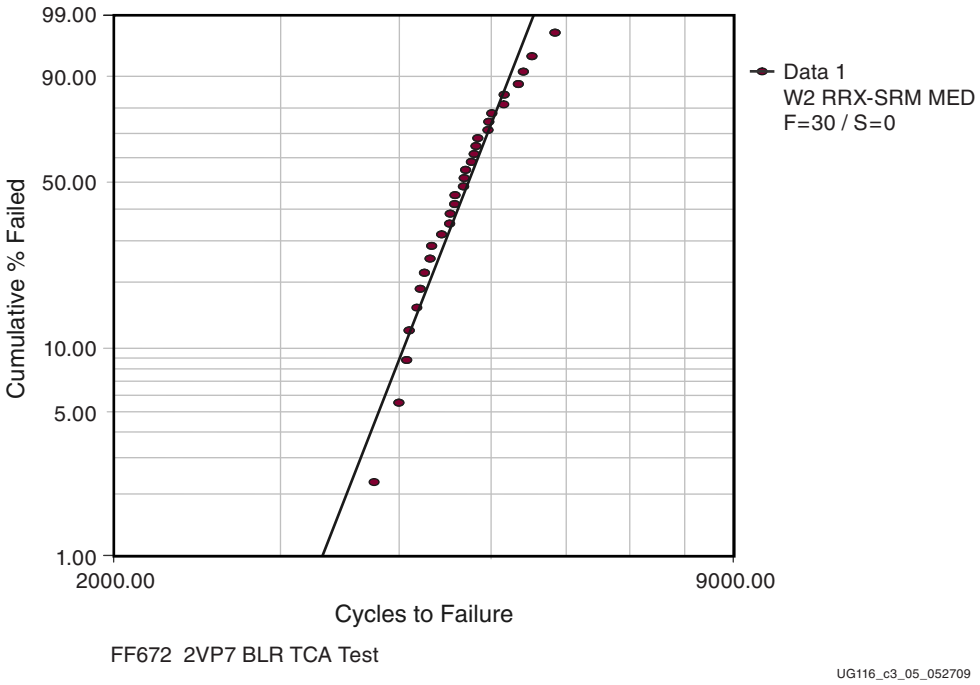

Figure 3-5: **Cycles to Failure in the Second-Level Reliability Tests for FF672**

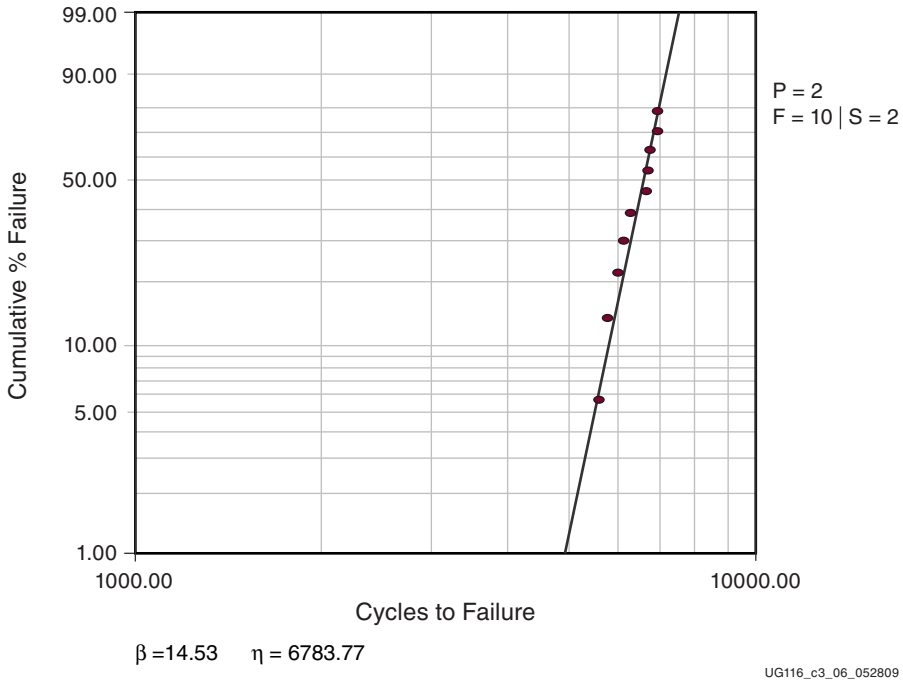

Figure 3-6: **Cycles to Failure in the Second-Level Reliability Tests for FF896**

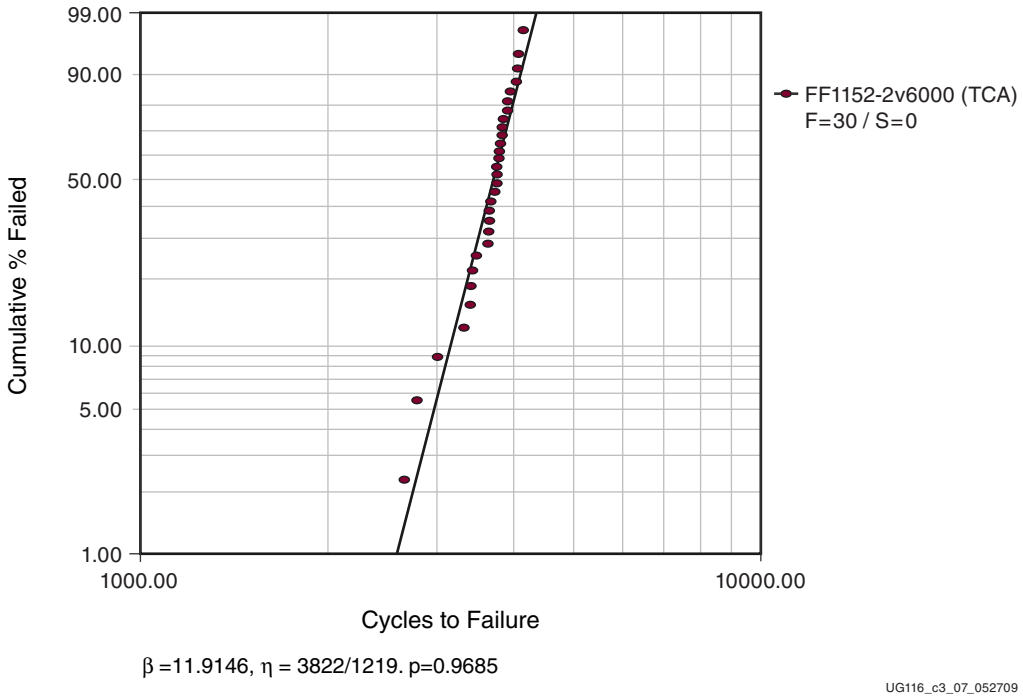

Figure 3-7: **Cycles to Failure in the Second-Level Reliability Tests for FF1152**

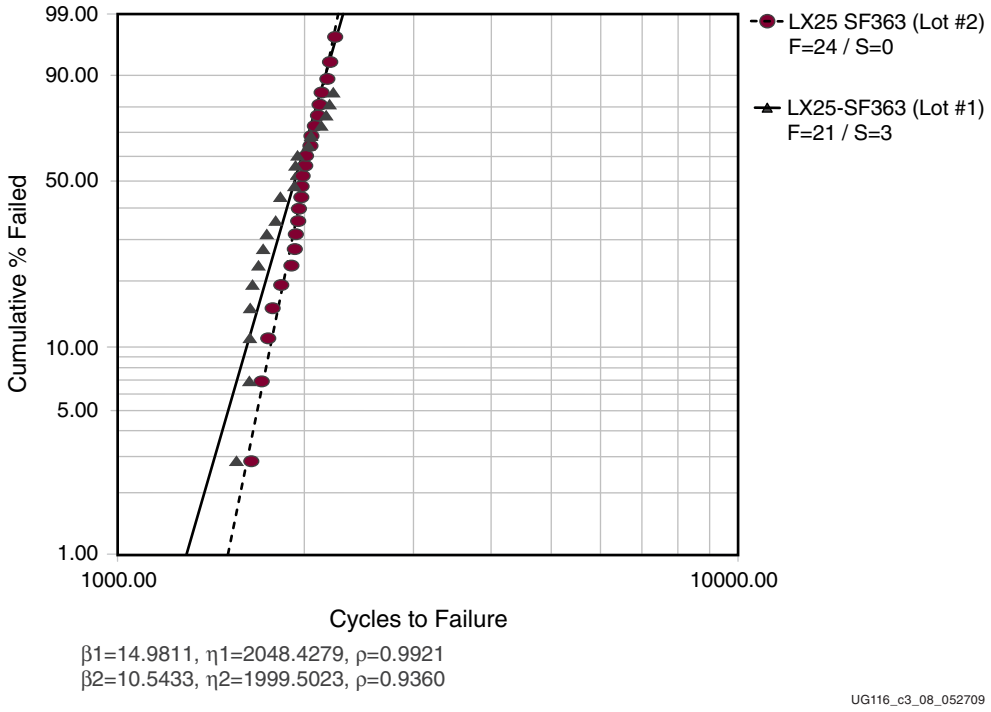

Figure 3-8: **Cycles to Failure in the Second-Level Reliability Tests for SF363**

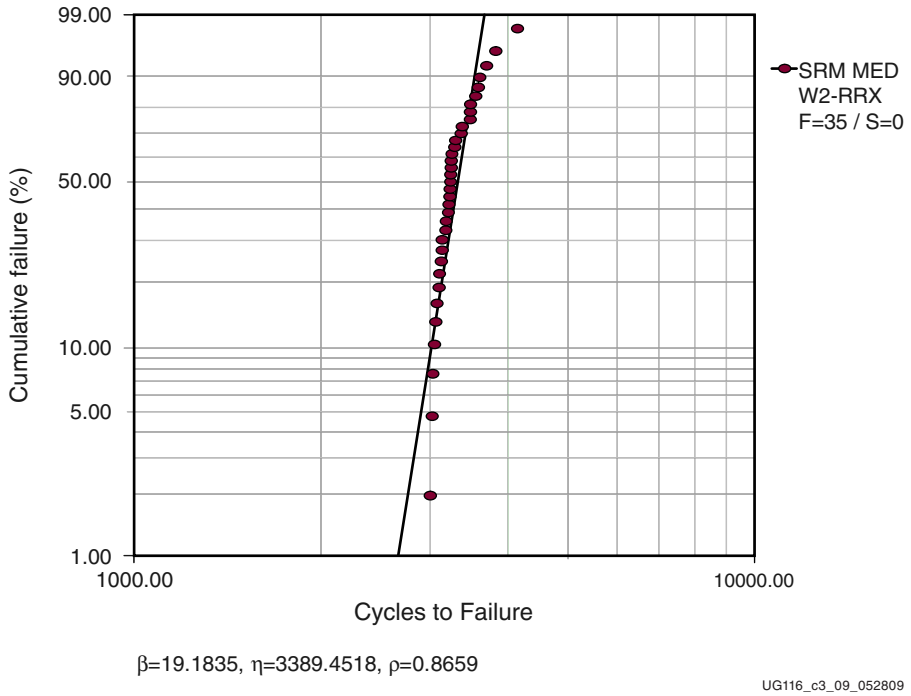

Figure 3-9: **Cycles to Failure in the Second-Level Reliability Tests for FF1704**

Board-Level Reliability Tests, Pb-Free BGA

FGG676, FFG1152, FBVA900, FFVB2104, FLVA1924, SFVA784, and SBVA784

Table 3-64: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FGG676	27 x 27	676	1.00	0.60	0.46	SMD	17.8 x 17.8 x 0.3	0.56 thick, 4-layer
FFG1704	42.5 x 42.5	1,704	1.00	0.60	0.53	SMD	23 x 23	1.152 thick, 6-layer
FFG1152	35 x 35	1,152	1.00	0.60	0.53	SMD	22 x 20 x 0.7	1.152 thick, 6-layer
FBVA900	31 x 31	900	1.00	0.60	0.53	SMD	16.30 x 11.36	1.24 thick, 10-layer
FFVB2104	47.5 x 47.5	2104	1.00	0.6	0.53	SMD	18 x 22.5	1.42 thick, 14-layer
FLVA1924	45 x 45	1924	1.00	0.6	0.53	SMD	25 x 31	1.33 thick, 12-layer

Mother Board Design and Assembly Details

- 8-layer, FR-4, 220 x 140 x 2.3622 mm size, OSP finish
- 0.5 mm pad diameter/0.65 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.1524 mm laser cut stencil, 0.50 mm aperture, alpha metals WS609 paste

Test Condition

- FGG676: 0°C – 100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate
- FFG1152: 0°C – 100°C, 10-minute dwells, 5-minute ramps, 2 cycles/hour

Failure Criteria

- Continuous scanning of daisy chain nets (every 2 minutes)
- **OPEN**: Resistance of net > threshold resistance (300Ω)
- **FAIL**: At least 2 opens within one cycle, log 15 failures for each net

Table 3-65: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FGG676	7,027	35	27	4,390	5,974
FFG1704	5,000	32	0	NA	NA
FFG1152	4,640	28	26	3,186	4,121
FBVA900	8,737	32	28	7,181	8,260
FFVB2104	8,568	32	14	5,205	9,351
FLVA1924	4,605	32	25	2,759	4,222

Weibull Plots

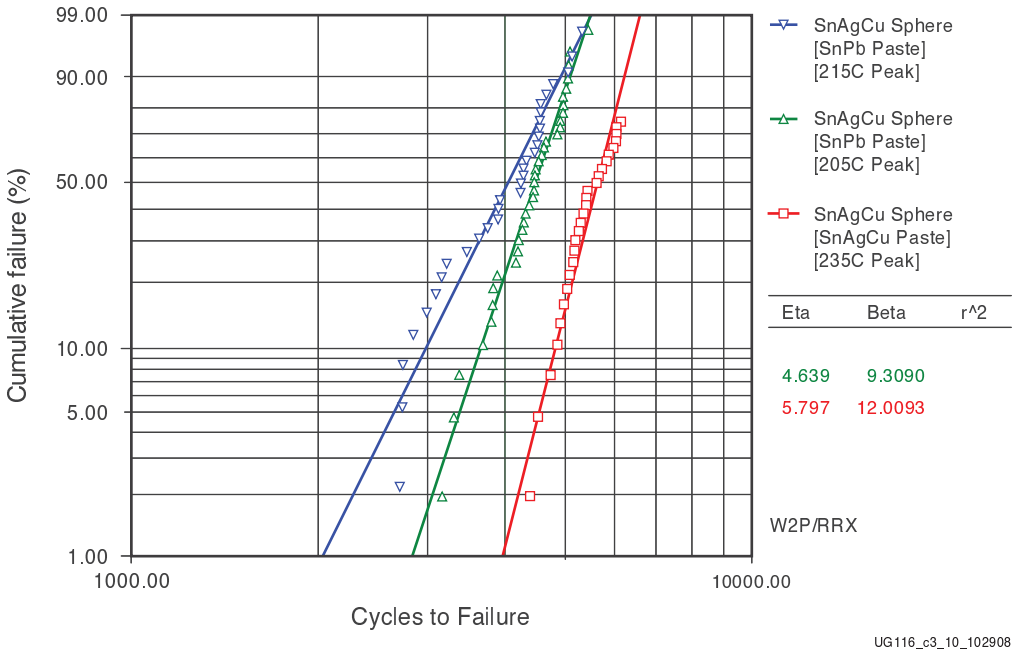

Figure 3-10: **Cycles to Failure in the Second-Level Reliability Tests for FGG676**

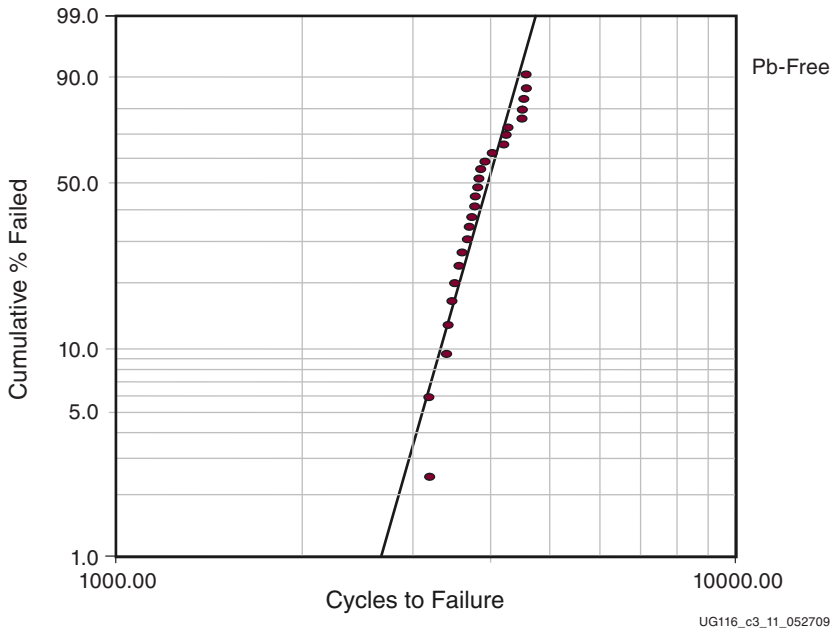

Figure 3-11: **Cycles to Failure in the Second-Level Reliability Tests for FFG1152**

FBG900

Table 3-66: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/Column Size	Pad Opening	Pad Type	Die Size	Substrate
FBG900	31 X 31	900	1.00	0.60	0.53	SMD	12.93 x 16.91	0.95 thick, 8-layer

Mother Board Design and Assembly Details

- 8-layer, FR-4, 220 x 140 x 2.36 mm size, ENIG finish
- 0.45 mm pad diameter/0.55 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.127 mm laser cut stencil, 0.50 mm aperture, alpha metals WS820 paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets with event detection
- **FAIL**: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 3-67: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FBG900	10,085	32	18	5,674	9,148

Weibull Plots

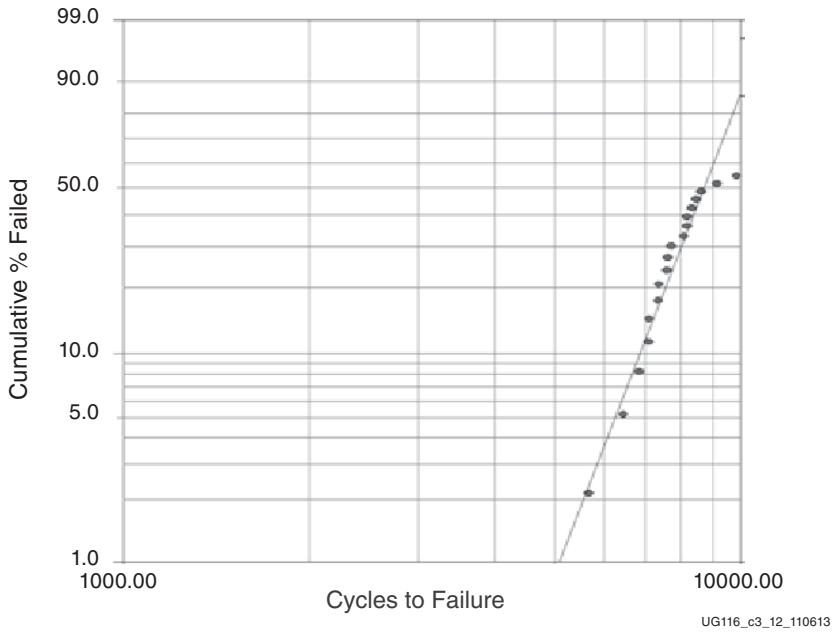

Figure 3-12: **Cycles to Failure in the Second-Level Reliability Tests for FBG900**

SBG484

Table 3-68: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/Column Size	Pad Opening	Pad Type	Die Size	Substrate
SBG484	19 X 19	484	0.8	0.50	0.40	SMD	10.82 x 12.04	0.98 thick, 8-layer

Mother Board Design and Assembly Details

- 8-layer, FR-4, 220 x 140 x 2.36 mm size, ENIG finish
- 0.33 mm pad diameter/0.50 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.

Test Condition

- 0°C – 100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets with event detector

- **FAIL**: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 3-69: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
SBG484	6,827	32	23	4,499	6,608

Weibull Plots

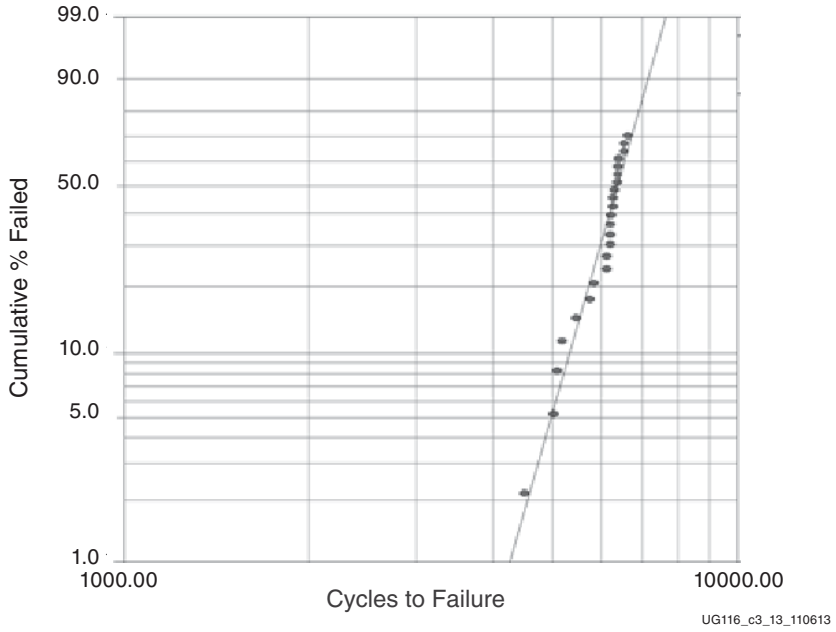

Figure 3-13: **Cycles to Failure in the Second-Level Reliability Tests for SBG484**

FFG1928

Table 3-70: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/Column Size	Pad Opening	Pad Type	Die Size	Substrate
FFG1928	45 X 45	1924	1.00	0.60	0.53	SMD	23.85 x 21.65	1.33 thick, 12-layer

Mother Board Design and Assembly Details

- 16-layer, FR-4, 220 x 140 x 2.4 mm size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.

- 0.127 mm laser cut stencil, 0.50 mm aperture, alpha metals WS820 paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets with event detector
- **FAIL**: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 3-71: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FFG1928	9,520	32	22	6,861	9,313

Weibull Plots

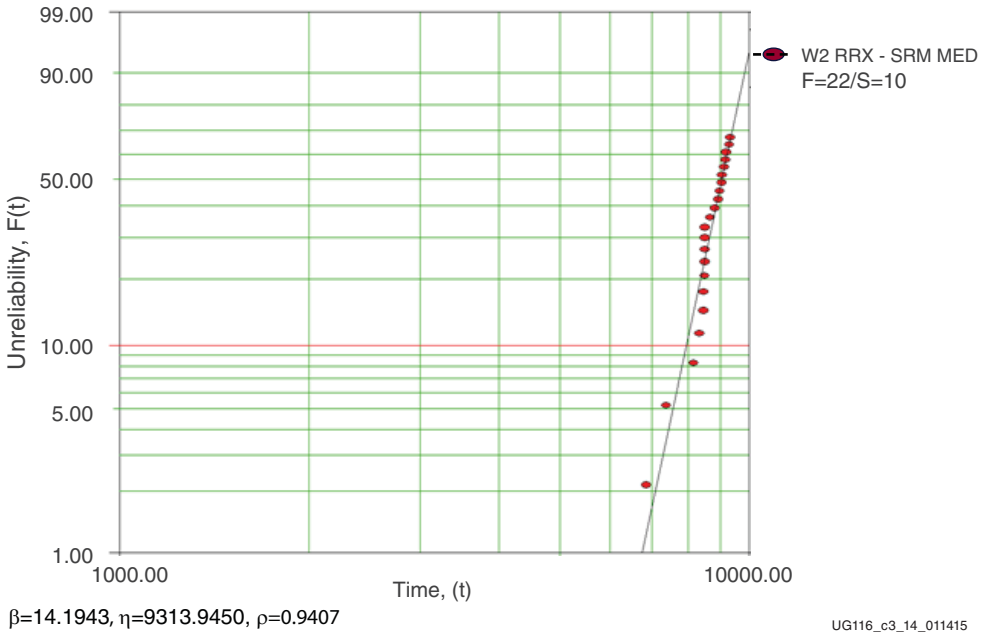

Figure 3-14: **Cycles to Failure in the Second-Level Reliability Tests for FFG1928**

FLG1925

Table 3-72: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/Column Size	Pad Opening	Pad Type	Die Size	Substrate
FLG1925	45 X 45	1924	1.00	0.635	0.53	SMD	23.85 x 21.65	1.42 thick, 12-layer

Mother Board Design and Assembly Details

- 16-layer, FR-4, 220 x 140 x 3.2 size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.127 mm laser cut stencil, 0.50 mm aperture, alpha metals WS820 paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets with event detector
- **FAIL**: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 3-73: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FLG1925	6,043	32	27	3,789	5,548

Weibull Plots

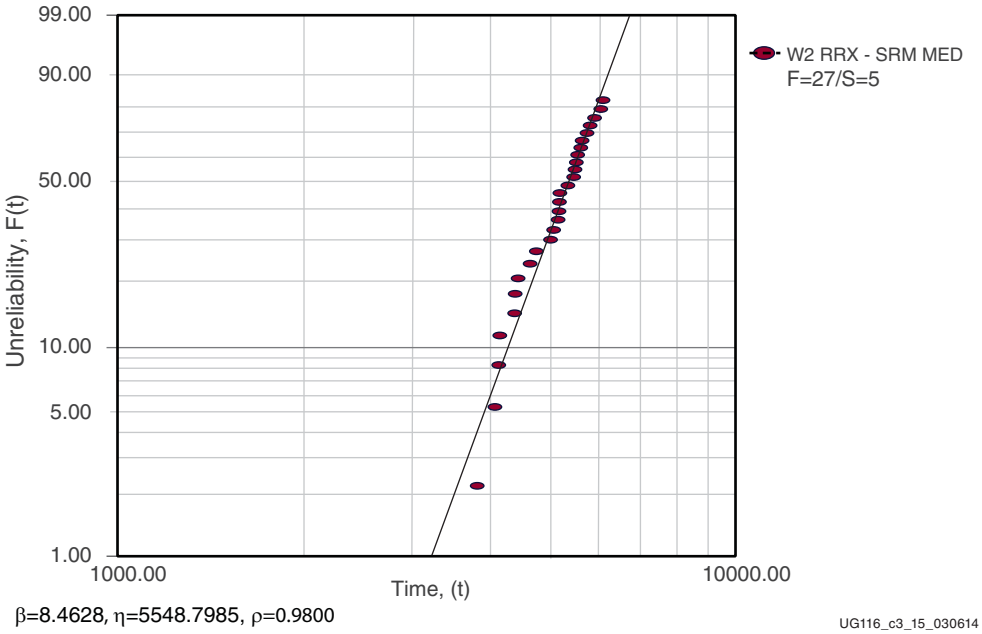

Figure 3-15: **Cycles to Failure in the Second-Level Reliability Tests for FLG1925**

FFV1928

Table 3-74: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/Column Size	Pad Opening	Pad Type	Die Size	Substrate
FFV1928	45 X 45	1924	1.00	0.60	0.53	SMD	23.85 x 21.65	1.33 thick, 12-layer

Mother Board Design and Assembly Details

- 16-layer, Megtron 6, 220 x 140 x 2.4 mm size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.127 mm laser cut stencil, 0.50 mm aperture, alpha metals WS820 paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets with event detector

- **FAIL**: Resistance of net > threshold resistance (500Ω) and lasting longer than 1 µs, followed by >9 events within 10% of the cycles to initial failure.

Table 3-75: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FFV1928	9,490	32	25	5,635	9,275

Weibull Plots

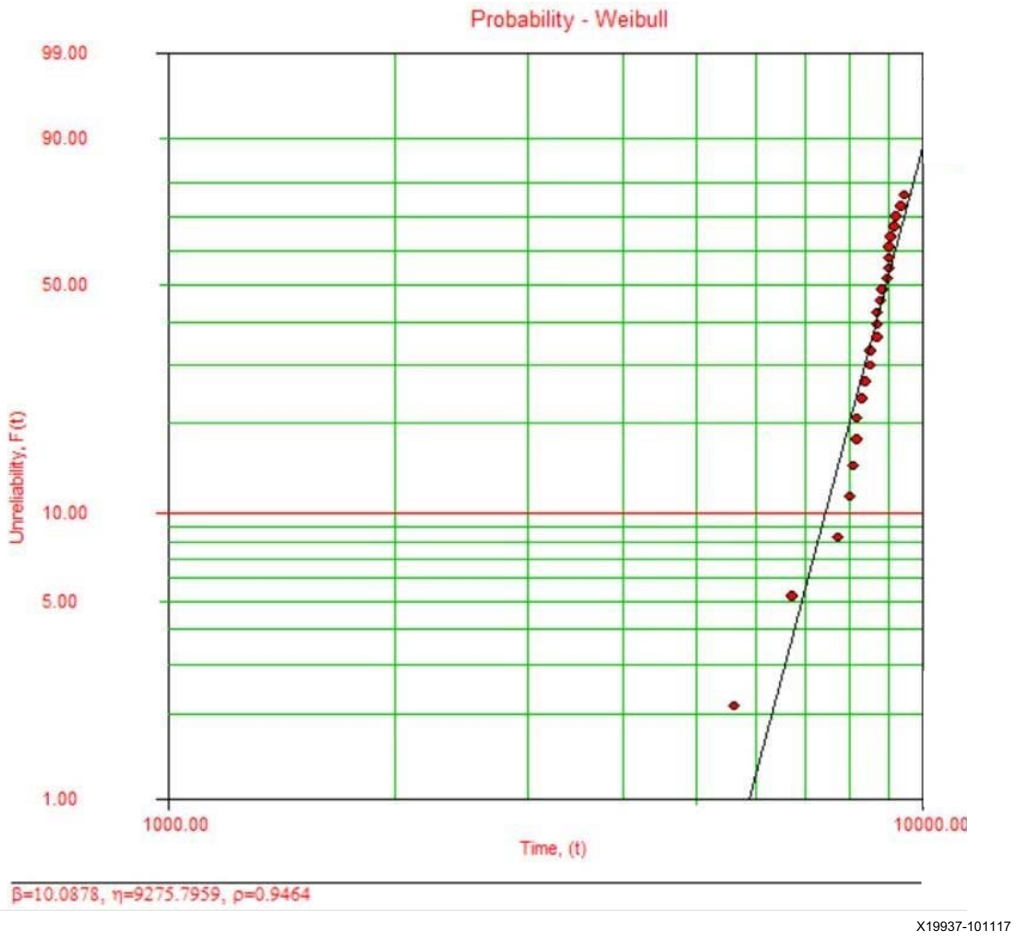

Figure 3-16: **Cycles to Failure in the Second-Level Reliability Tests for FFV1928**

FBVA900

Table 3-76: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FBVA900	31 X 31	900	1.00	0.60	0.53	SMD	16.30 x 11.36 x 0.762	1.24 thick, 10-layer

Mother Board Design and Assembly Details

- 16-layer, Megtron-6, 290 x 140 x 3.2 mm size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: 16 layer with simulated power, ground (70% metal), and signal (40% metal) layer
- 0.127 mm laser cut stencil, 0.530 mm aperture, Indium 8.9HF paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets with event detection
- **FAIL**: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 3-77: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FBVA900	8737	32	28	7181	8260

Weibull Plots

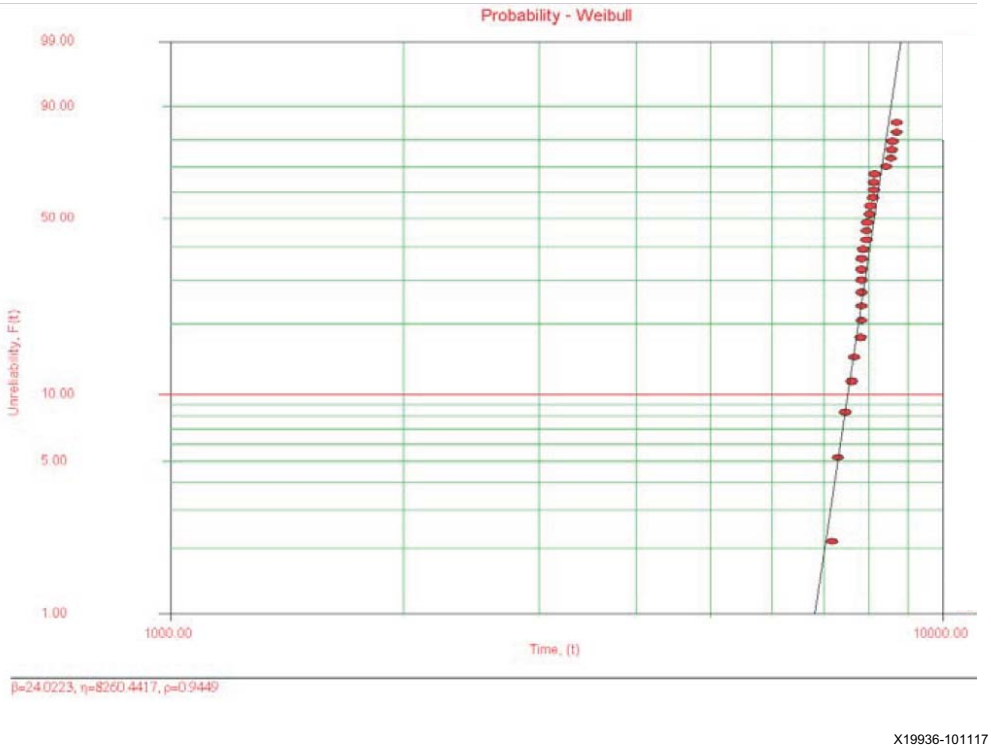

Figure 3-17: **Cycles to Failure in the Second-Level Reliability Tests for FBVA900**

FFVB2104

Table 3-78: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FFVB2104	47.5 x 47.5	2104	1.00	0.60	0.53	SMD	18 x 22.5 x 0.762	1.42 thick, 14-layer

Mother Board Design and Assembly Details

- 28-layer, Megtron-6, 290 x 140 x 3.4 mm size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: 28 layer with simulated power, ground (70% metal), and signal (40% metal) layer
- 0.127 mm laser cut stencil, 0.530 mm aperture, Indium 8.9HF paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets with event detector
- **FAIL**: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 3-79: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FFVB2104	8568	32	14	5205	9351

Weibull Plots

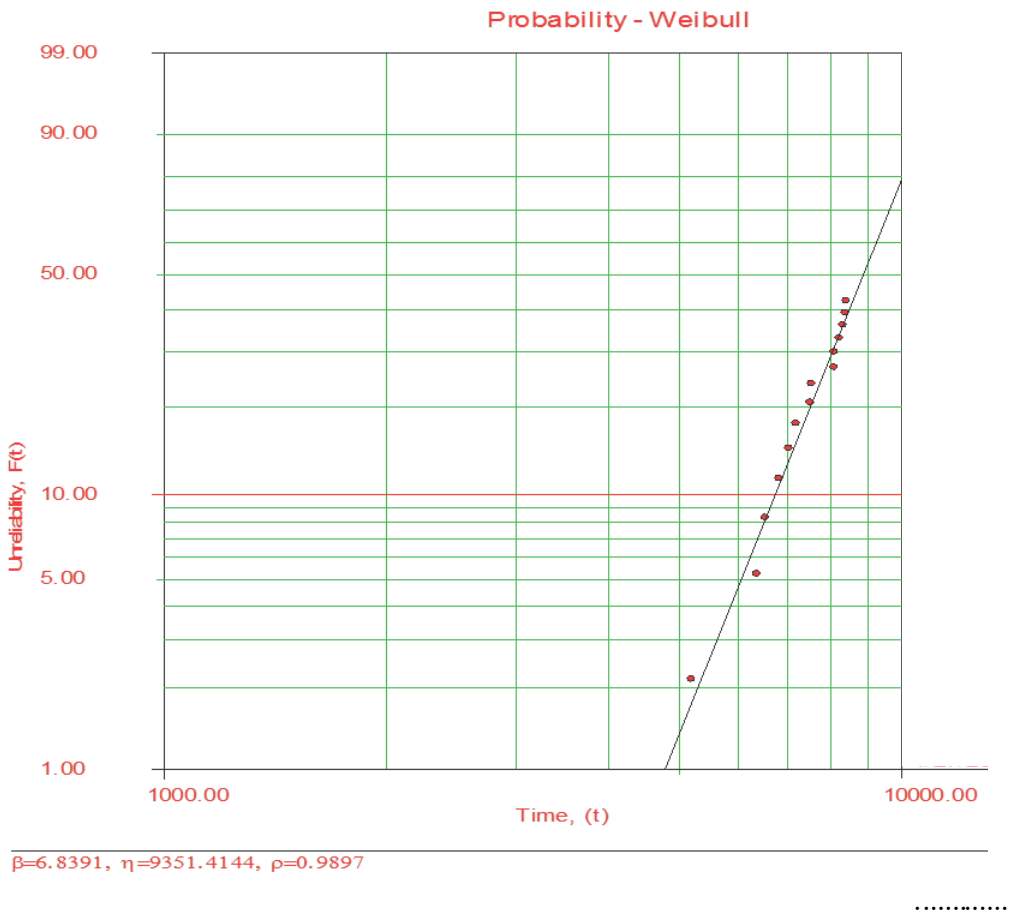

Figure 3-18: **Cycles to Failure in the Second-Level Reliability Tests for FFVB2104**

FLVA1924

Table 3-80: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FLVA1924	45 x 45	1924	1.00	0.60	0.53	SMD	14.4 x 23 x 0.10 (2 pcs) 25 x 31 x 0.50	2.00 thick, 18-layer

Mother Board Design and Assembly Details

- 28-layer, Megtron-6, 290 x 140 x 3.4 mm size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: 28 layer with simulated power, ground (70% metal), and signal (40% metal) layer
- 0.127 mm laser cut stencil, 0.530 mm aperture, Indium 8.9HF paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets with event detector
- **FAIL**: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 3-81: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FLVA1924	4605	32	25	2759	4222

Weibull Plots

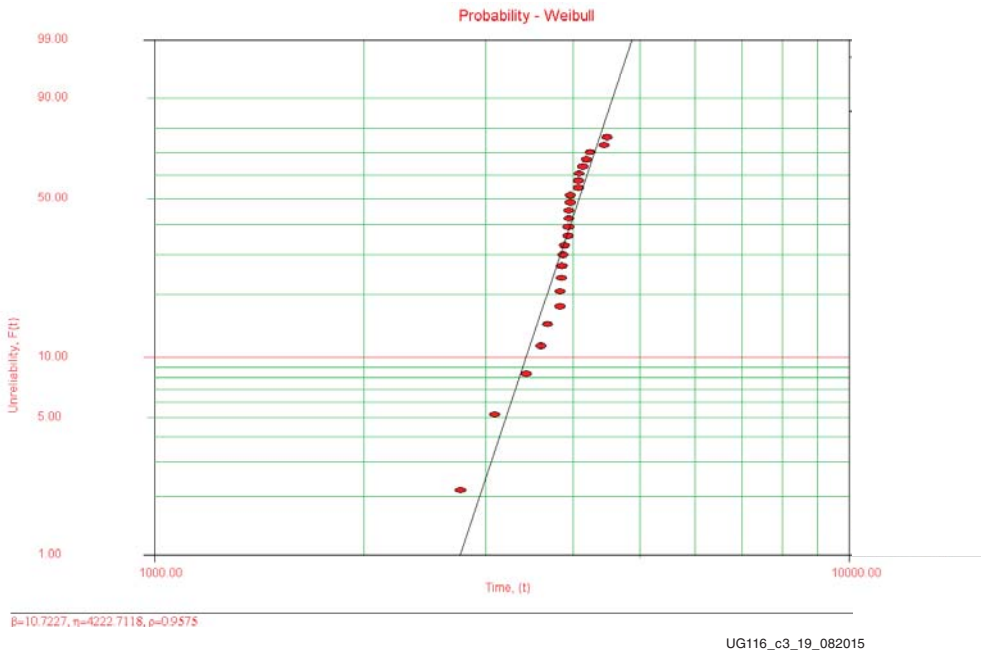

Figure 3-19: **Cycles to Failure in the Second-Level Reliability Tests for FLVA1924**

SFVA784 and SBVA784

Table 3-82: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Openi ng	Pad Type	Die Size	Substrate
SFVA784	23 x 23	784	0.8	0.50	0.40	SMD	16.3 x 11.36	1.33 thick, 12-layer
SBVA784	23 x 23	784	0.8	0.50	0.40	SMD	16.3 x 11.36	1.33 thick, 12-layer

Mother Board Design and Assembly Details

- 28-layer, Megtron-6, 305 x 140 x 3.4 mm size, OSP finish
- 0.40 mm pad diameter/0.50 mm solder mask opening (NSMD pads)
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.127 mm laser cut stencil, 0.40 mm aperture, SAC305 solder paste.

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets with event detector
- **FAIL**: Resistance of net > threshold resistance (500 Ω) and lasting greater than 1 µs, followed by >9 events within 10% of the cycles to initial failure.

Table 3-83: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
SFVA784	6800	32	25	5049	6540
SBVA784	6140	32	25	4120	5718

Weibull Plots

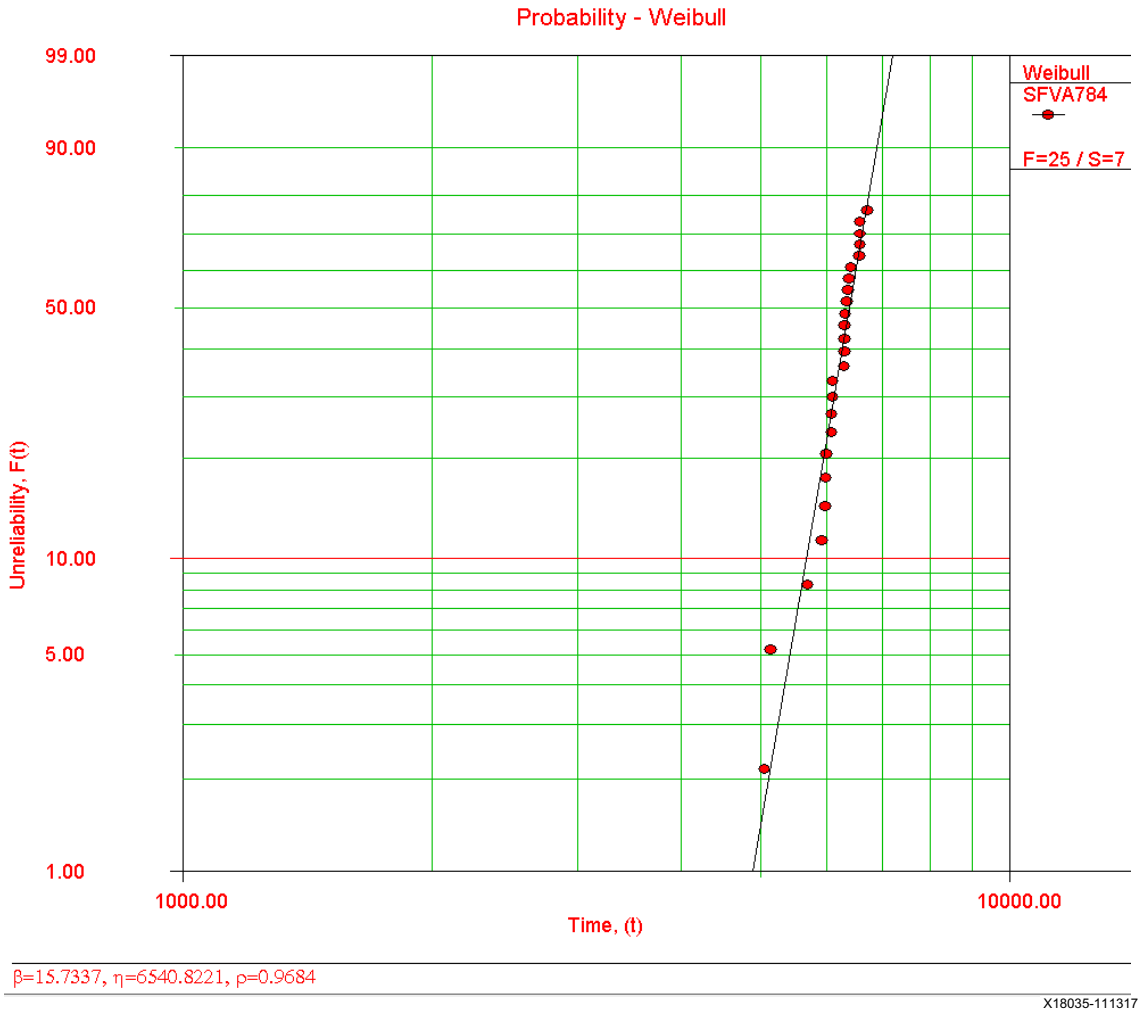

Figure 3-20: **Cycles to Failure in the Second-Level Reliability Tests for SFVA784**

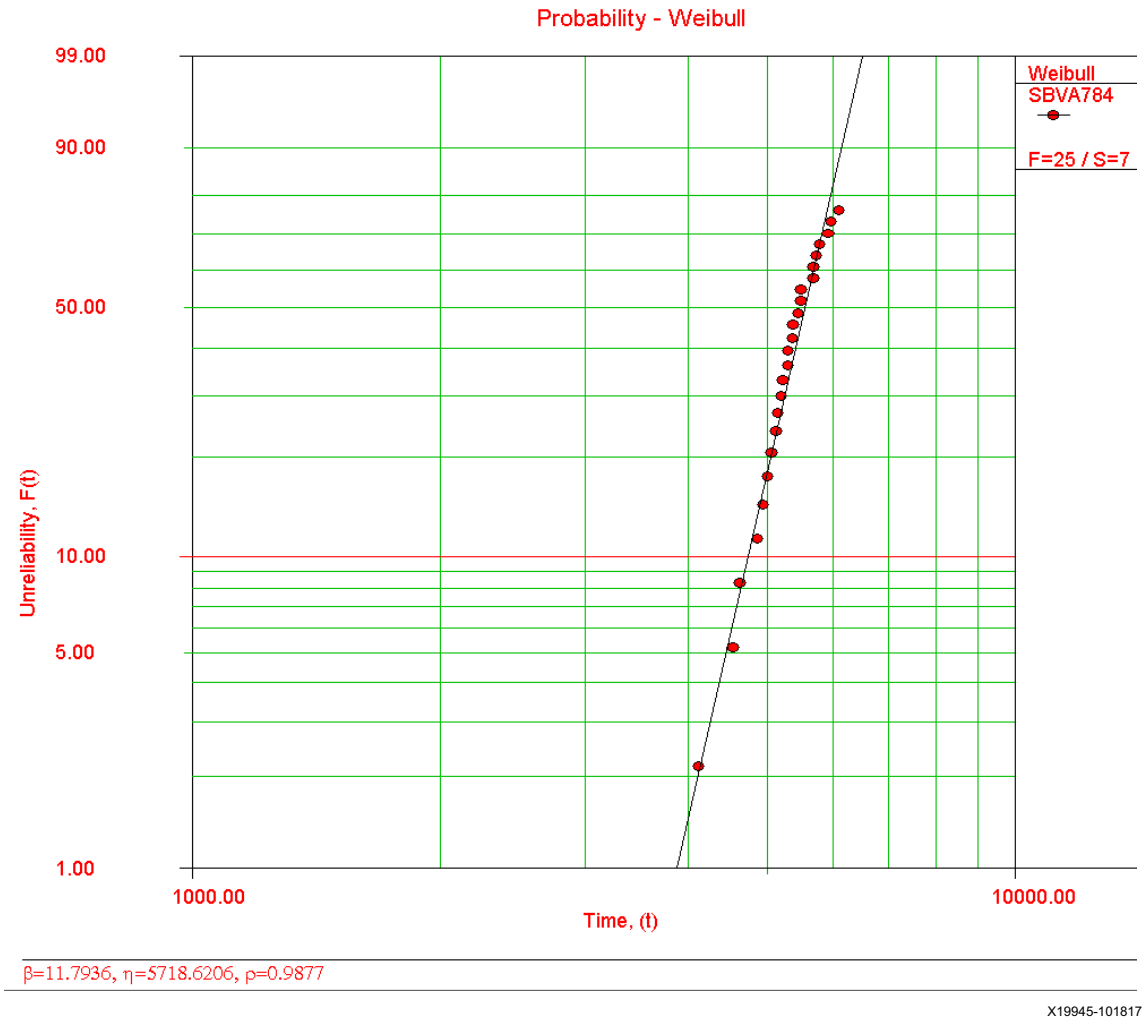

Figure 3-21: **Cycles to Failure in the Second-Level Reliability Tests for SBVA784**

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Appendix A

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter **`docnav`**.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

1. *Device Package User Guide* (UG112)
2. *Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits* (WP286)
3. *Virtex-4 FPGA Packaging and Pinout Specification* (UG075)
4. *Virtex-5 FPGA Packaging and Pinout Specification* (UG195)
5. *Virtex-6 FPGA Packaging and Pinout Specifications* (UG365)
6. *Spartan-6 FPGA Packaging and Pinouts Product Specification* (UG385)
7. *7 Series FPGAs Packaging and Pinout Product Specification* (UG475)
8. *Zynq-7000 SoC Packaging and Pinout Product Specification* (UG865)
9. *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification* (UG575)
10. *Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide* (UG1075)

Training Resources

1. Designing FPGAs Using the Vivado Design Suite 1 Training Course
2. Vivado Design Suite QuickTake Video Tutorials

Please Read: Important Legal Notices