Fabrication process development for superconducting VLSI circuits: minimizing plasma charging damage

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Abstract. In order to realize the potential of superconducting digital integrated circuits and make them competitive with semiconductor ICs, their integration scale must be increased from a current level of ~ 10^4 Josephson junctions (JJs) per chip to a VLSI level, and the maximum clock frequency, currently ~ 30 GHz, must also be increased above 50 GHz. It is shown that the main factor preventing successful fabrication of VLSI superconducting digital circuits is variations of the Josephson critical currents in logic cells caused by plasma-induced charging damage (electric stress) to the ultra thin oxide tunnel barrier of JJs. The results are presented for Nb/Al/AlO_x/Nb tunnel junctions fabricated on 150-mm wafers by an 11-level process for superconducting integrated circuits. It is shown that, as a result of charging in processing plasmas, the critical current I_c of JJs becomes dependent on the way the junctions are connected to the circuit ground plane and interconnected with other circuit elements. For instance, the I_c of the grounded junctions may abnormally increase with respect to the I_c of the floating junctions. Depending on the processing plasma parameters, plasma charging can damage all junctions in a circuit or only some specific junctions, e.g., the smallest in size. In addition to the I_c enhancement, the damage also reveals itself as increased subgap conduction in tunnel junctions and as an enhanced spread of the critical currents of the same-size junctions, a result of the statistical nature of the oxide barrier breakdown under electric stress. The plasma damage model is proposed and the most damaging plasma processing fabrication steps are discussed as well as the ways of minimizing the plasma-induced charging damage to superconducting integrated circuits.

1. Introduction

Superconducting digital electronics based on the rapid single flux quantum (RSFQ) logic [1] offer great advantages in circuit speed and energy consumption in comparison with semiconductor digital electronics. In order to realize the potential of superconducting digital electronics, the integration scale of superconducting digital integrated circuits (superDICs) need to be increased from a current level of ~10^4 Josephson junctions (JJs) per chip to a very large scale integration (VLSI) level of >10^5 JJs per chip. This would allow for a dramatic increase in the functionality of superDICs that currently is relatively low. On the other hand the clock frequency should also be increased from a recently achieved level of f_{cl}~ 30 GHz [2] to 50 GHz and beyond. These advances coupled with the progress in chip packaging on commercial cryocoolers [3,4] may help to overcome an existing reluctance of commercial markets in taking on superconducting digital electronics.

In order to become competitive with semiconductor digital devices and survive in a profit-driven market, superconducting ICs must be manufactured with a high yield that is comparable with the yield acceptable in the semiconductor industry. They also need to be manufactured on large wafers, 150 mm and larger, using the same or similar processing tools that are acceptable and available in the semiconductor chip manufacturing. Any fabrication process, however, unavoidably introduces some randomness in the parameters of circuit elements such as critical currents of individual Josephson junctions I_{ci}, resistors R_i, inductors L_i, etc. RSFQ logic is known to be sensitive to deviations of the circuit elements parameters from the optimum values. The frequency of circuit operation as a function of parameters δI_{ci}, δL_i, δR_i, forms a surface encompassing a region into a multidimensional space that can be called the "margin space", where δI_{ci}, δL_i, δR_i are deviations of the circuit elements from the optimized design values. The maximum clock frequency corresponds to all the deviations being zero. If one of the circuit parameters falls outside the margin space the circuit becomes un-operational. As the circuit complexity grows so does the probability of random deviations, and the experimentally observed f_{cl} diminishes. For instance, it was noted in [2] that f_{cl} decreases with N almost as $1/N^{0.3}$, where N is the number of JJs in the circuit. It was also shown [5] that the main limiting factor is the deviations of the critical current of the smallest-size junctions in the circuit from the design value.

The fabrication process-induced variations of the critical current of Josephson junctions can be of two types. The first one is the random fluctuations which usually can be approximated by a normal distribution with the standard deviation σ_I. The second type is the systematic deviations of the critical currents of Josephson junctions that are circuit-dependent, depend on the way the junctions are interconnected, depend on the junction location on chip, and of the chip location on the wafer, etc. as was shown in our previous work [6,7]. For instance, we have found a systematic difference between the critical current of junctions connected to the circuit ground plane during the fabrication and of floating junctions. In this case, the grounded junctions always have larger critical currents than the floating ones with the deviation greatly exceeding σ_I. Other pattern-dependent effects on the critical current, e.g. metal wiring "antenna" effect, have also been observed [6,7]. If small random fluctuations of the circuit parameter just reduce the maximum clock frequency, large variations of I_{ci} drive the circuit out of the margin space and simply render it completely un-operational. It was proposed in [6,7] that the cause of these large, systematic, and circuit pattern-dependent deviations of the critical currents of Josephson junctions from the expected values is the plasma process-induced charging damage (electric stress) to the ultrathin tunnel barrier of the junctions that happens during specific steps of wafer processing. In this paper we present experimental evidence that the observed phenomena are indeed caused by plasma charging effects, discuss the possible damage mechanisms and the most damaging steps of circuit fabrication as well as ways of minimizing the charging-induced damage to superconducting integrated circuits.

2. Basics of plasma charging damage

Below we will give a brief description of how the plasma-induced charging damage to Josephson junctions in a superDIC may occur. It is in many respects similar to the well-known problem of the gate oxide damage in semiconductor integrated circuit manufacturing reviewed in detail in [8]. The main differences are in the direct tunnelling nature of the charge transport in Josephson junctions, the fabrication process and equipment, and in differences in the circuit design.

It is well know that any isolated object exposed to plasma will rapidly charge negatively due to much higher mobility of electrons than ions in the plasma. It will charge to a negative potential known as floating potential V_f at which a balance between the electron and ion fluxes to the object is reached so the net current is zero (all the potentials are measured with respect to the grounded plasma chamber walls). If the plasma potential V_p is nonuniform in space so becomes the V_f which tracks the plasma potential. It is this nonuniformity of the plasma potential across the wafer and tracking it floating potential that is one of the prime causes of charging damage to integrated circuits [9-11]. The V_p can be nonuniform because of a variety of reasons usually related the plasma processor design such as nonuniform plasma density or electron temperature due to nonuniform plasma excitation or gas

distribution, presence of magnetic field, proximity of the wafer to the chamber walls, etc. Others are related to the plasma processing procedures such as turning plasma on and off, moving wafer in and out of plasma which is often done in order to increase the uniformity of a deposition or etching process, moving objects above the wafer in plasma, e.g., opening shutters, etc.

2.1 Charging damage to superconducting integrated circuits: the model

Let us see how this basic physics can be applied to the superconducting integrated circuits. In superDICs all signals and bias currents are applied to the contact pads located at the chip edges and return to the superconducting ground plane, and then are taken off the chip through the contact pads to the ground plane (metal layer M0) also located at the chip edges. At room temperature, where the wafer processing is done, the ground plane is just a lightly patterned piece of highly conducting metal (Nb) film about the size of the chip (typically 5 by 5 mm^2 or 10 by 10 mm^2). The pattern etched in the ground plane is simply a large number of moats (holes) that are used to trap residual magnetic flux in the superconducting state. The typical sheet resistance of the ground plane in the normal state is R_{sq} ~ 2-3 ohms per square. The ground plane is electrically isolated from the Si wafer by a layer of SiO_2 thermally grown on the wafer surface. Ground planes of different chips on the wafer do not make electric contact to each other. In the simplest case, Josephson junctions in the circuits fall into the two categories – junctions with base electrode directly connected to the ground plane and junctions with base electrode electrically isolated from the ground plane (floating junctions). The simplest example is just a series array of junctions where all the junctions are floating except for the last junction, as shown in figure 1.

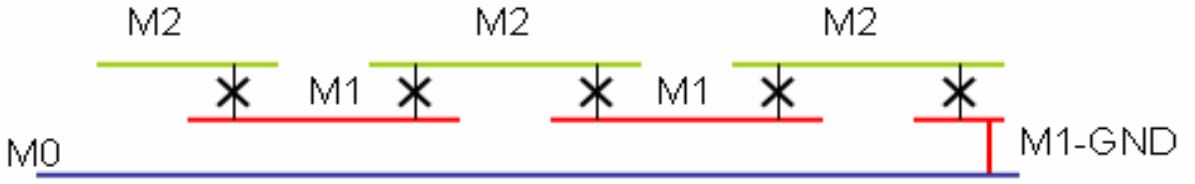

Figure 1. A series array of Josephson junctions showing that base electrodes of the junctions (layer M1) form floating islands that are not electrically connected to the ground plane (layer M0) up until the wiring layer M2 is deposited. The last junction in the array (referred to as M1-GND) is connected to M0 layer by its base electrode through a contact hole in the interlayer insulation.

Consider an incompletely processed circuit at a fabrication stage when all contacts to the junctions' counter electrodes and to the ground plane have been etched as shown in figure 2(a). If such a circuit is exposed to a nonuniform plasma, the ground plane will float close to the minimum of the floating potential distribution, as shown in figure 2(a), due to an asymmetric response of the plasma to the positive and negative potential on an object and to the fact that electron current from the plasma can be much higher than the ion current. All the junctions which do not make a contact with the ground plane will be charged to their individual floating potentials which are position dependent and determined by the local plasma potential. The charge will reside on the isolated metal islands formed by the junction base and counter electrodes. Except for a very brief charging transient (~ a few microseconds), no current will flow through the junctions in the stationary state and there will be no voltage difference across the tunnel barrier of the junctions. However, this is not the case for the junction whose base electrode is in electric contact with the ground plane. For this junction, its counter electrode would also like to float to a local floating potential but its base electrode is tied to the ground plane potential that is determined by exposure of the large ground contacts to the plasma at the chip edges. As a result, an electric field will develop across the junction and there will be an electric current flowing through the junction. This plasma-induced current will be determined by the potential difference and electric resistance of the current pass as shown in the circuit diagram in figure 2(b) $I_p = \Delta V_f/(R_J+R_{GP}+R_p)$, where R_J is the junction resistance in the normal state at room temperature, R_{GP} is the resistance of the current pass from the junction through the ground plane to the ground plane

contacts, and R_p is the plasma internal resistance. For simplicity we modelled plasma as a current limited voltage source and ignored all dependences on time that may exist in RF-driven plasma. If needed they can be included in the full model similarly to how it is done in analyzing gate oxide charging [12].

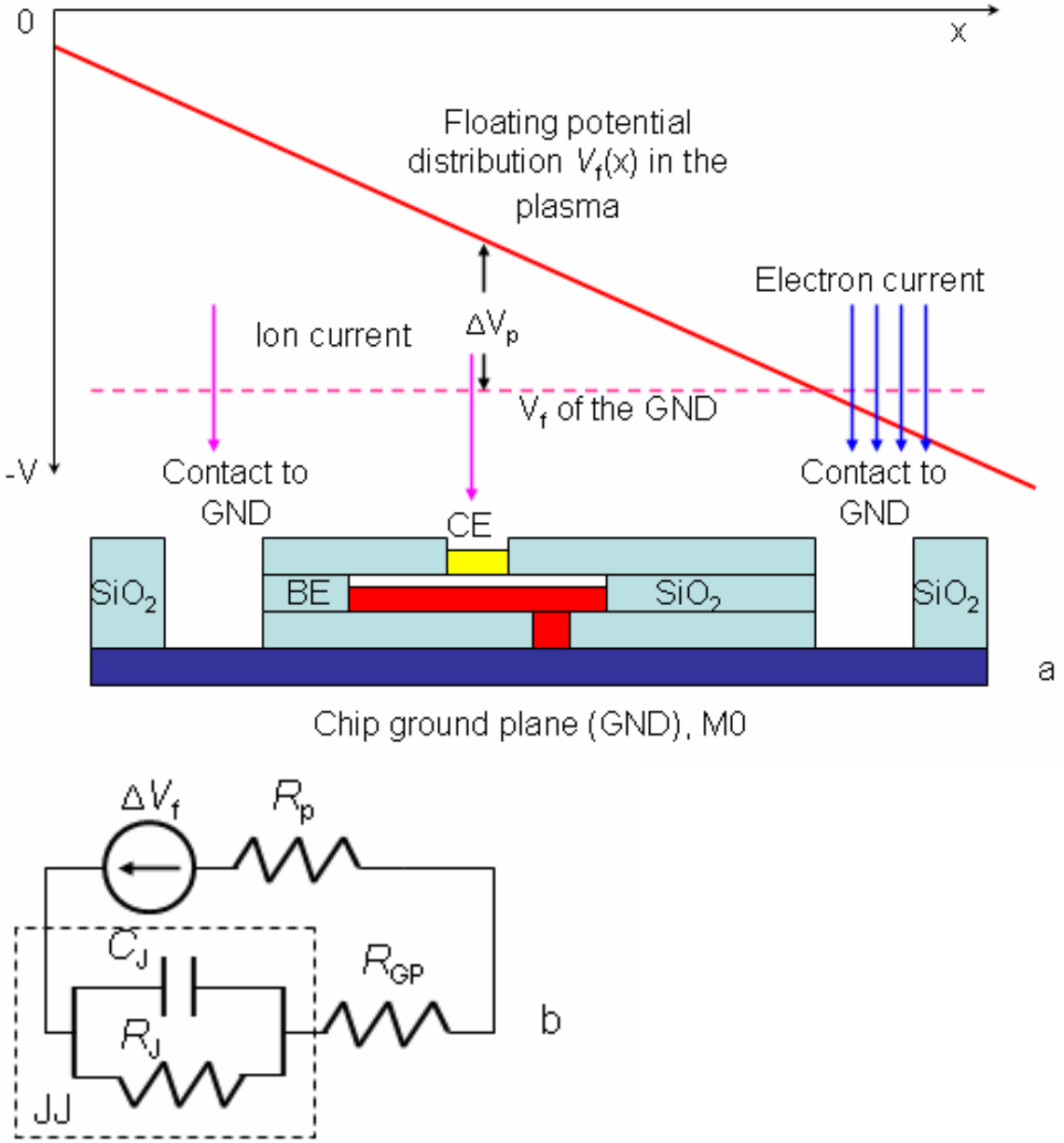

Figure 2. a) Test chip exposed to nonuniform plasma after contacts to the chip ground plane and to the junctions' counter electrode (CE) have already been etched. Junction's base electrode (BE) is shown in red, Al/AlO_x barrier in white, CE in yellow, GNP in blue. b) Simplified circuit diagram with a nonlinear plasma model replaced by a current-limited voltage source.

If the potential difference across the junction and the corresponding current are high enough, an electric stress (soft breakdown) may occur that will irreversible change the properties of the junction. The breakdown voltage for the ultra thin (~1 nm) AlO_x barrier used in superDICs is $V_{bd} \sim 0.6$ V [7,13,14]. Since the junction resistance is determined by the tunnel barrier, $R_J \approx R_N$ where R_N is the junction normal resistance at 4.2 K (we neglect for simplicity the dependence of the tunnel resistance

on the applied voltage and on temperature). Then, the estimate of the breakdown current becomes $I_{bd} = V_{bd}/R_N = V_{bd}I_c/(I_cR_N)$. Since for Nb-based junctions the I_cR_N product is approximately 1.5 mV, the typical breakdown current scales with the critical current of the junction as $I_{bd} \approx 400I_c$. For the smallest size junctions used in superDICs: $I_c \sim 100$ μA and, hence, $I_{bd} \sim 40$ mA. Note that V_{bd} strongly depends on temperature [14], decreasing almost tenfold at $T > 450$ K. Therefore, I_{bd} may be a few times less if the wafer temperature rises during the plasma processing.

So if in the process of fabrication, superconducting integrated circuits are exposed to nonuniform plasma such that both electrodes of Josephson junctions are in contact with the plasma, electric breakdown of the tunnel barrier in the junctions may occur if the plasma can supply enough current.

3. Experiment

The simple model given above explains the difference between the critical currents of the floating and grounded junctions that was first found in [6,7]. How can one verify that the proposed scenario indeed takes place and the cause of the damage is indeed the plasma-induced electric current through the junctions? The easiest thing is to test the model. Let us fix the wafer processing conditions and increase only the resistance of the ground plane pass R_{GP}. Since the plasma-induced current is inversely proportional to the R_{GP}, a transition from the damaged junctions to undamaged junctions should be observed with R_{GP} increasing.

3.1 Test chip design

The test chip containing eighteen 20-junction arrays of the circular junctions was placed in many locations on 150-mm process wafers for simultaneous processing with superDICs. The chip size was 5x5 mm^2 and the junctions' diameter was 1.8 μm for the wafers with 4.5 kA/cm^2 critical current density and 3.6 μm for 1.0 kA/cm^2, giving the target critical current $I_c \sim 100$ μA in both cases. This is the smallest I_c typically used in superDICs. The first 19 junctions in the arrays are floating and the last junction is connected to the ground plane by its base electrode (layer M1). A photograph of the test chip is shown in figure 3. In order to increase the ground pass resistance some of the arrays where surrounded by a moat in the ground plane forming a bottleneck shape as shown in the right panel of figure 3. The length l and width w of this bottleneck determine the resistance between the M1-gounded junctions and the contact pads to the ground plane according to $R_{GP} = R_{sq}l/w$, where $R_{sq} = 2$ Ω/sq is the sheet resistance of the ground plane Nb film. Some arrays were completely surrounded by a moat in order to form an island in the ground plane totally isolated from the ground plane contacts at the edges of the test chip, corresponding to $R_{GP} = \infty$. Electrical connection to such isolated islands was made by the first wiring layer M2. Since the area of the island is much smaller than the area of the ground plane, testing of these arrays allows us to study the effect of M0 metal antenna area on the critical current. All the arrays were placed close to each other in the centre of the test chip in order to minimize any critical current variation due to possible critical current density gradient across the chip.

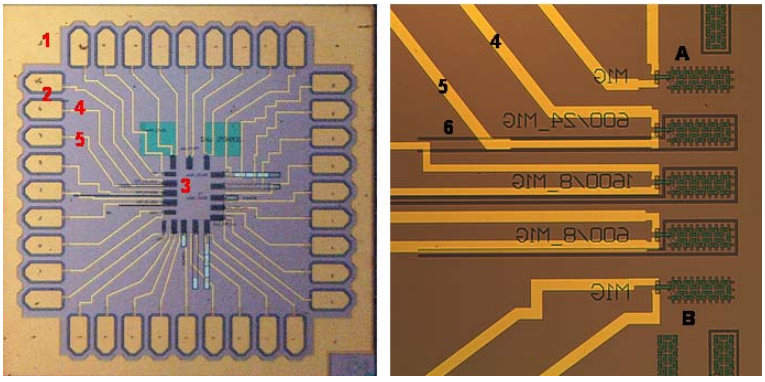

Figure 3 (left panel). Test chip view showing large contact to the ground plane around chip edges (1), signal contact pads (2), arrays of JJs (3), voltage and current leads (4), (5).

Figure 3 (right panel). Blow up of the test arrays with M1-grounded junctions (marked **A** and **B**) and with different resistor R_{GP} in the ground plane formed by a moat (6) in ground plane layer M0.

All wafers with test chips and other superDICs went through the full fabrication cycle using an 11-level fabrication process with Nb/Al/AlO_x/Nb Josephson junctions as described in detail in [2,7,15]. After the fabrication all the arrays were tested by a 4-probe *I-V* measurements in a magnetically shielded cryoprobe using a data acquisition system with Keithley 6220 precision current source, Keithley 2182A nanovoltmeter, and low pass *RC* filters in all wires.

4. Experimental results

Figure 4 shows the typical *I-V* characteristics of 20-junction arrays of unshunted Josephson junctions with the last junction connected to the ground plane by its base electrode (M1-GND junction). The deviation of the critical current of one junction (the last JJ) in the array from the average is clearly seen (arrays A and B). It is a signature mark of the difference between the floating and the M1-grounded junctions as was first found in [6,7]. A pronounced feature also exists in the return current branch where the damaged junction shows much higher subgap leakage current than the rest of the JJs in the array. More details of this behaviour are shown in figure 5. Figure 4 shows also the *I-V* characteristics of the identical arrays but with different ground plane resistors R_{GP}. It is clearly seen that the amplitude of the anomalous 1-junction deviation diminishes with R_{GP} increasing and basically seizes to exist at $R_{GP} > 150\ \Omega$. All the arrays on electrically isolated islands of ground plane do not show any abnormal deviation of the M1-grounded junction from the floating junctions or anomalies on the return branch as also shown in figure 4.

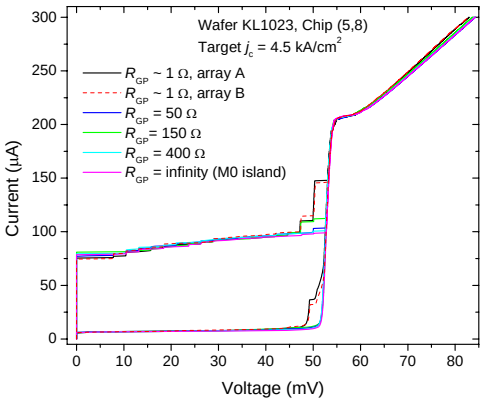

Figure 4. The current-voltage characteristics of six 20-junctions arrays of unshunted circular JJs with 1.8 μm diameter from a test chip located in the top right quadrant of the wafer. Different curves correspond to the different resistor R_{GP} in the ground plane pass for the plasma-induced current during wafer processing. The I_c of the M1-grounded junction deviates more than 40% from the mean when R_{GP} is low. The deviation disappears at R_{GP} larger than ~150 Ω.

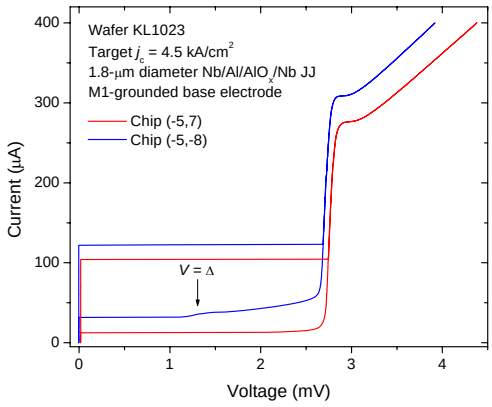

Figure 5. *I-V* characteristics of a single Josephson junction from un undamaged part of the wafer [chip (-5,7)] and from the part that experienced significant plasma-induced damage [chip (-5,-8) in the left bottom quadrant of the wafer]. The critical current enhancement in the damaged JJ is about 18% whereas the subgap current at 2 mV increased 235%, showing that subgap leakage is the most sensitive indicator of the plasma-induced charging damage to the ultrathin tunnel barriers.

Figure 5 shows the *I-V* characteristics of two nominally identical single M1-grounded junctions from the test chips located in strongly plasma-damaged and undamaged parts of the wafer. In addition to the greatly enhanced critical current density in the junction from the high damage region, we see also a greatly enhanced subgap leakage current in the return branch of the *I-V* curve. It means that charging-induced electric stress creates additional channels for the supercurrent in the tunnel barrier (e.g., nanoshorts) that contribute both to the critical current and to the subgap current. Conduction via such channels can be due, e.g., to Andreev reflection processes. An indication of this is the appearance

of a pronounced subgap step at $V = \Delta$ where Δ is the superconducting gap in the junction electrodes. More detailed results on Josephson tunnelling and subgap conductance in electrically stressed Josephson junctions will be published elsewhere [16]. Our measurements show that the subgap leakage current is even more sensitive indicator of the charging damage than the difference between the critical currents of the floating and M1-grounded junctions.

So we have tested all the predictions of the plasma charging model described in section 2.1 and found the experimental results to be fully consistent with the model. This proves that the difference between the critical currents of the floating and grounded junctions and other pattern-dependent effects discovered in our previous works [6,7] are indeed caused by plasma-induced charging damage to ultrathin tunnel barrier of the Josephson junctions.

4.1 Extreme cases of plasma damage and damage distribution across the wafer

In many cases we have observed that in some parts of the wafer the plasma-induced damage can be so strong that not only M1-grounded junctions become damaged but also the floating ones as shown in figure 6 that compares an array of junctions from a strongly damaged chip (-8,-7) from the bottom left quadrant of the wafer and practically undamaged chip (-1,1) from the wafer centre. An enormously increased subgap leakage can be easily seen in all of the junctions on chip (-8,-7) whereas only M1-grounded JJ is damaged on chip (-1,1). Another interesting feature of plasma-induced damage is in dramatic increase of the critical current spread in junctions of the same size. If we exclude the M1-grounded JJ and compare only the floating JJs, the total spread of the critical currents in the array on chip (-1,1) is $I_c^{max} - I_c^{min} = 12$ μA and the mean $I_c = 134$ μA. That is the relative total spread is about ±4.5%. On the other hand, the array on chip (-8,-7) has a total spread of 64 μA at a mean $I_c = 210$ μA, that is a relative spread of ±15%. This increase in the spread of the junction critical currents is the second main factor that renders complex digital integrated circuit un-operational. We suggest that the spread of I_cs increases due to a statistical nature of the barrier soft breakdown. That is, although the junctions experience the same electric stress, their barrier transparency change has probabilistic character that is described by some distribution function. For instance it is known that the hard breakdown in oxides is well described by the Weibull distribution $F(V) = 1 - \exp[(-V/V_c)^{\beta}]$, where $F(V)$ is the cumulative failure fraction at a stress voltage V, V_c is the characteristic breakdown voltage, and β is the Weibull slope, see for instance [8]. More experimental results on damage statistics in $Nb/Al/AlO_x/Nb$ tunnel junctions will be presented elsewhere [16].

In order to get more insight into which processing step may cause the plasma charging damage in our fabrication process we looked into the space distribution of damage to M1-grounded junctions. Since the most sensitive indicator is the subgap resistance of the junctions, in figure 7 we show the distribution map of the subgap resistance of 20-JJ arrays at 40 mV (number of JJs times 2 mV). The map indicates the presence of a strong gradient of plasma-induced damage in basically one direction. This gradient is most likely a result of a strong gradient of the plasma potential in one of the plasma processing tools coupled with a wafer temperature gradient.

4. Discussion

From the value of ground plane resistor at which the damage to floating JJs disappears $R_{GP} \sim 150$ Ω we can roughly estimate the floating potential difference needed to establish a soft breakdown voltage $V_{BD} \sim 0.6$ V across an M1-GND junction by assuming that the plasma resistance R_p is much less than R_{GP}. This gives $\Delta V_p \sim 6$ V. Since the typical distance between the JJ arrays and the ground plane contacts at the chip edge is ~ 2 mm, it means that the floating potential gradient is ~ 30 V/cm. This is too large a gradient to exist in any modern plasma etching or dielectric deposition systems used in the fabrication process in this work. (Both the reactive ion etching and the plasma-enhanced chemical vapour deposition systems used in this work are designed for VLSI fabrication in semiconductor industry.)

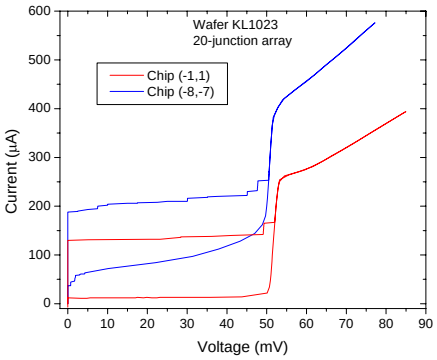

Figure 6. *I-V* characteristics of JJ arrays in the case of strong plasma-induced damage to all the junctions in the 20-JJ array [chip (-8,-7)]. Both the critical and subgap leakage currents are strongly enhanced in the floating JJs so the difference with M1-GND JJ is less pronounced.

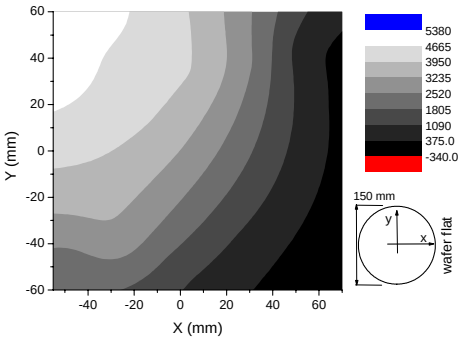

Figure 7. Gray scale map of the subgap resistance of 20-JJ arrays at V= 40 mV on wafer KL1023. The last JJ in each array is grounded by its base electrode (M1-GND). Gray scale is ohms. The higher is the subgap resistance the lesser is the damage. The typical normal state resistance of an undamaged array at j_c = 4.5 kA/cm^2 is ~260 Ω.

The only system where a large plasma potential gradient may exist is a dc magnetron sputtering system that is used for Nb wiring layers deposition (layers M2 and M3). This system is designed such that the wafer is scanned under the sputtering gun in order to increase the deposited film uniformity. It means that a wafer with all contacts to the junctions and to the ground plane opened is moved from the area of no plasma (V_f =0) to the area of a very strong plasma (V_f ~ -35 V). Since the deposition power is quite large (2.28 kW) such plasma can support enough current to produce significant damage to many junctions. Also as the scan progresses, the wafer temperature rises. This in turn decreases the breakdown voltage and breakdown current, thus increasing the damage. The wafer scan direction and wafer orientation are fully consistent with the damage map shown in figure 7. An interesting issue of how a strong differential charging and plasma-induced damage can be generated at a metal deposition that is supposed to produce an equipotential surface on the wafer will be considered separately [17].

In conclusion, we have studied the effects of plasma-induced damage on the *I-V* characteristics and Josephson junction parameters on 150-mm wafers fabricated by an 11-level process for superconducting integrated circuits. All the results were found to be fully consistent with the proposed model of nonuniform charging in nonuniform plasma that causes soft breakdown of the ultrathin AlO_x tunnel barrier. The observed large deviations of the critical currents of Josephson junctions from the design values coupled with the found dependence of the critical current on the type of junction connection to the ground plane and to other circuit elements are the prime limitations on the yield and complexity of superconducting digital circuits. A thorough development work is needed in order to minimize and possibly eliminate plasma charging damage to superconducting integrated circuits. Plasma-induced damage can be reduced by increasing the resistance of the ground plane by adding moat structures and by designing the fabrication process such that the junctions and the ground plane are not exposed to plasmas at the same time.

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