EE657 – Parallel and Distributed Computing
Fall 2013
Instructors: Murali Annavaram, Mary Eshaghian-Wilner and Michel Dubois

Preliminary Syllabus--subject to change
Final syllabus will depend on the number of students. TA information is missing.

1. Overview

EE657 is a unique course offering with three instructors each teaching one mini-course in parallel and distributed computing focused on a particular topic. In the Fall of 2013 EE657 will focus on three topics: (1) General Purpose Graphical Processing Units (GPGPUs) designs (Annavaram), (2) Interconnection Topologies (Eshaghian-Wilner) and (3) Transactional Memory (Dubois). The first six lectures will be dedicated to the overview of each mini-course and will be followed by approximately 7 lectures on each topic (for a total of 9 lectures on each topic). Each mini-course will include a midterm. The list of topics covered is given below. But please note that these are just rough guidelines as the actual topic list may slightly vary due to time constraints.

- **GPGPU.** Topics covered include: (1) Overview of GPU design and SIMT execution paradigm, (2) Kepler microarchitecture, (3) GPGPUsim simulator details, (4) CUDA programming language for programming GPGPUs from NVidia, (5) GPGPU power efficiency, (6) GPGPU reliability concerns

- **Interconnection Topologies.** Topic covered include: (1) Overview of Static Topologies, (2) Multi-Stage Interconnection Networks, (3) VLSI Reconfigurable Connections, (4) Optical and Electro-optical Interconnects, (5) Interconnections for Heterogeneous/Cluster/Grid/Cloud Computing, and (6) Nanoscale Connectivity.

- **Transactional Memory (TM).** TM is a paradigm to simplify parallel programming in which locks are replaced by transactions. TM topics include: (1) TM design principles, (2) Classification of TM systems, (3) Intel and IBM architectural support for TM, (4) Example of TM systems (HTM, TCC and derivatives, UTM, Log-TM, etc), (5) SESC/SuperTrans simulation environment, and (6) Bulk-based shared-memory.

2. Textbooks

Dubois, Annavaram and Stenström: "Parallel Comupter Organization and Design" Cambridge University Press, 2012. ISBN: 978-0-521-88675-8. Purchase from the USC bookstore or from Amazon.com. REQUIRED. This book contains EE557 material. Some material not covered in EE557 will be taught from this book supplemented with additional material that will be provided on the blackboard. Also some problems and reading assignments will be picked from the book.

A list of required readings and notes will be posted on the blackboard, from which copies can be downloaded.

3. Prerequisite

EE557. Computer System Architecture.

4. Instructor Information

Michel Dubois: Office: EEB228. Tel:(213) 740-4475. E-mail: dubois@paris.usc.edu. Office hours: 11-12MW or by appointment.

Murali Annavaram: Office: EEB 232. Tel: (213) 740-3299. E-mail: annavara@usc.edu. Office hours: MW: 2-3PM or by appointment.

Mary Eshaghian-Wilner: Office: EEB 300. Tel: (213)-740-6257. E-mail: eshaghia@usc.edu. Office hours: 12:30-2:00 PM TTH by appointment.

5. TA

Chieh-Ting Huang (aka Justin). Tel: (213) 740 4372. E-mail: chiehtih@usc.edu. Office hours: 10-12TU in PHE330. The TA will help with simulation environments and projects.

6. Venue and Time

KAP 163—Tu-Th 2-3:20pm.

7. Course Work and Grading

Each mini-course will have a set of quizzes (5% for each mini-course) and one midterm (20% for each mini-course). One project (over the entire course) involving simulations of parallel systems will be assigned (25%).

Midterms can be in-class or take-home. The policies for midterms are at the discretion of each instructor. Each instructor may also have their own policy with regard to administration and number of quizzes.

A list of projects will be given at the beginning of the semester. The final will be dedicated to the presentation of projects. The projects should be done by teams of two students and both students in a team will receive the same grade for the project.

8. Statement for Students with Disabilities

Any student requesting academic accommodations based on a disability is required to register with Disability Services and Programs (DSP) each semester. A letter of verification for approved accommodations can be obtained from DSP. Please be sure the letter is delivered to me (or to TA) as early in the semester as possible. DSP is located in STU 301 and is open 8:30 a.m.-5:00 p.m., Monday through Friday. The phone number for DSP is (213) 740-0776.

9. Statement on Academic Integrity

USC seeks to maintain an optimal learning environment. General principles of academic honesty include the concept of respect for the intellectual property of others, the expectation that individual work will be submitted unless otherwise allowed by an instructor, and the obligations both to protect one's own academic work from misuse by others as well as to avoid using another's work as one's own. All students are expected to understand and abide by these principles. Scampus, the Student Guidebook, contains the Student Conduct Code in Section 11.00, while the recommended sanctions are located in Appendix A: http://www.usc.edu/dept/publications/SCAMPUS/gov/. Students will be referred to the Office of Student Judicial Affairs and Community Standards for further review, should there be any suspicion of academic dishonesty. The Review process can be found at: http://www.usc.edu/student-affairs/SJACS/.

12. Tentative Course Schedule:

MA: Murali Annavaram; MD: Michel Dubois; MEW: Mary Eshaghian-Wilner

Lecture	Date	Topics	Instructor	MILESTONES/REMARKS
Lect 1	8/27	Introduction to the course	MA,MD,MEW	
Lect 2	8/29	Interconnection Topologies	MEW	
Lect 3	9/3	Interconnection Topologies	MEW	
Lect 4	9/5	Transactional Memory	MD	
Lect 5	9/10	Transactional Memory	MD	
Lect 6	9/12	GPGPU	MA	Friday 9/13: Last day to drop w/o W
Lect 7	9/17	GPGPU	MA	
Lect 8	9/19	GPGPU	MA	
Lect 9	9/24	GPGPU	MA	
Lect 10	9/26	GPGPU	MA	
Lect 11	10/1	GPGPU	MA	
Lect 12	10/3	GPGPU	MA	
Lect 13	10/8	GPGPU	MA	
Lect 14	10/10	GPGPU	MA	MIDTERM #1
Lect 15	10/15	Interconnection Topologies	MEW	
Lect 16	10/17	Interconnection Topologies	MEW	
Lect 17	10/22	Interconnection Topologies	MEW	
Lect 18	10/24	Interconnection Topologies	MEW	
Lect 19	10/29	Interconnection Topologies	MEW	
Lect 20	10/31	Interconnection Topologies	MEW	
Lect 21	11/5	Interconnection Topologies	MEW	MIDTERM #2
Lect 22	11/7	Transactional Memory	MD	
Lect 23	11/12	Transactional Memory	MD	
Lect 24	11/14	Transactional Memory	MD	Friday 11/15: Last day to drop with W
Lect 25	11/19	Transactional Memory	MD	
Lect 26	11/21	Transactional Memory	MD	
Lect 27	11/26	Transactional Memory	MD	
	11/28	No class		THANKSGIVING RECESS
Lect 28	12/3	Transactional Memory	MD	MIDTERM #3
Lect 29	12/5	Course wrap-up		
	12/6	END OF CLASSES		FINAL on Thursday 12/12

13. Transactional Memory (Dubois)

Lectures 1 and 2: Introduction: CMP programming paradigms and introduction to TM

Lecture 3: Lock-free data structures; Hardware Transactional Memory; Speculative Lock Elision

Lecture 4: Unbounded TM (UTM and LTM), Virtualized TM.

Lecture 5: Log-TM and applications

Lecture 6: SESC/SuperTrans Simulation environment; TM benchmarks; Transactional behavior of multi-threaded programs

Lecture 7: TM ISA support by Intel (TSX), by AMD (ASF), by IBM (TSX) and by Sun Sparc (Rock HTM)

Lecture 8: Transactional Cache Consistency and Bulk Consistency

Lecture 9: Software & Hybrid Transactional Memory—brief overview

14. GPGPUs (Annavaram)

Lectures 1 and 2: GPGPU Pipeline Basics

Lecture 3: Unified Shader Model and SIMT Execution

Lecture 4: GPGPU Parallelism Specification through CUDA, GPGPUsim basics

Lecture 5: Memory Hierarchy of GPGPUs

Lecture 6: Core Microarchitecture of GPGPUs

Lecture 7: Branch Divergence and Warp Formation Inefficiencies

Lecture 8: Efficient Warp Formation approaches

Lecture 9: Power and Reliability Considerations for GPGPUs

15. Interconnection Topologies (Eshaghian-Wilner)

Lectures 1 and 2: Introduction, Static Topologies and Evaluation Methods

Lecture 3: Multistage and Hierarchical Interconnection Networks

Lecture 4: VLSI Reconfigurable Connections

Lecture 5: Optical and Electro-optical Interconnects

Lecture 6 and 7: Interconnections for Heterogenous/Cluster/Grid Cloud Computing

Lecture 8 and 9: Nanoscale Connectivity: Self Assembled, Quantum Dots, Spin Wave