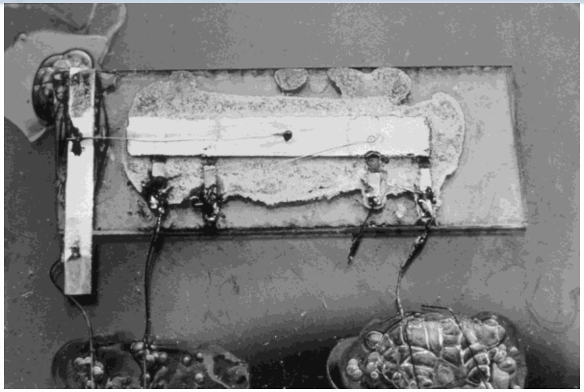
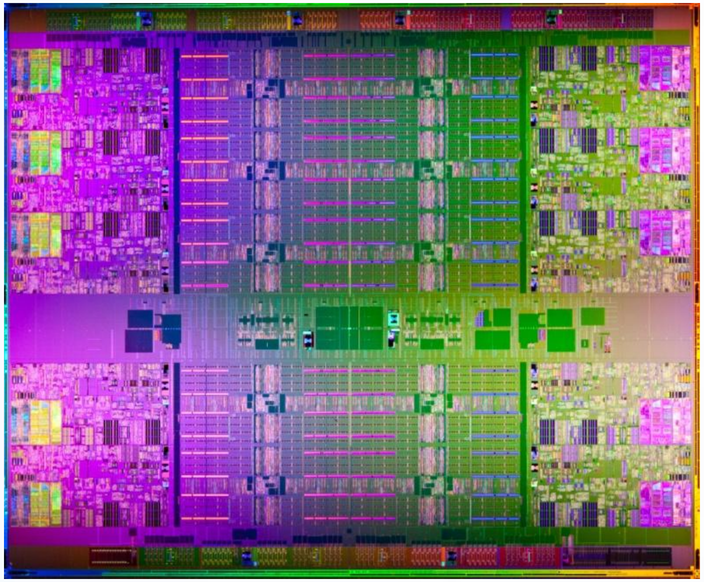
VLSI Trends

A Brief History

- 1958: First integrated circuit
  - Flip-flop using two transistors
  - From Texas Instruments
- 2011
  - Intel 10 Core Xeon Westmere-EX
    - 2.6 billion transistors
    - 32 nm process



Courtesy Texas Instruments

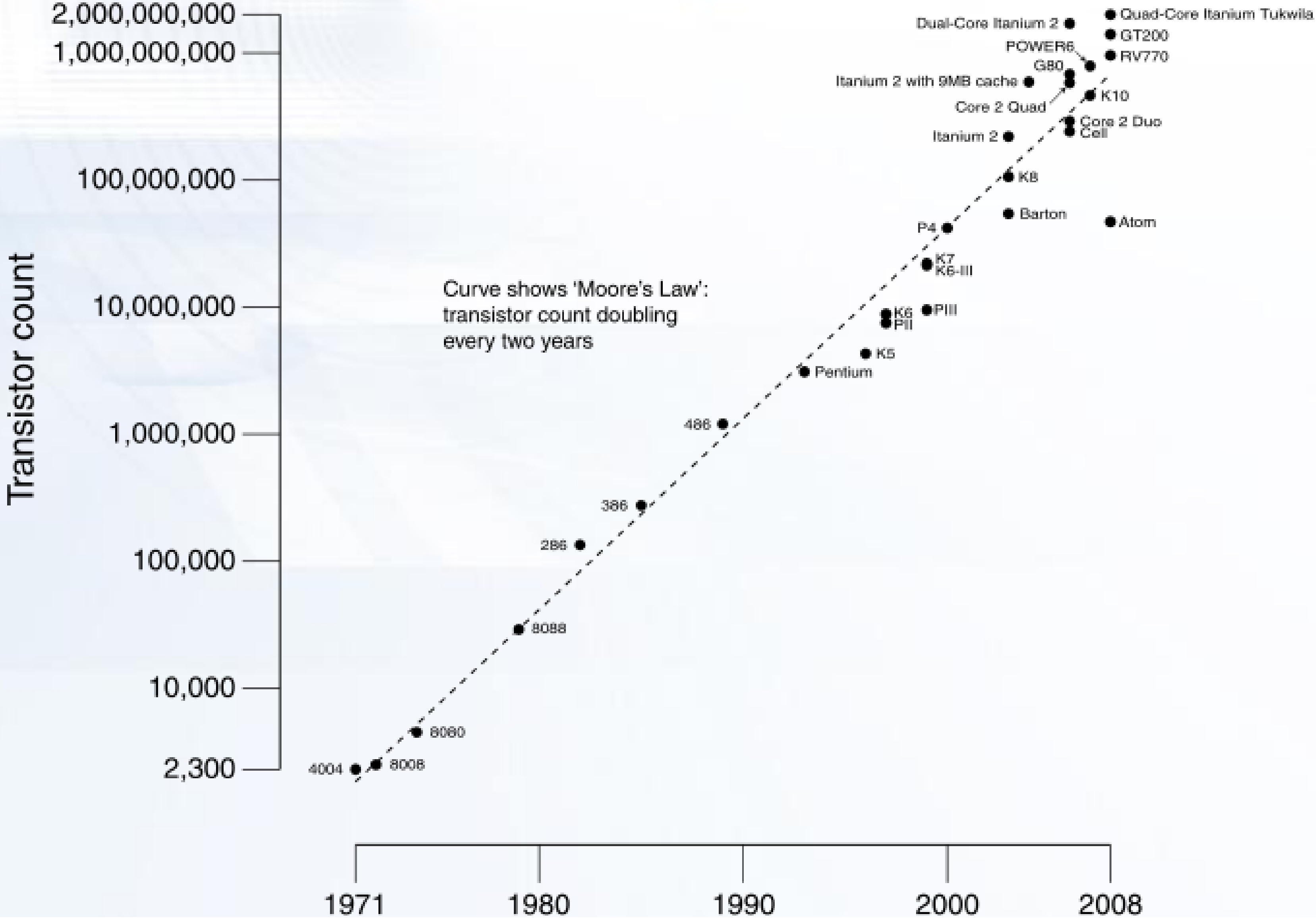


Courtesy Intel

Moore's Law

- **Growth rate**
  - 2x transistors & clock speeds every 2 years over 50 years
  - 10x every 6-7 years
- **Dramatically more complex algorithms previously not feasible**
  - Dramatically more realistic video games and graphics animation (e.g. Playstation 4, Xbox 360 Kinect, Nintendo Wii)
  - 1 Mb/s DSL to 10 Mb/s Cable to 2.4 Gb/s Fiber to Homes
  - 2G to 3G to 4G wireless communications
  - MPEG-1 to MPEG-2 to MPEG-4 to H.264 video compression
  - 480 x 270 (0.13 million pixels) NTSC to 1920x1080 (2 million pixels) HDTV resolution

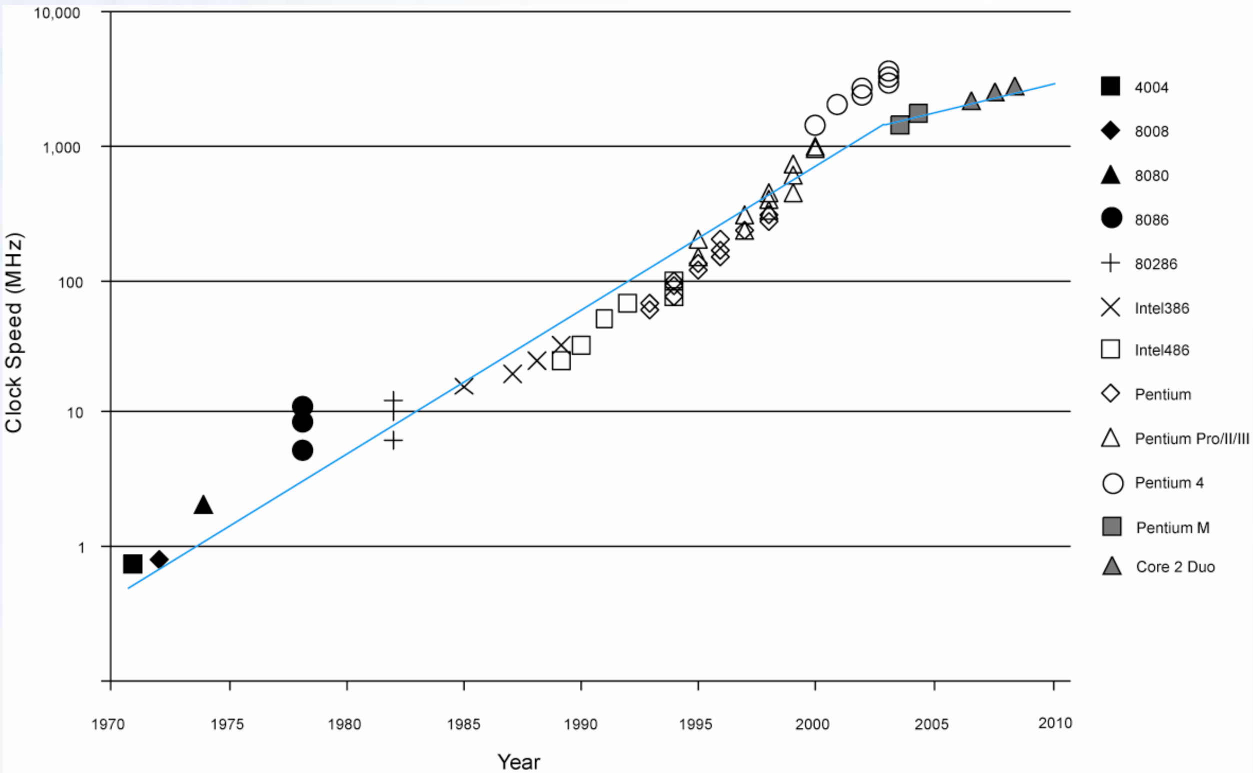
Moore's Law



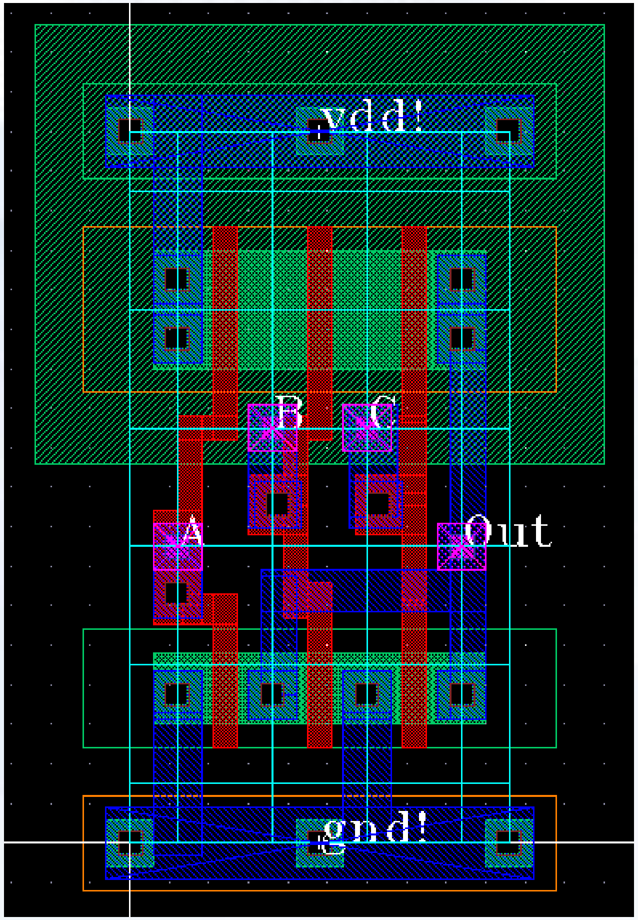
Transistor count
2,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
2,300
Curve shows 'Moore's Law': transistor count doubling every two years
Dual-Core Itanium 2
Quad-Core Itanium Tukwila
GT200
RV770
POWER6
G80
Itanium 2 with 9MB cache
Core 2 Quad
K10
Core 2 Duo
Cell
Itanium 2
K8
Barton
Atom
P4
K7
K6-III
K6
PII
PIII
K5
Pentium
486
386
286
8088
8080
8008
4004
1971
1980
1990
2000
2008

Moore's Law

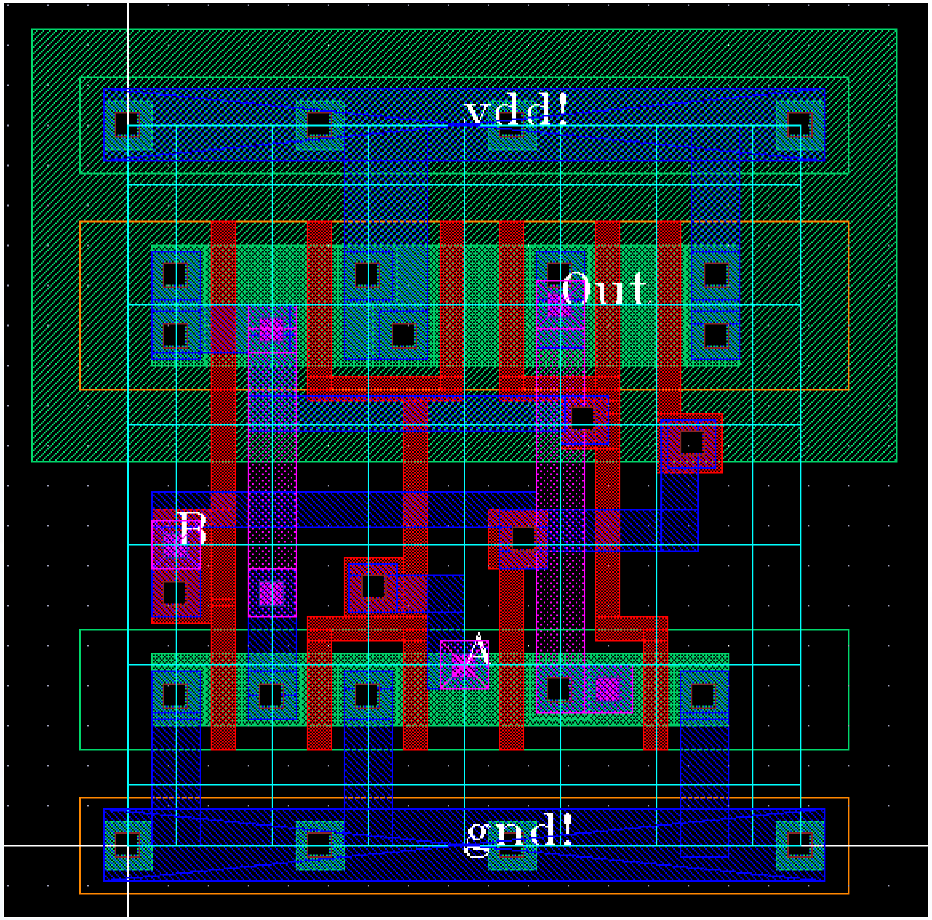
- Many other factors grow exponentially
  - Ex: clock frequency, processor performance



Standard Cells

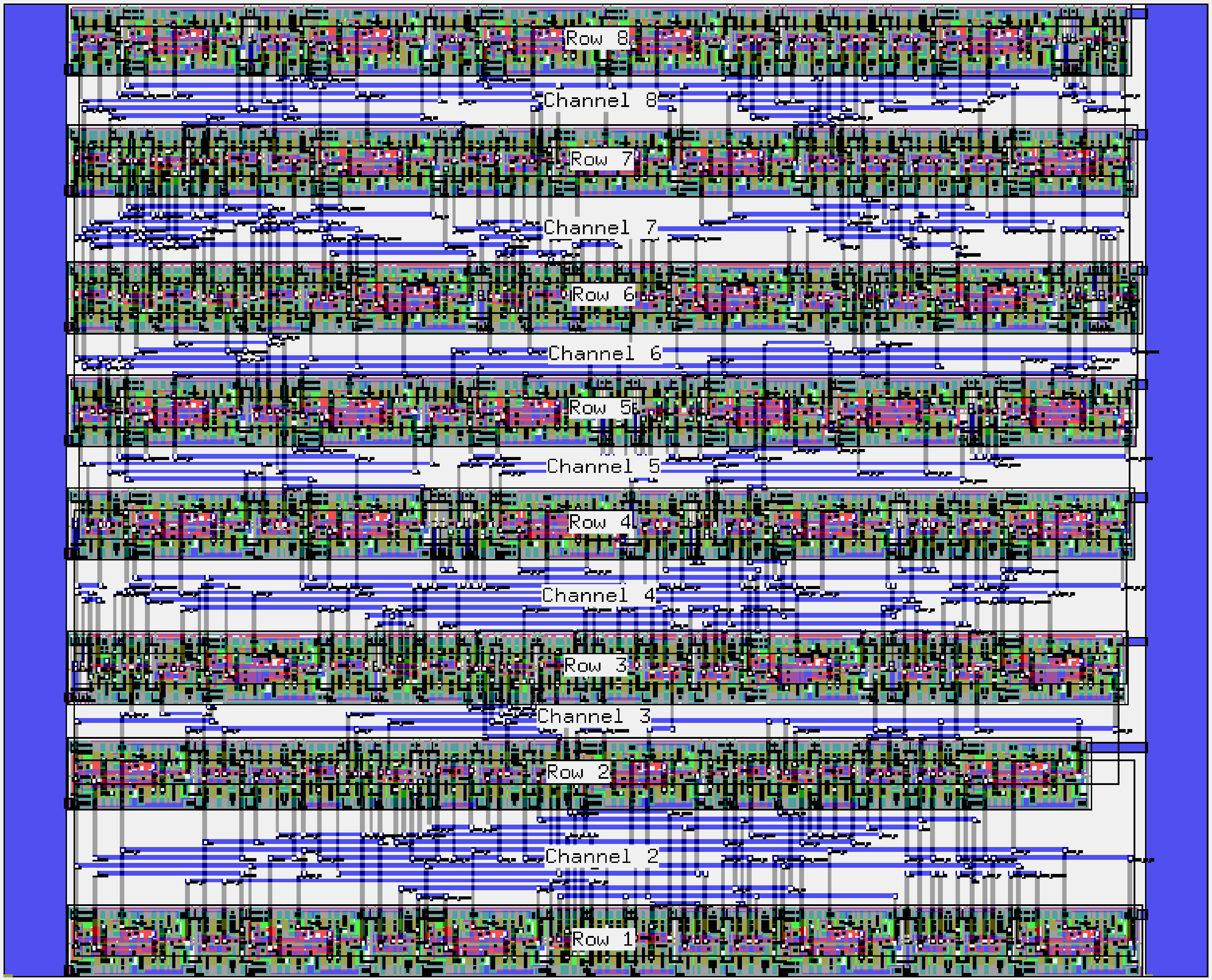


NOR-3



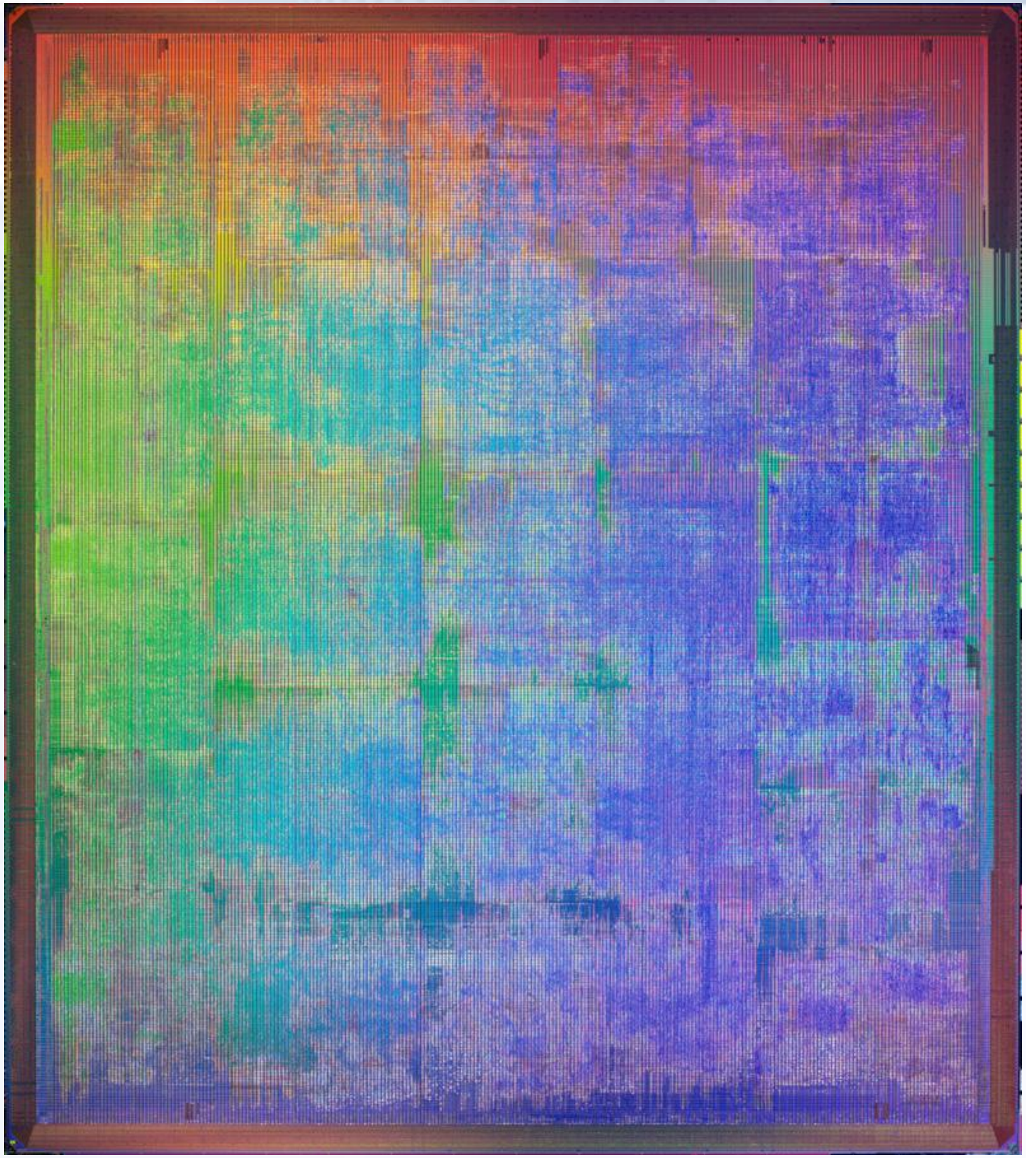
XOR-2

Standard Cell Layout

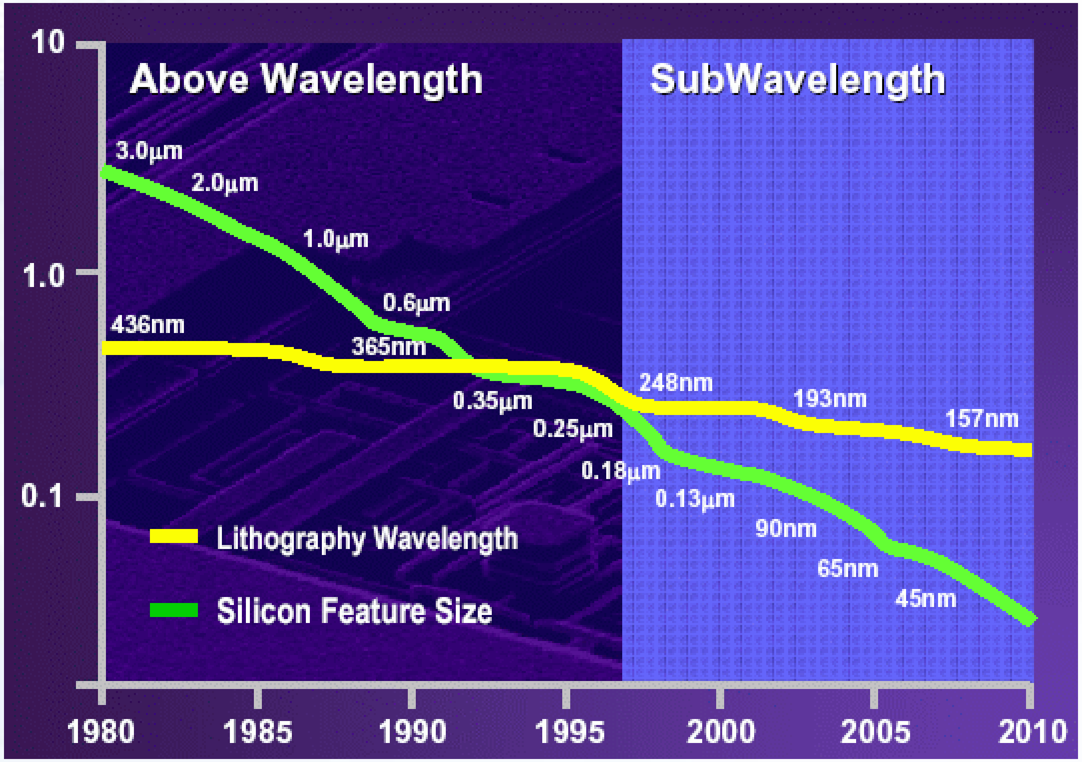


GeForce 8800

(600+ million transistors, about 60+ million gates)

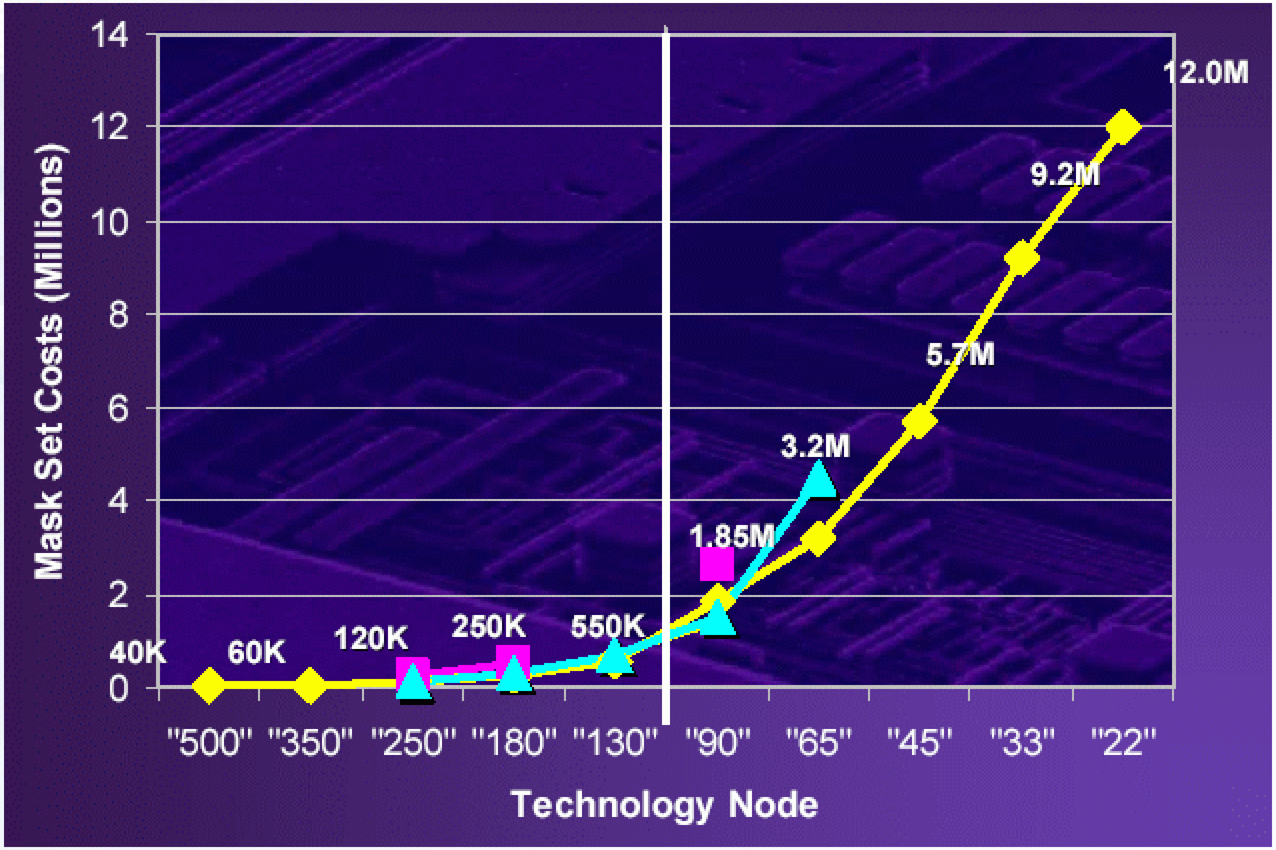


Subwavelength Lithography Challenges



Source: Raul Camposano, 2003

NRE Mask Costs



Source: MIT Lincoln Labs, M. Fritze, October 2002

ASIC NRE Costs Not Justified for Many Applications

- Forecast: By 2010, a complex ASIC will have an NRE Cost of over $40M = $28M (NRE Design Cost) + $12M (NRE Mask Cost)

- Many "ASIC" applications will not have the volume to justify a $40M NRE cost

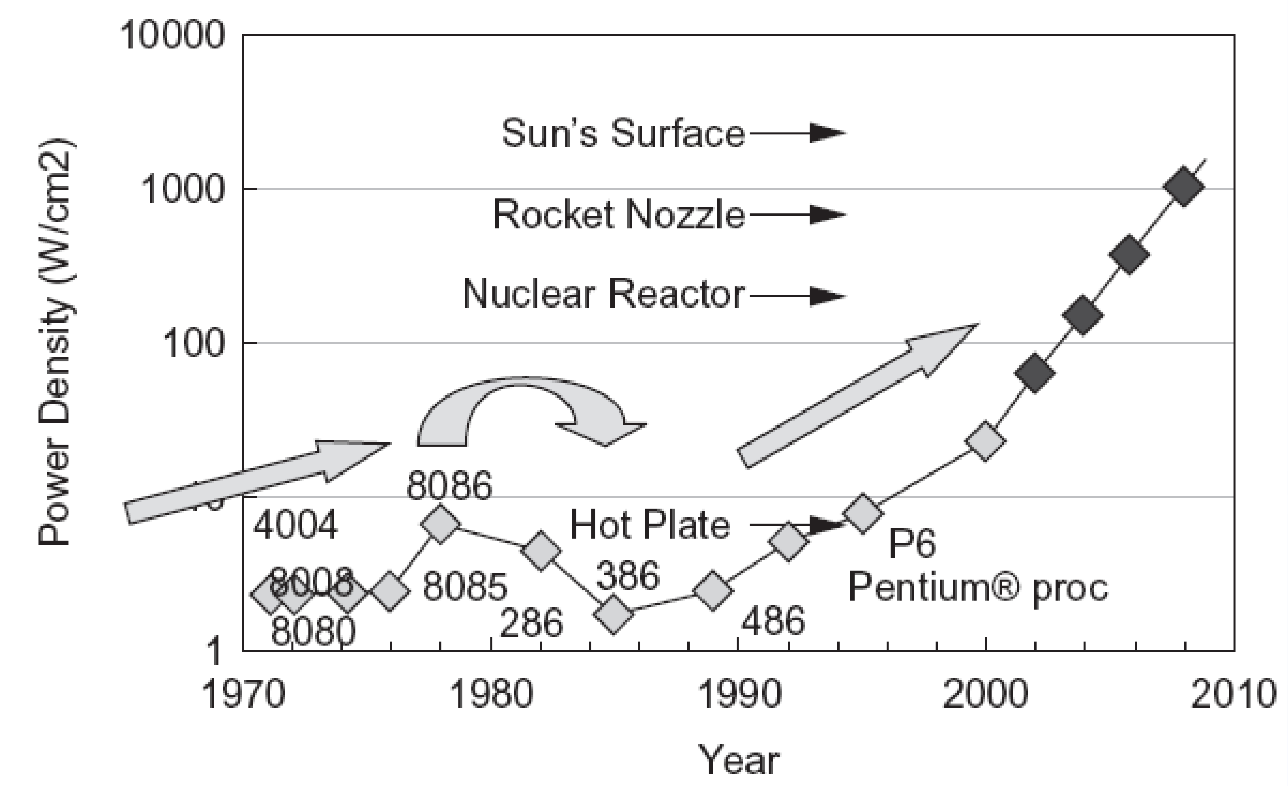
- e.g. a $30 IC with a 33% margin would require sales of 4M units (x $10 profit/IC) just to recoup $40M NRE Cost

Power Density a Key Issue

- Motivated mainly by power limits
- $P_{total} = P_{dynamic} + P_{leakage}$
- $P_{dynamic} = \frac{1}{2} \alpha C V_{DD}^2 f$
- Problem: power (heat dissipation) density has been growing exponentially because clock frequency (f) and transistor count have been doubling every 2 years

Power Density a Key Issue

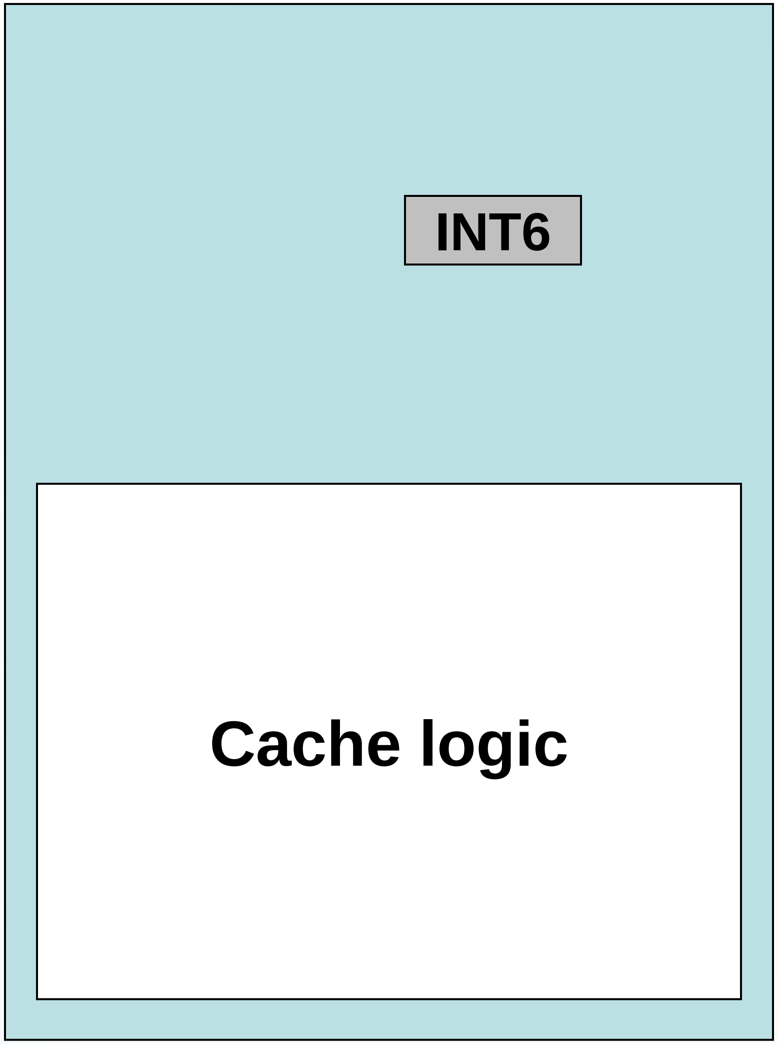
- **Intel VP Patrick Gelsinger (ISSCC 2001)**
  - **"If scaling continues at present pace, by 2005, high speed processors would have power density of nuclear reactor, by 2010, a rocket nozzle, and by 2015, surface of sun."**



Courtesy Intel

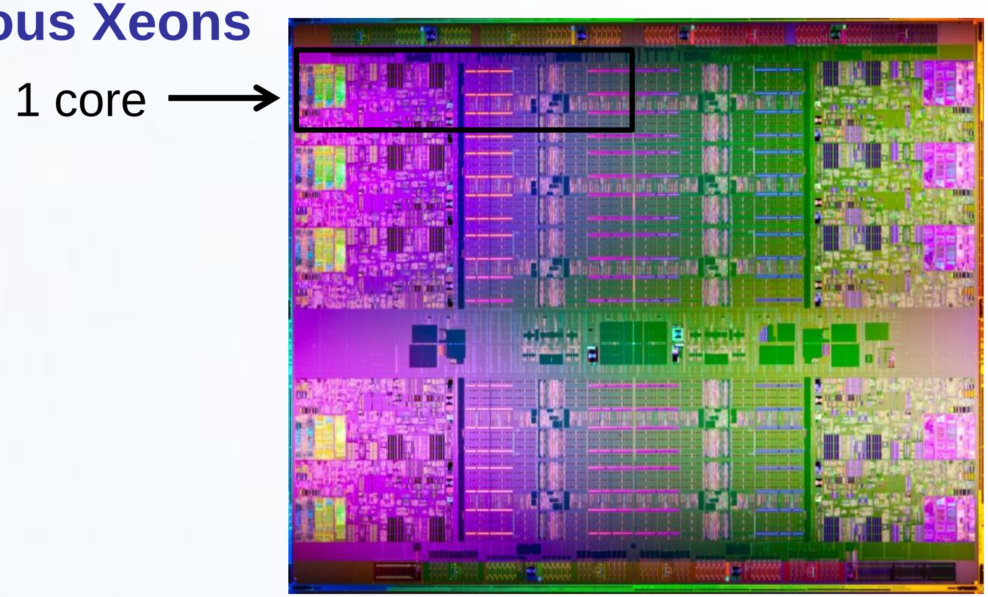
Before Multicore Processors

- e.g. Intel Itanium II
  - 6-Way Integer Unit < 2% die area
  - Cache logic > 50% die area
- Most of chip there to keep these 6 Integer Units at “peak” rate
- Main issue is external DRAM latency (50ns) to internal clock (0.25ns) is 200:1
- Increase performance by higher clock frequency and more complex pipelining & speculative execution



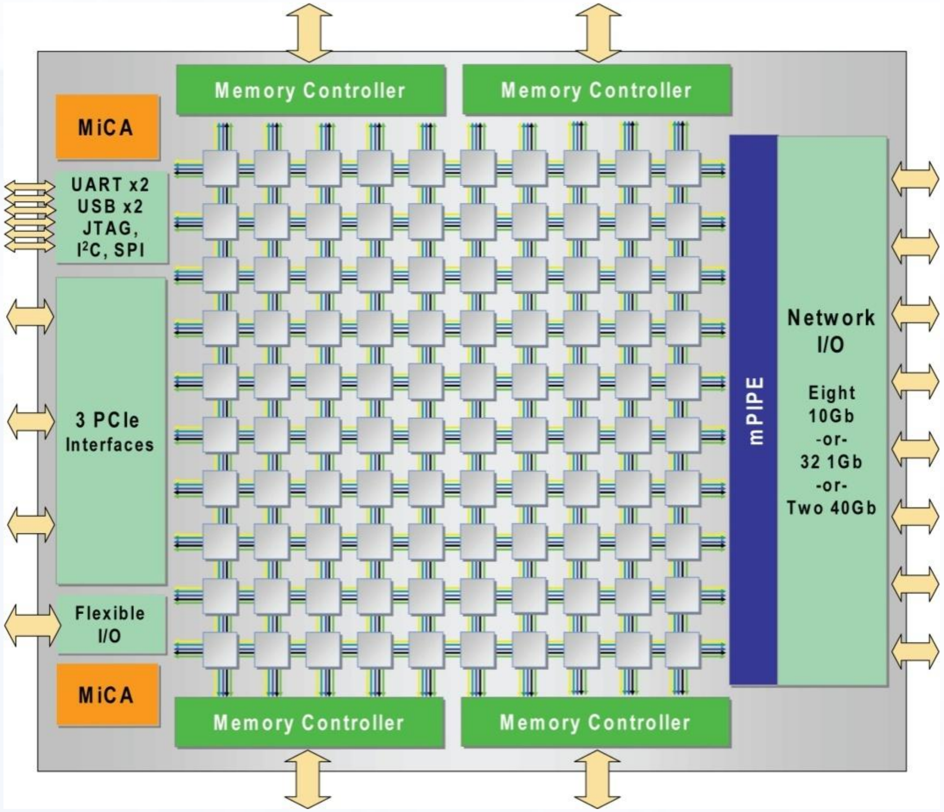
Multicore Era

- Multicore era
  - Operate at lower voltage and lower clock frequency
  - Simpler processor cores
  - Increase performance by more cores per chip
- e.g. Intel 10 Core Xeon Westmere-EX
  - 1.73-2.66 GHz (vs. previous Xeons at 4 Ghz)



Embedded Multicore Processors

- **Embedded multicore processors replacing ASICs**
  - Much simpler processor cores, much smaller caches
- **e.g. Tilera-GX: 100 processors**



What Does the Future Look Like?

Corollary of Moore's law: Number of cores will double every 18 months

	'02	'05	'08	'11	'14
Research	**16**	**64**	**256**	**1024**	**4096**
Industry	**4**	**16**	**64**	**256**	**1024**

(Cores minimally big enough to run a self-respecting OS!)

Source: MIT, A. Agrawal, 2009

ITRS Roadmap

- **Semiconductor Industry Association forecast**
  - **Intl. Technology Roadmap for Semiconductors**

Year	2009	2012	2015	2018	2021
Feature size (nm)	34	24	17	12	8.4
L_{gate} (nm)	20	14	10	7	5
V_{DD} (V)	1.0	0.9	0.8	0.7	0.65
Billions of transistors/die	1.5	3.1	6.2	12.4	24.7
Wiring levels	12	12	13	14	15
Maximum power (W)	198	198	198	198	198
DRAM capacity (Gb)	2	4	8	16	32
Flash capacity (Gb)	16	32	64	128	256