

EE 382M

VLSI-II: Class Project Overview

Mark McDermott

VLSI Design metrics, optimization & trade-offs

- **VLSI design is the process of finding an optimal point in a multidimensional space. There are no perfect circuits, no ‘right’ answers.**
 - **Obvious tradeoffs: area, power, frequency, performance**
- **Issues important for VLSI designers:**
 - **Robustness**
 - **Works in all the process corners**
 - **Scalable to next generation process**
 - **Trade-offs include:**
 - **Complexity and TTM (time to market)**
 - **Frequency and IPC (instructions/clock)**
 - **Frequency and power**
 - **Die size and performance**
- **TTV “Time to Volume” is the most important tradeoff to consider.**
 - **A high volume microprocessor can ship 500K-750K units per week generates revenues of \$100-\$300 per unit.**
 - **1% of performance is lost each week that you are late to the market place.**

What are design metrics?

- **There are numerous metrics which impact the successful design of a VLSI chip. The primary metrics include:**
 - **Area:** Size of the die, which relates to cost and profit
 - **Speed/Delay:** How fast the transistors can switch
 - **Power:** How much energy does it take to get the work done.
- **These metrics produce the resulting chip attributes :**
 - **IPC:** Number of instructions that can executed per clock cycle
 - **Frequency:** Inverse of the clock cycle.
 - **Performance:** The multiplication of the IPC and Frequency.
- **The challenge in chip design is accurately estimate the metrics before implementation.**
- **Usually a tradeoff between one of the primary metrics or chip attributes must be made to meet the TTM requirements**

Area Metric

- **This is the simplest to estimate:**
 - Measures the size of the circuits in mils² or microns²
 - Determines the cost of the resulting product.
- **Since the performance of the circuit depends on the wire delays, we would like to know what the size of the cells are during circuit design. We need area estimates as early as possible**
- **There are standard methods of estimating area from the schematic or RTL:**
 - For very regular structures (memory arrays or register files) it is best to lay out the base cell and do a rudimentary cell placement and floorplan.
 - For random/control logic, estimate using synthesis, and cell area or preliminary placement.
 - For datapath structures a combination of the regular structure and random logic estimation techniques.

Speed/Delay Metric

- **Units of measurement are typically:**
 - ns, ps, FO4 inv delay, etc.
- **What and how to measure is more considerably more complex:**
 - What are the constraints?
 - What paths are important.
 - Can the speed path be sensitized such that it is worse case?
- **DSM effects make it even harder:**
 - Noise, power delivery, cross-die transistor variations, etc all cause timing variations.
- **Other issues:**
 - How does the circuit need to be set up for worse-case delay?
 - What are the characteristics of the input signal?
 - Is time-borrowing valid?
 - Can we optimize either (or both) the rising and falling edges of the output signal?

Power Metric

- **Typical measurements include:**
 - **Standard power (W), or energy, or energy-delay**
- **The problem is that power is a strong function of performance, so you need to measure both power and performance to get a useful number.**
- **Two kinds of power:**
 - **Static**
 - **DC current that does not depend on signal activity, in bulk CMOS this is typically sub-threshold leakage**
 - **Dynamic**
 - **AC current proportional to signal transitions**
- **There are two primary issues associated with power:**
 - **Power delivery: this is the ability to deliver the voltage and current needed to run the chip.**
 - **Power extraction: The ability to remove the heat generated by the chip.**
- **Power will limit all future high performance DSM chip designs.**

Project design metrics

- **There are four metrics that we will be optimizing in this design:**
 - **Cycle time**
 - **Power**
 - **Area**
 - **TTFG (time to final grade).**
- **Naturally TTFG is the top priority. The remaining order of importance is:**
 - **Area: 8 mm²**
 - **Energy: .02 mw/MHz**
 - **Frequency: 30+MHz**
- **Technology: 65nm (Sub-threshold)**
- **VDD: 0.5v**

Overview of the project assignment

- **The intent of the project is to do a top-down design of an embedded processor. The project activities will include:**
 - Doing a detailed floorplan of the cluster level components.
 - Doing a detailed top-level floorplan using the cluster abstracts.
 - Determining the critical timing paths and setting the component constraints at the top level and the component level. If the critical path exceeds the timing budget, the logic will have to be re-designed or the micro-architecture will have to be re-pipelined. Timing will be negotiated among all clusters and the top-level integration team.
 - Doing a detailed power estimation determining the power grid requirements.
 - Determining the clocking requirements and designing the clock distribution and regeneration components.
 - Determining the standard cell and custom library elements needed to completely do the design with APR tools.

Project Review

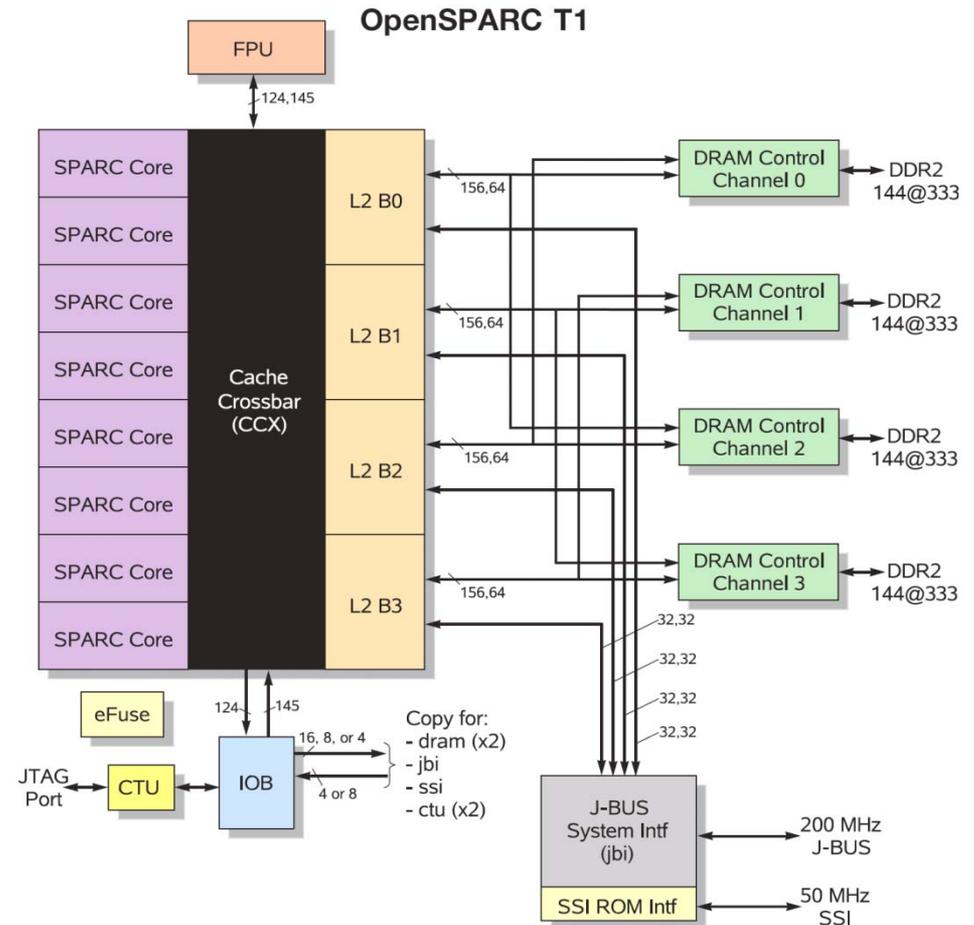
- **There will be a full blown design review of your designs during the last 3 weeks of class.**
- **This review will determine 30% of your final grade.**

VLSI-2 Project: OpenSPARC T1 Core

Spring 2008

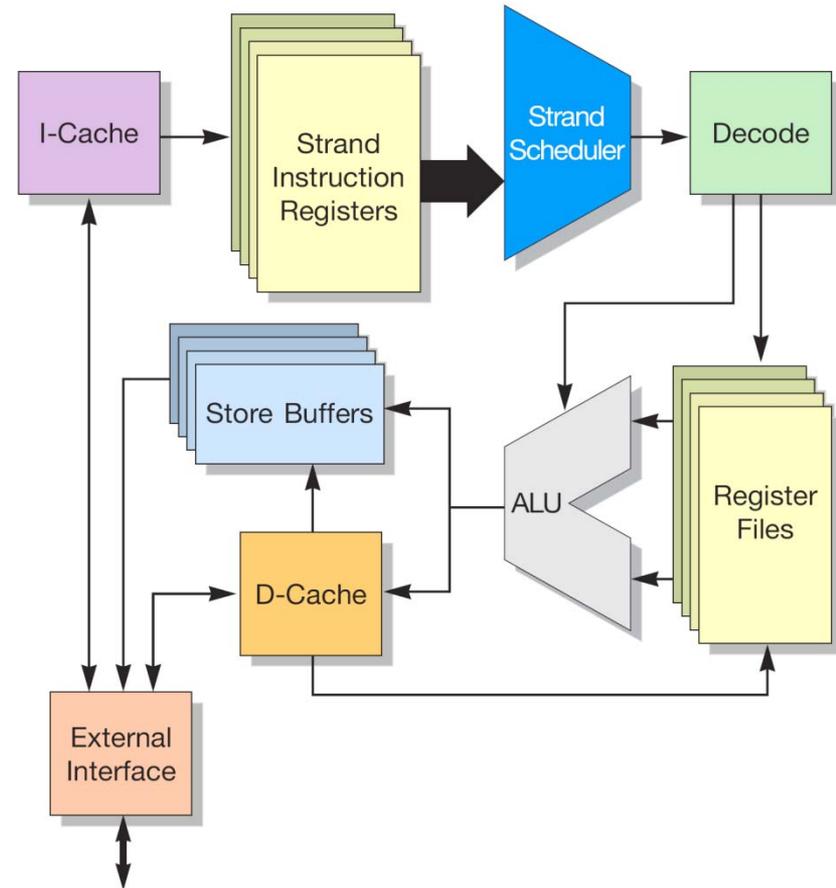
OpenSPARC T1

- One of eight SPARC V9 cores
- Capable of handling 4 threads
- Interfaces to four L2 caches via processor crossbar
- Single FPU shared between eight cores via crossbar



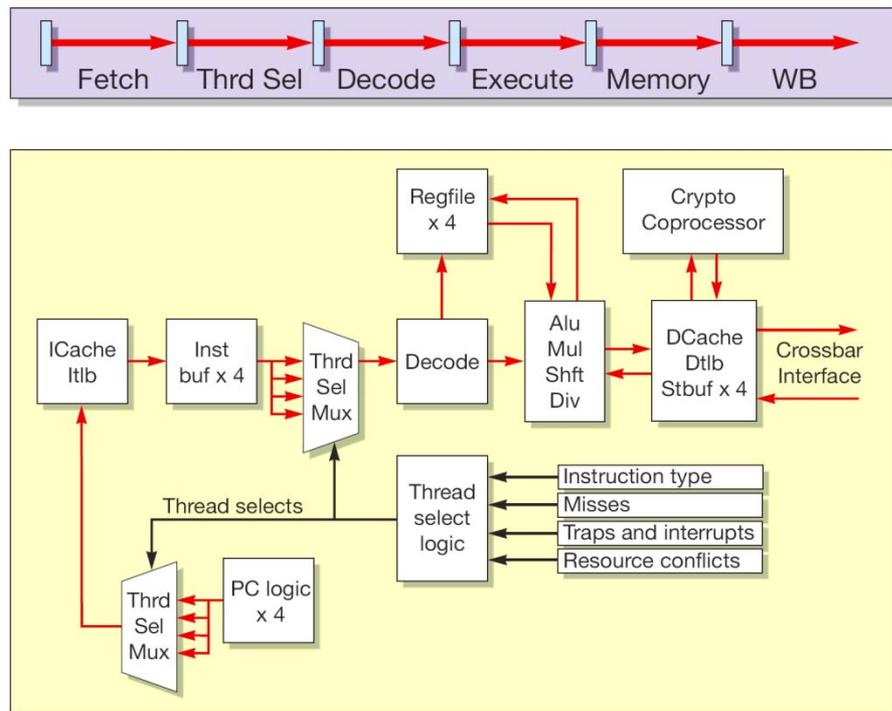
OpenSPARC T1 Core Units

- **Instruction Fetch Unit**
- **Execution Unit**
- **Load/Store Unit**
- **Trap Logic Unit**
- **Memory Management Unit**
- **Floating Point Front-End Unit**
- **Stream Processing Unit**



OpenSPARC T1 Core Pipeline

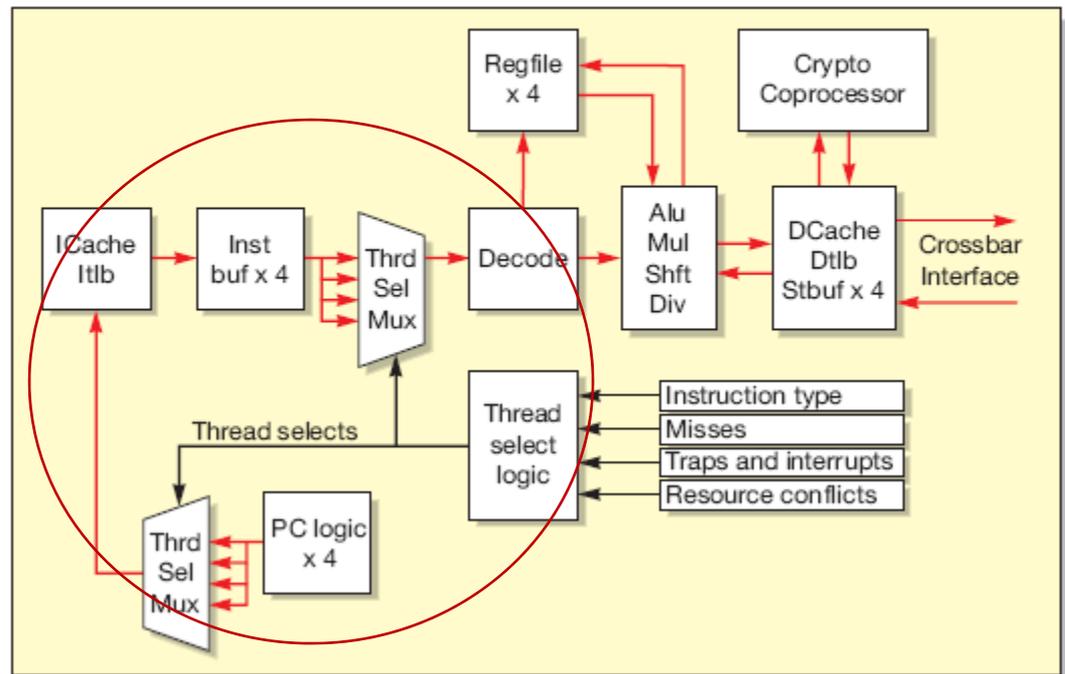
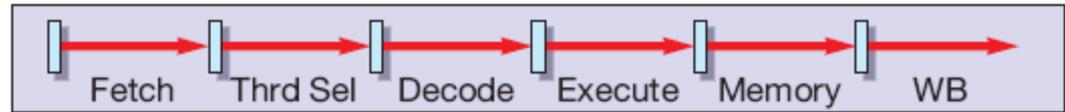
- 6 stage pipeline
- 4 threads per core
- Crypto Coprocessor obtains instructions from IFU (not shown)
- FP Front-end Unit obtains instructions from IFU (not shown)



IFU Block Diagram

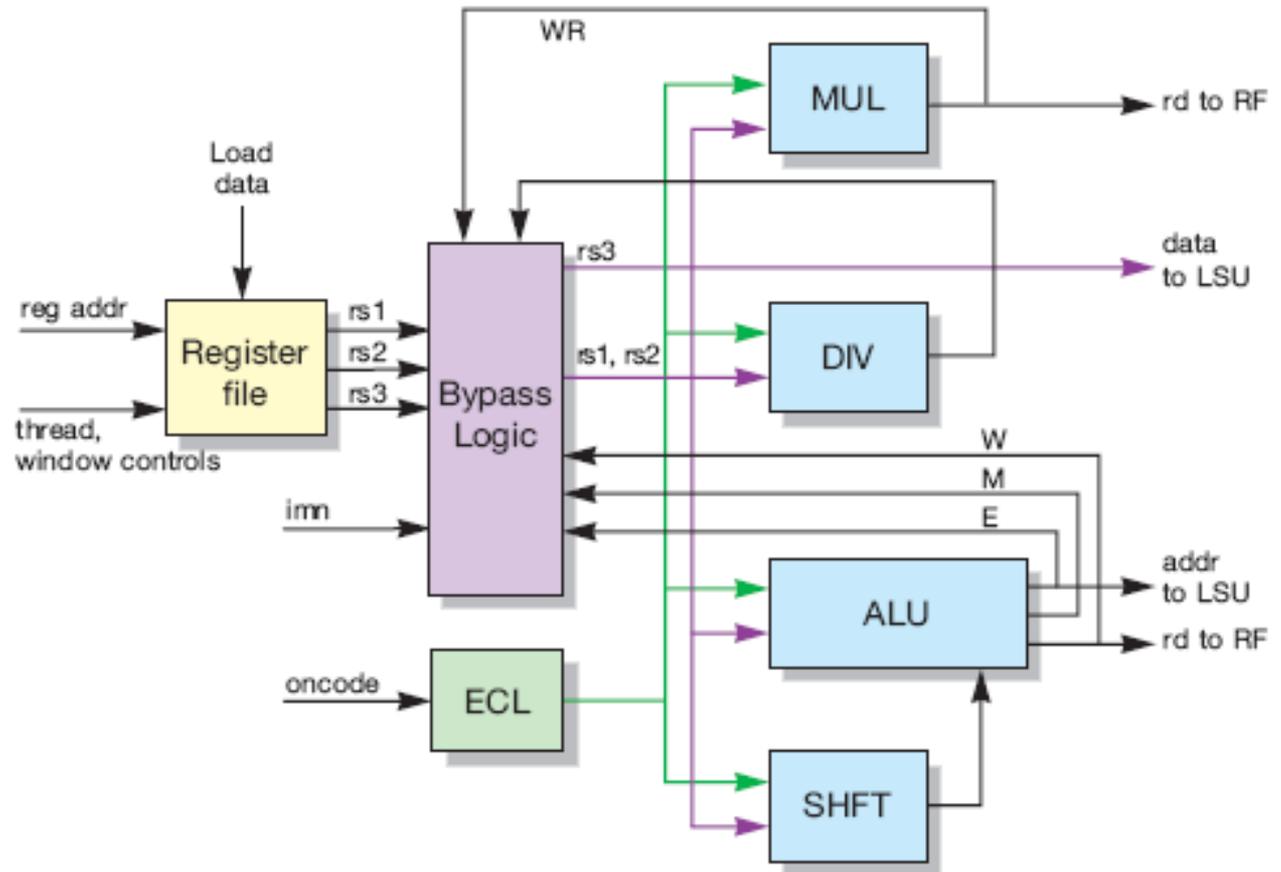
- IFU includes pipeline stages:

- Fetch
- Thread Selection
- Decode



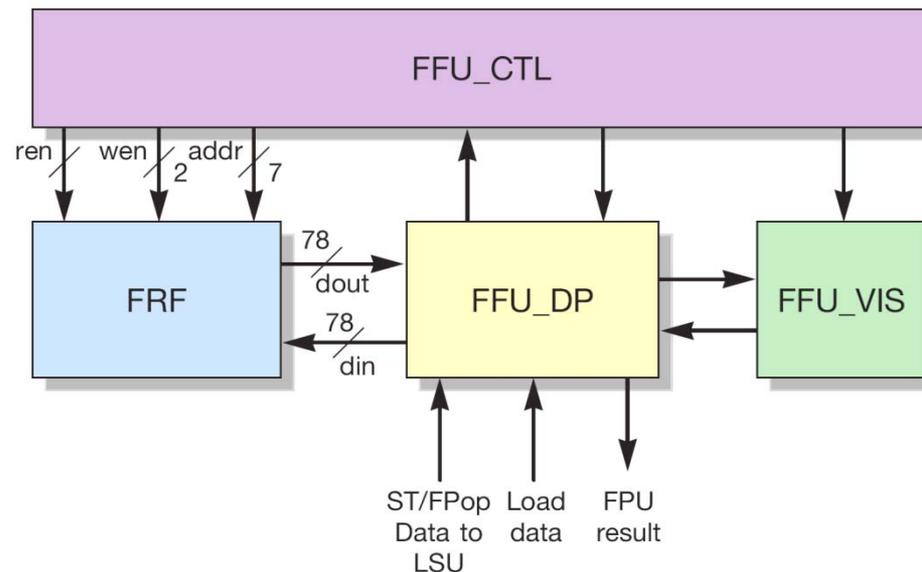
EXU Block Diagram

- Register File
- Bypass Logic
- ECL
- ALU
- MUL
- DIV
- SHFT



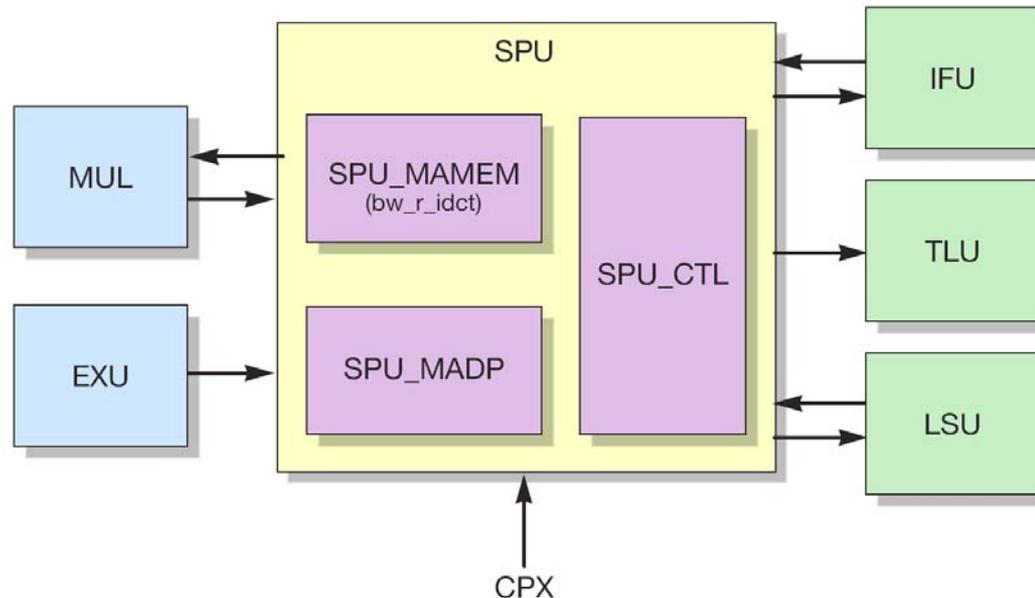
FFU Block Diagram

- Decode and dispatch Floating-point operations to Floating-Point Unit (FPU) via LSU.
- Contains Floating-Point Register File
- Maintains Floating-Point State Register (FSR)



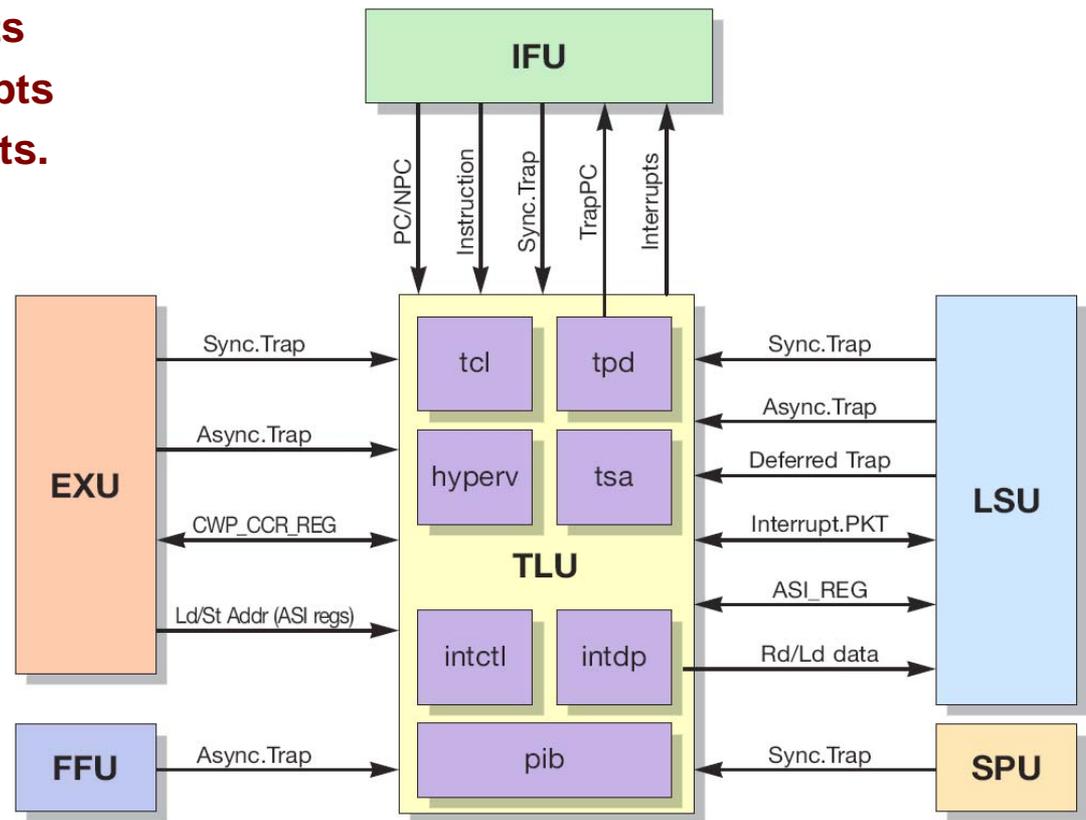
SPU Block Diagram

- Each SPARC core is equipped with a stream processing unit (SPU) supporting the asymmetric cryptography operations (public-key RSA) for up to a 2048-bit key size.
- The SPU shares the integer multiplier with the execution unit (EXU) for the modular arithmetic (MA) operations. The SPU itself supports full modular exponentiation.



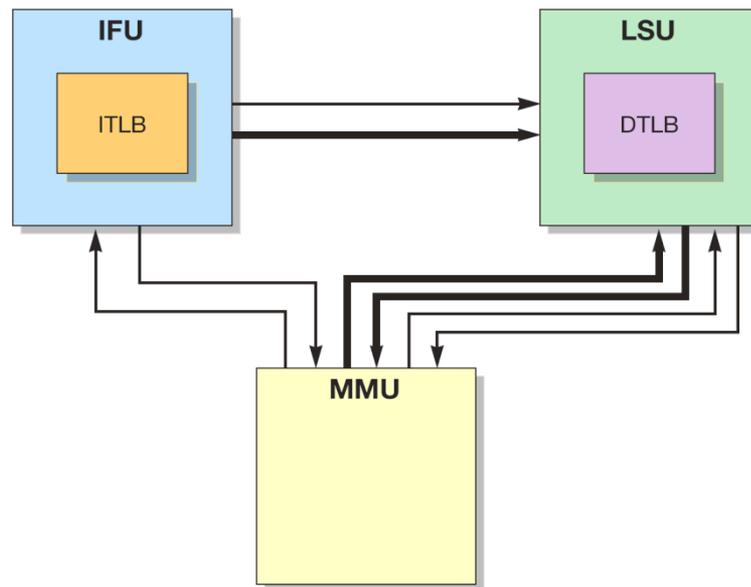
TLU

- The TLU maintains the Trap Logic and Trap Program Counter.
- The TLU handles all interrupts
 - This includes:
 - External interrupts
 - Inter-core interrupts
 - Software interrupts.



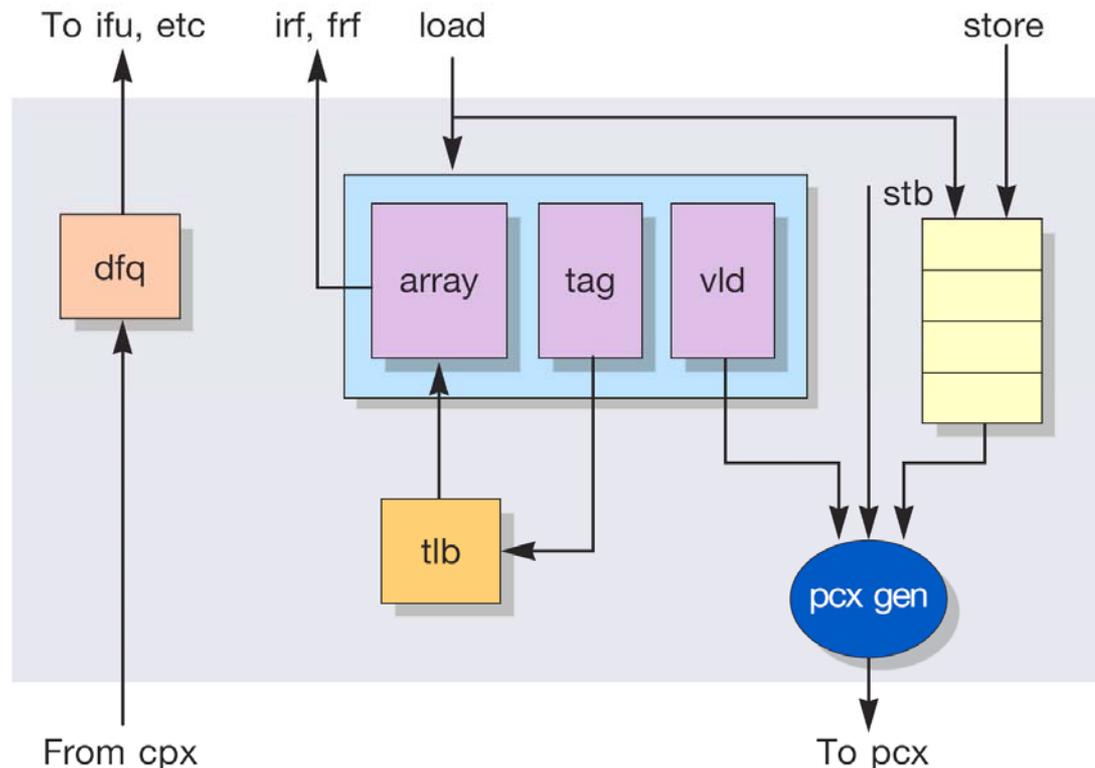
MMU Block Diagram

- **Maintains the contents of ITLB (IFU), DTLB (LSU).**
 - All TLBs shared by threads, consistency among the TLB entries is maintained through demap.
 - MMU generates pointers to the software translation storage buffers (TSB), and fault status of various traps.



LSU Block Diagram

- The threaded architecture of the LSU can process four loads, four stores, one fetch, one FP operation, one stream operation, one interrupt, and one forward packet. (13 Sources supply data to the LSU)



Team assignments

- **Block Distribution**
 - **FFU : 2 students**
 - **MUL : 2 students**
 - **SPU : 2 students**
 - **Caches : 2 - 4 students**
 - **TLBs : 2 - 3 students**
 - **Register Files : 3 - 4 students**
 - **MMU : 2 students**
 - **TLU : 3 students**
 - **EXU: 2 students**
 - **IFU: 3 students**
 - **LSU: 4 students**

Team Assignments (contd.)

- **Integration**
 - **LSU integration - 1 student**
 - Liaison with other integrators and determine connectivity, interdependence, datapath requirements, etc. Also run some placement within block boundary as well as look at clock requirements
 - **EXU integration - 1 student**
 - Same as above but only for EXU block
 - Also need to tend to MUL and SPU block
 - **IFU integration - 1 student**
 - **Global Timing - 2 students**
 - **Global Clocks & Reset - 2 students**
 - **EDA Tool Support – 1-2 students**
 - Support existing tools & scripts
 - Develop new scripts as needed

Team Assignments (contd.)

- **Integration (contd.)**
 - **Power Grid & Estimation - 2 students**
 - **Library Team - 3 students**
 - **Need to verify and support library**
 - **Also assist in developing cells as needed**
 - **Global Floorplanning and Integration**
 - **1 or 2 students**
 - **Strong computer architecture background necessary**