ADC Architectures VI: Folding ADCs

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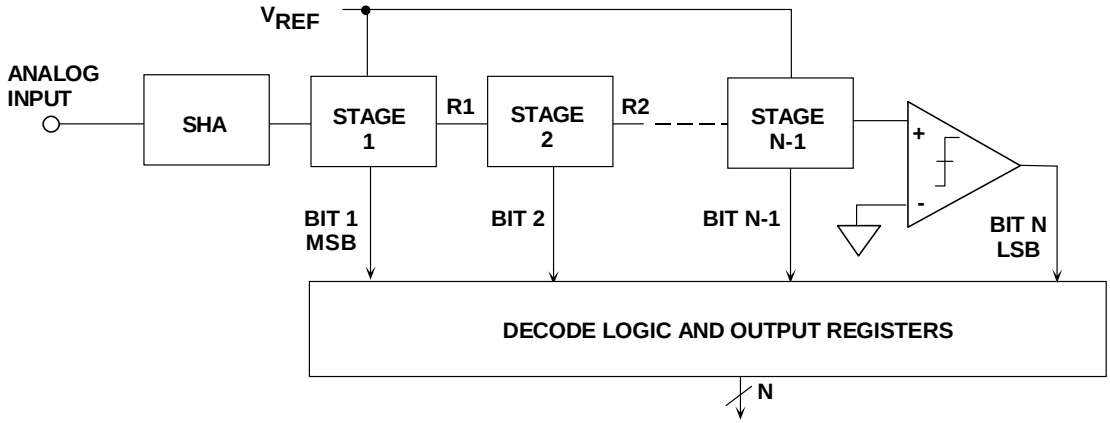
INTRODUCTION

The "folding" architecture is one of a number of possible serial or bit-per-stage architectures. Various architectures exist for performing A/D conversion using one stage per bit, and the overall concept is shown in Figure 1. A multistage pipelined subranging ADC with one bit per stage and no error correction is basically a bit-per-stage converter. In practice, this type of pipelined converter generally uses a 1.5 bit per stage approach to provide error correction (this is discussed in more detail in Reference 1).

In the bit-per-stage ADC, the input signal must be held constant during the entire conversion cycle. There are N stages, each of which have a "bit" output and a "residue" output. The residue output of one stage is the input to the next. The last bit is detected with a single comparator as shown.



B. D. Smith, "An Unusual Electronic Analog-Digital Conversion Method,"
***IRE Transactions on Instrumentation*, June 1956, pp. 155-160.**

Figure 1: Generalized Bit-Per-Stage ADC Architecture

It is possible to combine the bit-per-stage architecture with other architectures. For example, the residue output of the final stage can be further digitized by a flash converter, thereby providing more resolution.

One of the first references to these architectures appeared in an article by B. D. Smith in 1956 (Reference 2). Smith indicates, however, that previous work had been done at M.I.T. by R. P. Sallen in a 1949 thesis. In the article, Smith describes both the binary and the Gray (or folding) transfer functions required to implement the A/D conversion.

BINARY AND FOLDING BIT-PER-STAGE (SERIAL) ADCs

The basic stage for performing a single binary bit conversion is shown in Figure 2. It consists of a gain-of-two amplifier, a comparator, and a 1-bit DAC (changeover switch). Assume that this is the first stage of the ADC. The MSB is simply the polarity of the input, and that is detected with the comparator which also controls the 1-bit DAC. The 1-bit DAC output is summed with the output of the gain-of-two amplifier. The resulting residue output is then applied to the next stage. In order to better understand how the circuit works, the diagram shows the residue output for the case of a linear ramp input voltage which traverses the entire ADC range, $-V_R$ to $+V_R$. Notice that the polarity of the residue output determines the binary bit output of the next stage.

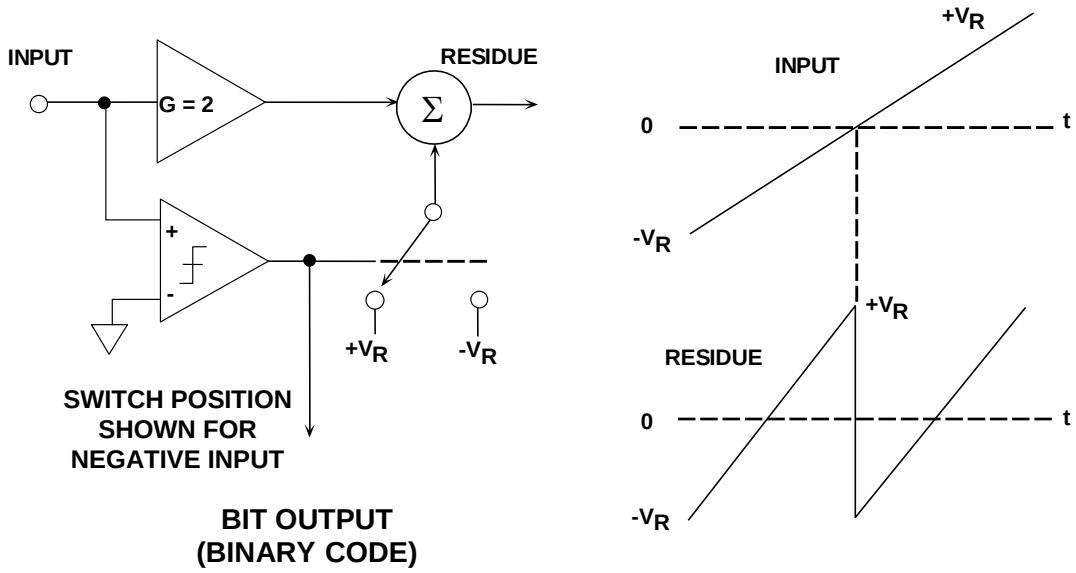


Figure 2: Single-Stage Transfer Function for Binary ADC

A simplified 3-bit serial-binary bit-per-stage ADC is shown in Figure 3, and the residue outputs are shown in Figure 4. Again, the case is shown for a linear ramp input voltage whose range is between $-V_R$ and $+V_R$. Each residue output signal has discontinuities which correspond to the point where the comparator changes state and causes the DAC to switch. The fundamental problem with this architecture is the discontinuity in the residue output waveforms. Adequate settling time must be allowed for these transients to propagate through all the stages and settle at the final comparator input. As presented here, the prospects of making this architecture operate at high speed are dismal. However using the 1.5-bit-per stage pipelined architecture (see Reference 1) makes it much more attractive at high speeds.

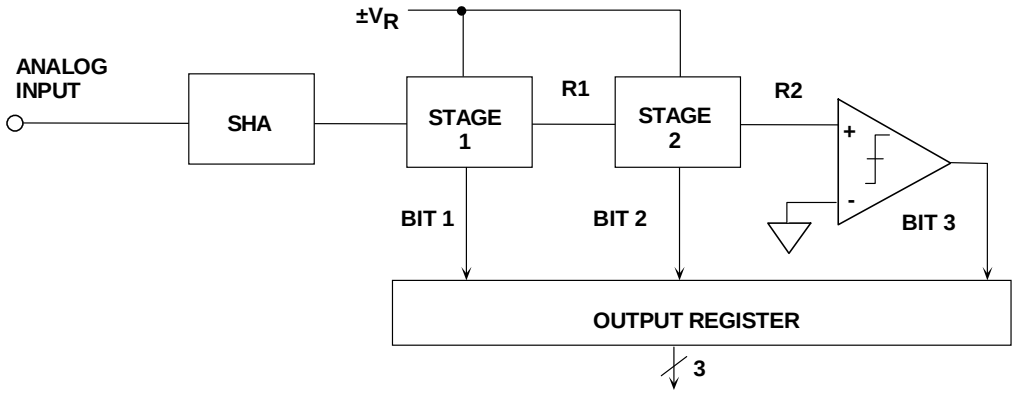


Figure 3: 3-bit Serial ADC with Binary Output

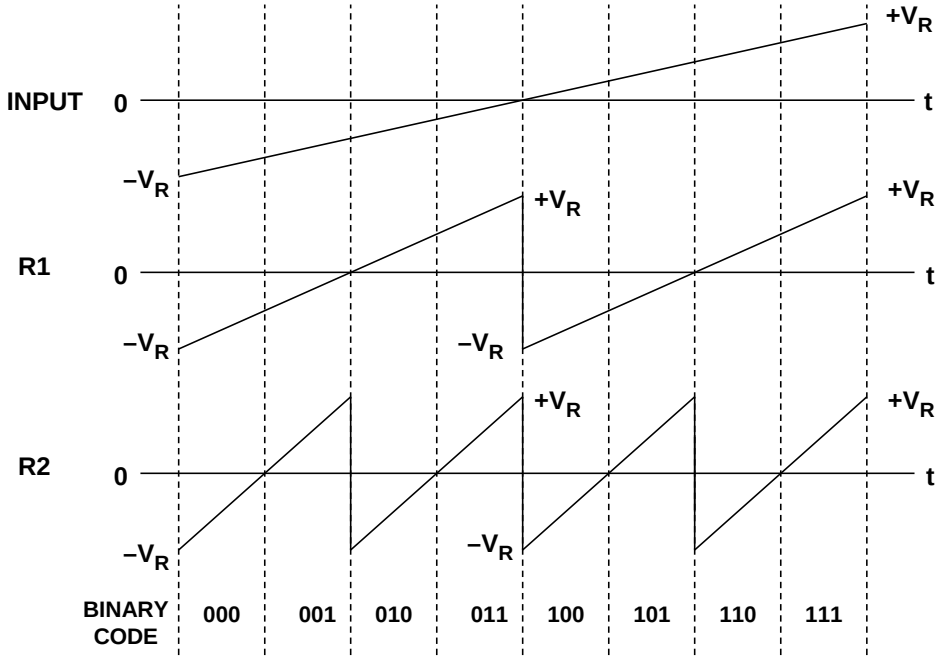


Figure 4: Input and Residue Waveforms of 3-Bit Binary Ripple ADC

Although the binary method is discussed in his paper, B. D. Smith also describes a much preferred bit-per-stage architecture based on absolute value amplifiers (magnitude amplifiers, or simply *MagAMPs*™). This scheme has often been referred to as *serial-Gray* (since the output coding is in Gray code), or *folding* converter because of the shape of the transfer function. Performing the conversion using a transfer function that produces an initial Gray code output has the advantage of minimizing discontinuities in the residue output waveforms and offers the potential of operating at much higher speeds than the binary approach.

The basic folding stage is shown functionally in Figure 5 along with its transfer function. The input to the stage is assumed to be a linear ramp voltage whose range is between $-V_R$ and $+V_R$. The comparator detects the polarity of the input signal and provides the Gray bit output for the stage. It also determines whether the overall stage gain is +2 or –2. The reference voltage V_R is summed with the switch output to generate the residue signal which is applied to the next stage. The polarity of the residue signal determines the Gray bit for the next stage. The transfer function for the folding stage is also shown in Figure 5.

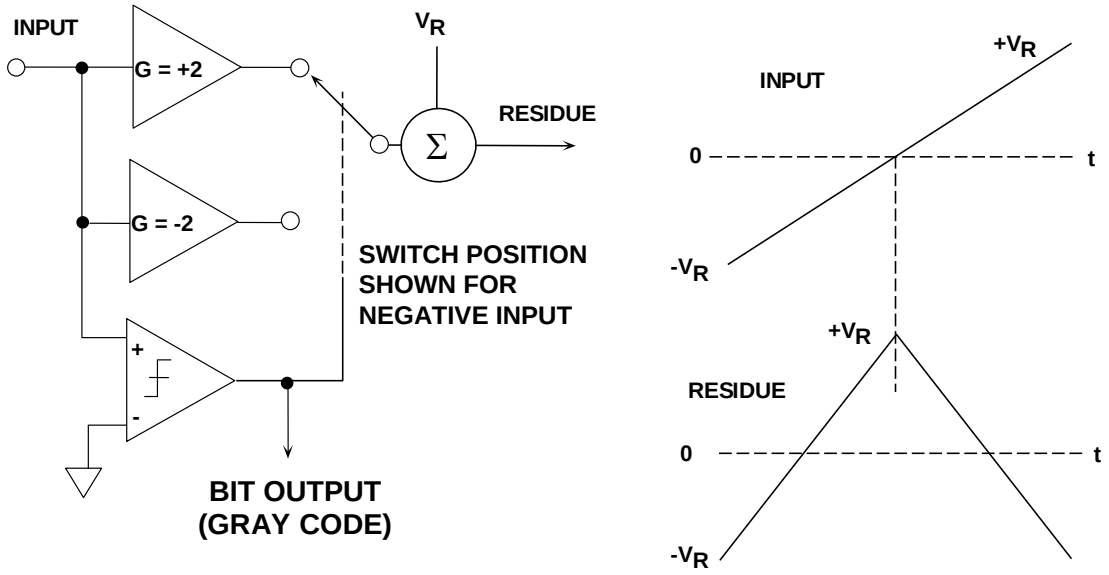


Figure 5: Folding Stage Functional Equivalent Circuit

A 3-bit MagAMP folding ADC is shown in Figure 6, and the corresponding residue waveforms in Figure 7. As in the case of the binary bit-per-stage ADC, the polarity of the residue output signal of a stage determines the value of the Gray bit for the next stage. The polarity of the input to the first stage determines the Gray MSB; the polarity of R1 output determines the Gray bit-2; and the polarity of R2 output determines the Gray bit-3. Notice that unlike the binary ripple ADC, there is no abrupt transition in any of the folding stage residue output waveforms. This makes operation at high speeds quite feasible.

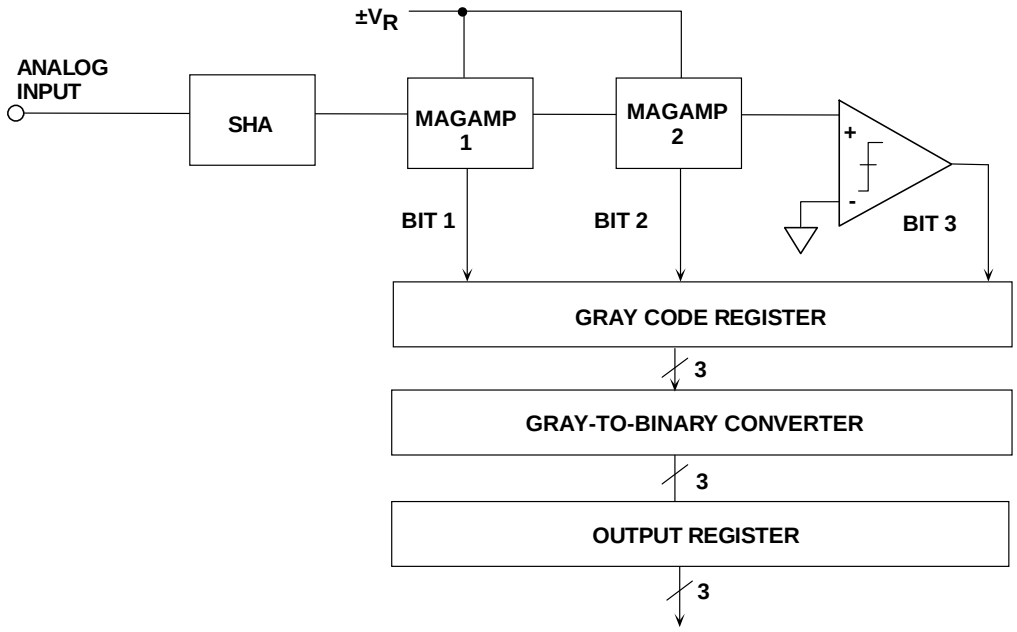


Figure 6: 3-bit Folding ADC Block Diagram

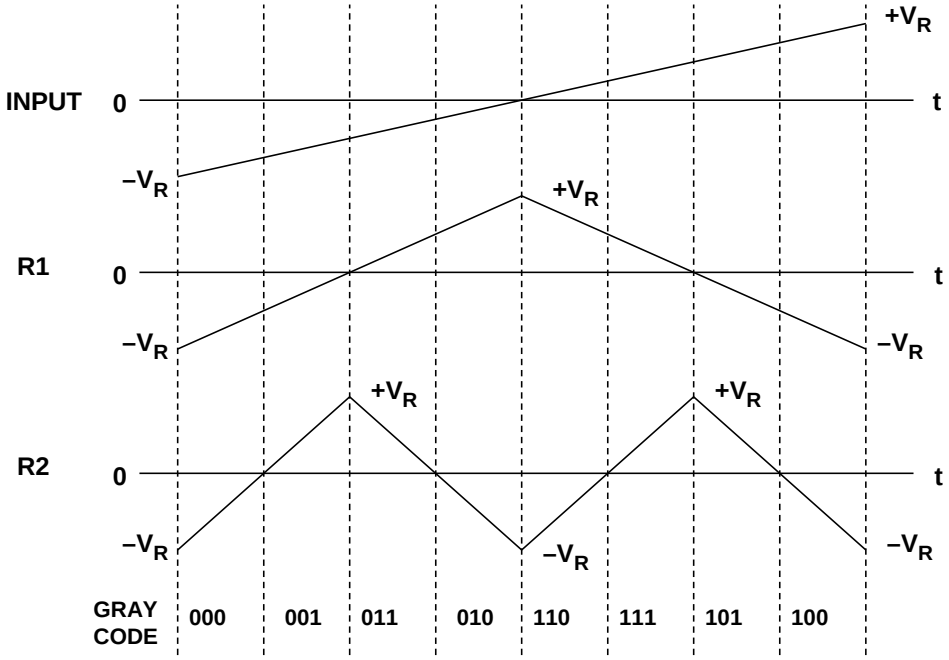
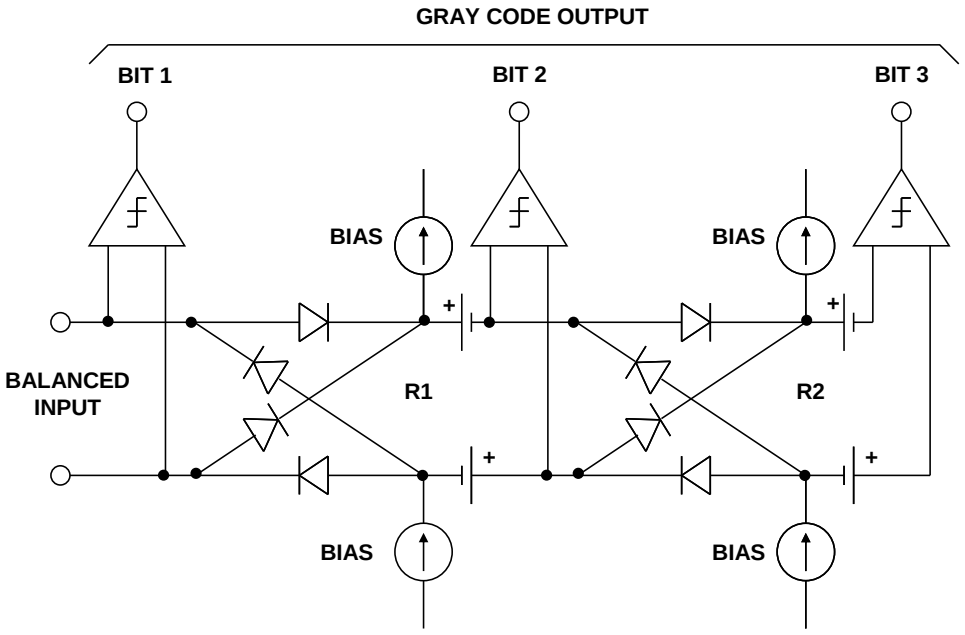


Figure 7: Input and Residue Waveforms for 3-Bit Folding ADC

The key to operating this architecture at high speeds is the folding stage. N. E. Chasek of Bell Telephone Labs describes a circuit for generating the folding transfer function using nested diode bridges in a patent filed in 1960 (Reference 3). This circuit made use of solid-state devices, but required different reference voltages for each stage (see Figure 8). Chasek's circuit also suffered from loss of headroom and gain when several stages were cascaded to form higher resolution

converters as shown in Figure 9. What is really needed to make the folding ADC work at high resolutions is nearly ideal voltage or current rectification.



Adapted from: N. E. Chasek, "Pulse Code Modulation Encoder,"
U.S. Patent 3,035,258, Filed November 14, 1960, Issued May 15, 1962

Figure 8: 3-Bit Folding ADC Based on N. E. Chasek's Design

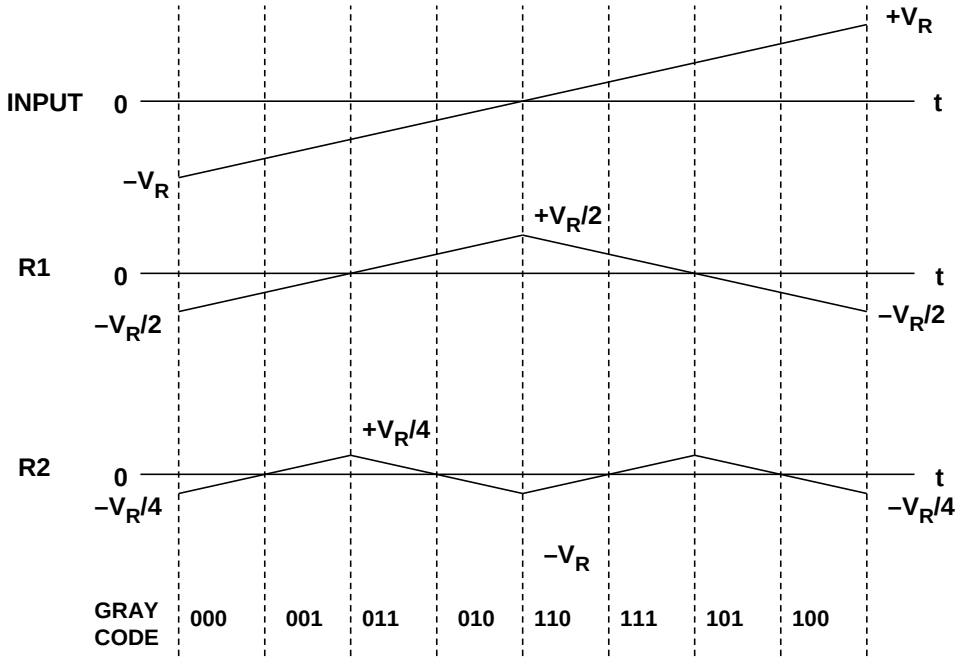
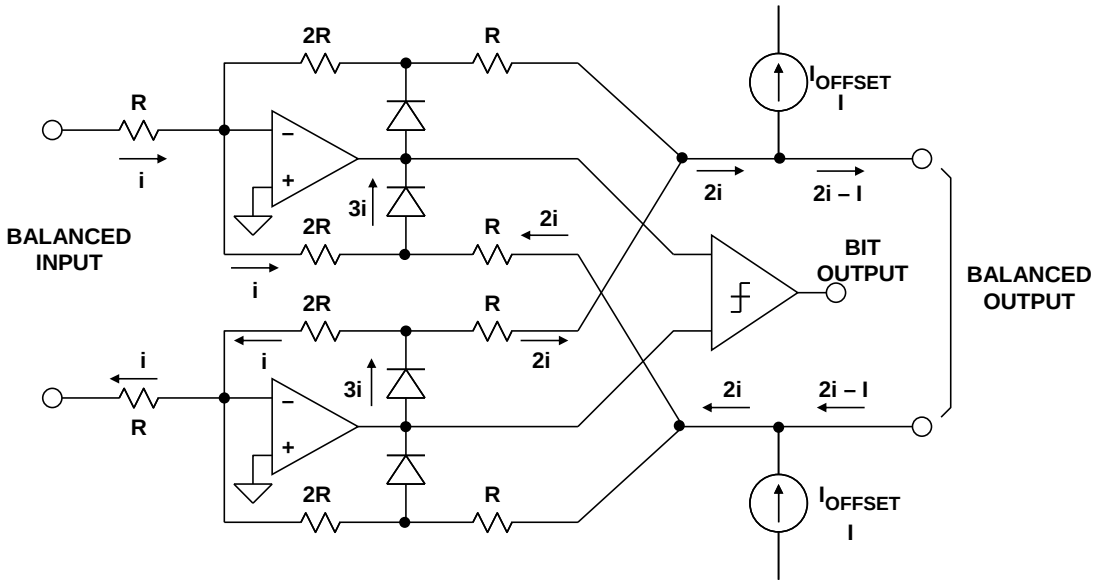


Figure 9: Single-Ended Waveforms in Chasek's Folding ADC

F. D. Waldhaur of Bell Telephone Labs remedied the problems of Chasek's nested diode bridge circuits in a classic patent filed in 1962 (Reference 4). Figure 10 shows Waldhaur's elegant implementation of the folding transfer function using solid state op amps with diodes in the feedback loop. The gain-of-two op amps allow the same reference voltages to be used for each stage and maintain the same signal level at each residue output with nearly ideal rectification.



Extracted from: F. D. Waldhauer, "Analog-to-digital Converter,"
***U.S. Patent 3,187,325*, Filed July 2, 1962, Issued June 1, 1965**

Figure 10: F. D. Waldhaur's Classic Folding Stage using Rectifier Amplifiers

J. O. Edson and H. H. Henning describe the operation and performance of this type of ADC in greater detail in a 1965 *Bell System Technical Journal* article (Reference 5). An operational 9-bit, 6-MSPS ADC of this type was used in experimental studies on 224-Mbit/second PCM terminals. These terminals were supposed to handle data as well as voice signals. The voiceband objective was to digitize an entire 600-channel, 2.4-MHz FDM band, therefore requiring a minimum sampling rate of approximately 6 MSPS.

It is interesting to note that the experimental terminal was also supposed to handle video as well, which required a higher sampling rate of approximately 12-MSPS. For this requirement, the latest (and final) generation Bell Labs' electron beam coder (see Tutorial MT-020) was needed to meet the ADC requirement, as the solid-state coder based on Waldhaur's patent did not have the necessary accuracy at the higher sampling rates.

The first commercial ADC using Waldhaur's Gray code architecture was the 8-bit, 10-MSPS HS-810 from Computer Labs, Inc., in 1966. The instrument used all discrete transistor circuits (no ICs) and was designed to be mounted in a 19" rack as shown in Figure 11 for an early experimental digital radar receiver application. The 8-bit, 10-MSPS converter contained its own linear power supply, dissipated nearly 150 watts, and sold for approximately $10,000. The same technology was used to produce 9-bit, 5-MSPS and 10-bit 3-MSPS versions. Although the next

generation of Computer Labs' designs would take advantage of modular op amps (Computer Labs OA-125 and FS-125), ICs such as the Fairchild µA710/711 comparators, as well as 7400 TTL logic, the first ADCs offered used all discrete devices. These early high speed ADCs produced by Computer Labs were primarily used in research and development projects associated with radar receiver development by companies such as Raytheon, General Electric, and MIT Lincoln Labs.

19" RACK-MOUNTED, 150W, $10,000.00

INSTALLATION OF 12 ADCs IN EXPERIMENTAL DIGITAL RADAR RECEIVER

Figure 11: HS-810, 8-bit, 10-MSPS ADC Released by Computer Labs, Inc. in 1966

The folding Gray code architecture was used in a few instrument and modular ADCs in the early 1970s, such as the HS-810, but commercial high speed ADCs primarily used either the flash or the error-corrected subranging architecture in the 1980s. With improvements in IC processes, there was, however, continued interest in the folding architecture in the late 1970s and throughout the 1980s—with quite a number of experimental designs reported in the various journals over the period (References 6-10).

Analog Devices developed the first high speed fully complementary bipolar (CB) process in the mid-1980s, and in 1994 Frank Murden and Carl Moreland filed patents on a significantly improved current-steering architecture for a Gray code MagAMP™-based ADC (References 11-15). The technique was first implemented for building block cores in the AD9042 12-bit, 41-MSPS ADC released in 1995, and refinements of the technique and a higher speed CB process, XFCB, (References 16 and 17) pushed the core technology to 14-bits with the release of the AD6644 14-bit 65-MSPS ADC in 1999, the AD6645 14-bit 80-MSPS ADC in 2001, and a 105-MSPS version of the AD6645 in 2003. Although these ADCs use the error-corrected pipelined subranging architecture, the internal building block core ADCs utilize the MagAMP™ architecture.

Modern IC circuit designs implement the transfer function using current-steering open-loop gain techniques which can be made to operate much faster. Fully differential stages (including the SHA) also provide speed, lower distortion, and yield 8-bit accurate folding stages with no requirement for thin film resistor laser trimming.

An example of a fully differential gain-of-two MagAMP folding stage is shown in Figure 12 (see References 11, 12, 14). The differential input signal is applied to the degenerated-emitter differential pair Q1,Q2 and the comparator. The differential input voltage is converted into a differential current which flows in the collectors of Q1, Q2. If +IN is greater than –IN, cascode-connected transistors Q3, Q6 are on, and Q4, Q6 are off. The differential signal currents therefore flow through the collectors of Q3, Q6 into level-shifting transistors Q7, Q8 and into the output load resistors, developing the differential output voltage between +OUT and –OUT. The overall differential voltage gain of the circuit is two.

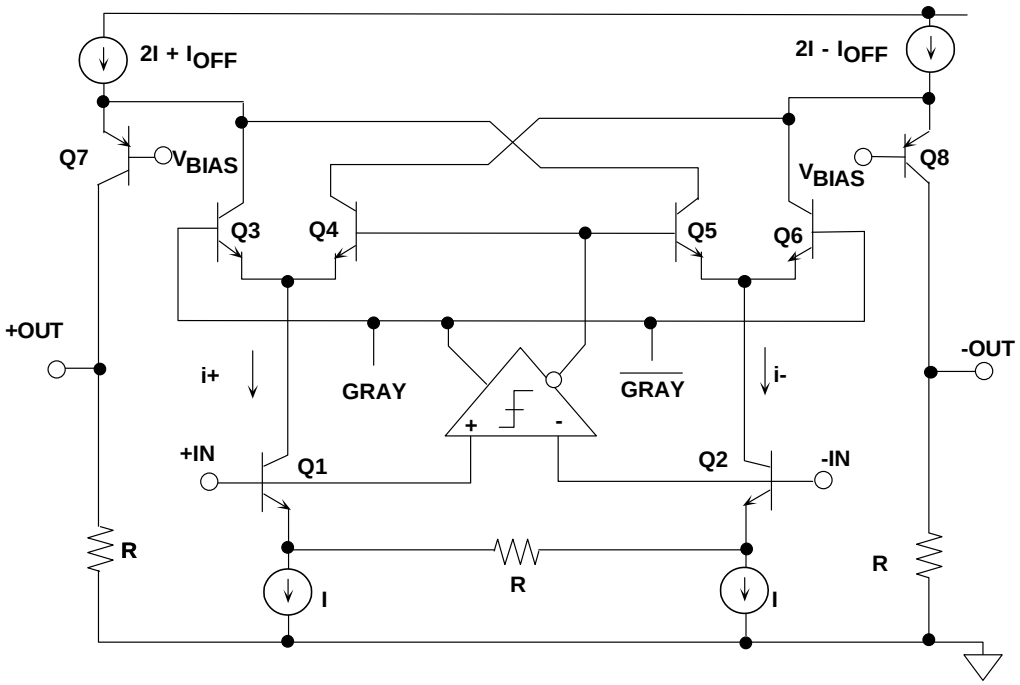


Figure 12: A Modern Current-Steering MagAMP™ Stage

If +IN is less than –IN (negative differential input voltage), the comparator changes state and turns Q4, Q5 on and Q3, Q6 off. The differential signal currents flow from Q5 to Q7 and from Q4 to Q8, thereby maintaining the same relative polarity at the differential output as for a positive differential input voltage. The required offset voltage is developed by adding a current I_{OFF} to the emitter current of Q7 and subtracting it from the emitter current of Q8.

The differential residue output voltage of the stage drives the next stage input, and the comparator output represents the Gray code output for the stage.

The MagAMP architecture offers lower power and can be extended to sampling rates previously dominated by flash converters. For example, the AD9054A 8-bit, 200-MSPS ADC is shown in Figure 13 and was first introduced in 1997. The device is fabricated on a high speed complementary bipolar process, and power dissipation is 500 mW. The first five bits (Gray code) are derived from five differential MagAMP stages. The differential residue output of the fifth MagAMP stage drives a 3-bit flash converter, rather than a single comparator.

The Gray-code output of the five MagAMPs and the binary-code output of the 3-bit flash are latched, all converted into binary, and latched again in the output data register. Because of the high data rate, a demultiplexed output option is provided.

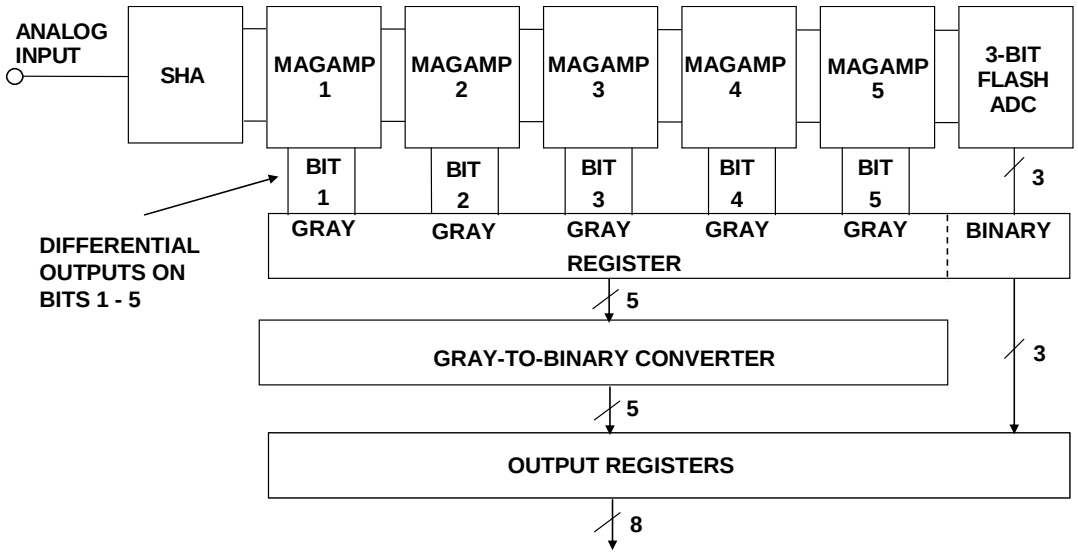


Figure 13: AD9054A 8-bit, 200-MSPS ADC Introduced in 1997

Recent introductions in the 8-bit high speed area have utilized CMOS processes and the pipelined subranging architecture, such as the 8-bit 250 MSPS, AD9480 (LVDS outputs) and AD9481 (demuxed CMOS outputs) which dissipate 700 mW and 600 mW, respectively.

SUMMARY

Although initially used in pioneering instrument ADCs at Bell Labs and Computer Labs in the 1960s, the flash the pipelined subranging architectures have dominated the high speed ADC marketplace. Although there have been a number of ICs designed using the folding architecture, it has never attained the popularity of the pipelined subranging ADC. Nevertheless, it is important to know that it exists because it may regain popularity in the future as IC processes evolve.

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3. N. E. Chasek, "Pulse Code Modulation Encoder," *U.S. Patent 3,035,258*, filed November 14, 1960, issued May 15, 1962. *(an early patent showing a diode-based circuit for realizing the Gray code folding transfer function).*

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