QUIESCENT CURRENT CONTROL CIRCUIT FOR CLASS AB

AMPLIFIERS

BY

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ABSTRACT

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Among the several types of amplifiers in analog design, we find the Class AB amplifier. In this type of amplifier, the quiescent bias current in the output devices has a major impact in the power dissipation. Controlling the bias current represents a major limitation, as it depends on other characteristics in the circuit. The motivation of this dissertation is to develop a new technique to control the quiescent current in the output transistors. This technique consists in making a replica of part of the circuit and having it operate under static conditions to

obtain the desired quiescent current for the output transistors. This is achieved with few additional devices.

The implementation of this technique in several Class AB designs is discussed. Also the Class AB performance of the amplifiers and the accurate control of the current in the output stage is analyzed to validate the operation of the implementation of this technique. In addition, a comparison between the performance of these designs is analyzed when used in different practical systems. To test the performance we needed systems that represent a low-impedance or a high-capacitive load. For this purpose we used an R-2R Digital-to-Analog Converter, a charge redistribution Digital-to-Analog Converter and a headphone speaker.

Simulations and experimental results show that Class AB operation is achieved with accurate quiescent current control when this technique is implemented in three different designs. These designs include, a transconductance amplifier, a conventional opamp using a battery as a level shift in the output devices, and a conventional Class AB buffer without bias current control. The implementation of this technique shows that some designs enhance the slew rate in a factor 5 compared to the conventional two-stage amplifier. They also enhance dramatically the output impedance by a factor 16500 compared to the conventional amplifier.

Simulation and experimental results from prototypes fabricated in a CMOS

0.5μm technology are provided to validate the performance of the proposed tech-

nique.

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1 INTRODUCTION

Circuit design has evolved very rapidly with technology in the past few decades. This evolution includes every branch of the electronics field. In the digital field, this evolution includes Digital Signal Processing (DSP), data compression for audio and video to achieve faster and more accurate processing of information, as well as higher integration of peripherals for embedded systems. The analog domain has evolved to achieve higher linearity and higher frequency of operation in filters, and reduced power consumption and voltage supply in power amplifiers.

Downscaling of CMOS processes has forced analog circuits to operate with continuously decreasing supply voltages and power consumption. On the other hand, in order to be compatible with higher speed digital circuits, analog circuits need to have better performance, in particular higher speed, wider input range and greater linearity. Many approaches have been developed to achieve these goals in op-amps and operational transconductance amplifiers (OTA) such as complementary differential pairs, folding transistors, floating gates and current-mode processing.

Another major concern for the analog designer is to develop circuits with lower power dissipation which helps to extend the battery life for consumer electronics. It is also an important requisite in implantable medical devices. Several schemes have been reported to reduce supply voltage requirements of a circuit,

such as operating CMOS transistors in the triode mode or the subthreshold region, applying floating gate techniques, applying bulk-driven techniques, using self-cascode techniques and processing signals in the current domain.

Opamps are one of the most popular basic cells in analog design. They are used in many applications, such as Digital-to-Analog converters and RF receivers and transmitters. Yet there is another type of amplifier which is becoming more popular: the transconductance amplifier, which gets its name by the ratio of its output current to input voltage. Some authors refer to them as Operational Transconductance Amplifiers (OTAs). These amplifiers, accompanied by current mirrors, have become equally important cells for integrated analog design. Several applications of the OTA require low-voltage operation, highly-linear transconductance and high input range, as they are used in open-loop structures with large differential input signals.

Many variations of output stages used in opamps and OTA's have been reported in the past. In these types of amplifiers authors address problems, such as lowering the impedance at the output node in order to drive high capacitive or low resistive loads, decreasing the power consumption to increase the efficiency, reducing the effect of channel length modulation and/or increasing the open-loop gain, among others. The intention of output stages is to use them as buffers in order to drive high capacitive or low resistive loads without causing distortion in the processing of a signal from previous stages.

Chapter 2 describes the design and operation of some of the output stages that have been developed in the past, as well as their advantages and disadvantages. Also, a comparison between the attributes of these amplifiers is provided. Certain characteristics are highlighted, such as the extremely high efficiency of the Class D amplifier and the very low distortion of the Class A amplifier.

Among these types of amplifiers we find the Class AB amplifier, described in Section 2.3, which has the capability to sink and source large currents at the output node. This type of amplifier offers a very high and symmetrical slew rate. An important challenge of the Class AB amplifier is the biasing of the output stage, usually composed of a PMOS sourcing device and an NMOS sinking device. Typically, setting the static current through the output devices becomes problematic as it depends on other characteristics of the circuit, such as the sizing of the transistors, or the value of the supply voltages.

Chapter 3 explains how this dissertation is focused on developing a technique to control the current of the output devices under static conditions. This technique consists in making a replica of part of the circuit, and having it operate under the desired bias conditions so as to obtain the proper state for the output devices. Although the principle of this technique is the same, the implementation varies for different designs.

Chapter 4 describes the utilization of the biasing technique described in Chapter 3 to implement a control circuit on a two-stage opamp to achieve Class

AB operation in the output stage. In addition, a three-stage opamp with the same quiescent current control technique is presented that achieves a better performance and higher speed.

Chapter 5 explains the technique discussed in Chapter 3 to implement Class AB operation in a two-stage amplifier using a dual-polarity battery, which can adapt to positive and negative values. Positive values accommodate large power supply voltages, whereas negative values are needed for low power supply voltages. Also, the control circuit to maintain constant power dissipation, regardless of the variations in the power supply, is studied.

Chapter 6 describes the implementation of the technique described in Chapter 3 to a Class AB output buffer which consists of two opamps and two complementary common-source transistors. The implementation is based on sensing the current in the output devices and comparing it against a bias current. Two approaches are discussed.

Chapter 7 describes a comparison between all the circuits where this technique was applied. Class AB amplifiers are used due to their capability to provide current when driving a low-resistive or a high capacitive load. Therefore, to test the amplifiers we used an R-2R Digital-to-Analog Converter, a charge redistribution Digital-to-Analog Converter and a headphone speaker. The three-stage amplifiers enhance the performance of the slew rate by a factor 5, whereas the output impedance is enhanced by a factor 165,000, compared to the conventional

amplifier. The two-stage amplifiers enhance the performance of the slew rate by a factor 2, whereas the output impedance is enhanced by a factor 350, compared to the conventional amplifier. A more detailed comparison is discussed in this chapter.

We conclude in Chapter 8 by summarizing the advantages of the proposed circuits and the performance achieved in simulation and experimental results. This chapter also discusses some future work in low-voltage, low-power applications of these cells.

A list of papers based on this dissertation is given below

1. S. Gupta, I. R. Padilla, J. Ramirez-Angulo, A. Torralba and M. Jimenez, "Comparison of Conventional and New Flipped Voltage Follower Structures," *Proc. IEEE Midwest Symposium on Circuits and Systems*, Cincinnati, OH August 21-23 2005.

2. "Low Voltage Rail-to-Rail Operational Amplifier Based on Flipped Voltage Followers," Ivan Padilla, Jaime Ramirez-Angulo, Ramon Carvajal, Antonio Lopez-Martin and Ramon G. Carvajal, *Proc. IEEE Midwest Symposium on Circuits and Systems*, Cincinnati, OH August 21-23 2005.

3. "New Rail-to-Rail Input Stage With Reduced Supply Requirements," Ivan Padilla, Jaime Ramirez-Angulo, Ramon G. Carvajal, Antonio Lopez-Martin. *Proc. XX Conference on Design of Circuits and Integrated Systems DCIS* 2005, November 18-21, 2005, Lisboa, Portugal.

4. I. Padilla-Cantoya, J. Ramrez-Angulo, A. J. Lopez-Martin, and R. G. Carvajal, "Rail-to-Rail Input Stage in Moderate Inversion with Reduced Supply Requirements, High CMRR and Small gm Variations," *Proc. IEEE Transactions on Circuits and Systems I*, (under review), submitted February 10 2006.

5. I. Padilla-Cantoya, J. Ramrez-Angulo, A. J. Lopez-Martin, and R. G. Carvajal, "Compact Implementation of Linear Weighted CMOS Transconductance Adder Based on the Flipped Voltage Follower," *Journal of Analog Integrated Circuits and Signal Processing*, (under review).

6. Ivan Padilla, Jaime Ramirez-Angulo, Ramon Carvajal, and Antonio Lopez-Martin, "Compact Implementation of Linear Weighted CMOS Transconductance Adder Based on the Flipped Voltage Follower," *Proc. IEEE International Symposium on Circuits and Systems*, May 21-24 2006, Kos, Greece.

7. Ivan Padilla, Jaime Ramirez-Angulo, "Highly Linear V/I Converter with Programmable Current Mirrors," *Proc. IEEE International Symposium on Circuits and Systems*, May 27-30 2007 New Orleans, USA, (accepted for presentation.)

2 BACKGROUND

This chapter gives a description of the different types of amplifiers that have been developed, including the classification depending on the common terminal. It also includes a description of power amplifiers, definition of conduction angle and implementations of the various types of amplifiers.

An important term in the classification of amplifiers is the "common" terminal. An amplifier stage is described by the terminal of the active device that is connected to signal ground. Signal ground is either the actual ground terminal, or one of the voltage rails. Some examples are common emitter or common-drain. Note that these names also reflect the type of active device used in the amplifier [1, 2, 3]. For instance, common-emitter refers to an amplifier with a bipolar transistor as the active device, while a common-drain amplifier uses a MOSFET [1]. Many designs have been developed for almost any terminal of any active device connected to signal ground. Each of these offer different characteristics that are appropriate for the application in which they are being used.

Amplifiers can be designed to magnify voltage (voltage amplifier), current (voltage buffer), or both (power amplifier), of a given input signal. Amplifiers can operate having a single supply (V_{dd} and Gnd) or double-sided or balanced supplies (V_{dd} and V_{ss} and Gnd) [3].

The "biasing" of a circuit is the method by which the active devices are set up to operate under static conditions. Typically, the DC value of the output signal is set to the midpoint between the power rails. Many approaches in amplifier design include symmetry so as to match device parameters. Class A amplifiers usually use only one device for the amplification stage. If the design includes both positive and negative rails, two devices may be included. Class C amplifiers, by definition, use a single polarity supply.

Amplifiers are often designed to have multiple stages connected in series to increase the overall gain. Some designs include stages of different types to obtain the advantages of each stage.

The letter assigned to each of the types of amplifiers is related to its design. The various designs are distinguished according to the relationship between the input and output signals, as well as the relative amount of time the amplifying device is used to conduct. This time is measured in degrees of duration of a sine wave test signal applied to the input of the amplifier, where 360 degrees represents one full cycle. This is known as the conduction angle [4,5,6], and it is defined for each of the amplifiers presented in this document in the following sections. The efficiency of the amplifier has a strong correlation to its conduction angle. Section 2.7 is dedicated to describe how to obtain the efficiency of the amplifiers based on the conduction angle.

Amplifiers can be implemented using transistors of various types such as Bipolar Junction Transistors (BJT) and Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET), among others [1]. When a signal is applied to the input terminal of an active device (base or gate), this causes a proportional output current to flow through the output terminal. This output current is obtained from the power supply. A very commonly used type of amplifier is the common emitter (BJT) or the common source (MOSFET) which amplifies and inverts the input signal. If the amplifying device is linear, then the output is an accurate copy of the input signal. In practice, transistors are non-linear active devices. These non-linearities lead to distortion in the output signal.

2.1   CLASS A

Fig. 2.1 shows the basic configuration of a Class A amplifier [1,4,7]. These circuits amplify the entire cycle of the input signal, so as to have a replicated version at the output multiplied by a scaling factor; therefore, the conduction cycle of this amplifier is 360°. This type of amplifier is very common for small-input signal applications. The efficiency is poor, it has a theoretical efficiency of 50% [7], but for small input signals the power consumption is extremely small. Therefore, their use is permitted in some designs. If the application requires an output with high voltage or current the Class A amplifier becomes problematic. This amplifier is designed in such a way that it operates over the most linear

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region of its operational range. The main reason for the inefficiency of the Class A amplifier is due to de fact that the amplifying device is conducting all the time, even if there is no input signal.
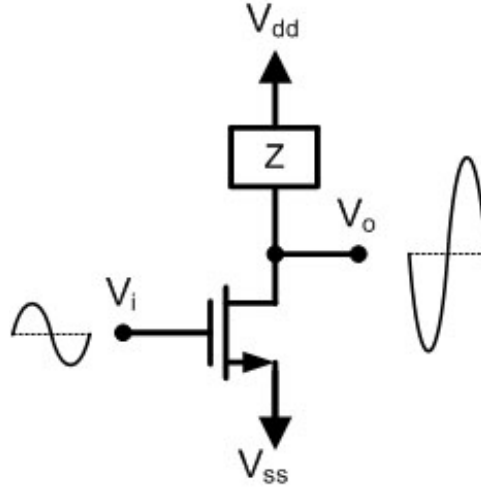
Figure 2.1: Basic configuration of a Class A amplifier.

For this reason, if a Class A amplifier is required to deliver a high current or voltage, the power consumption becomes significant. In the best case it consumes at least the same power that is being delivered to the output. This represents a drawback as the minimum power supply requirements might increase and even a large amount of heat might be generated. Class A amplifiers were common in audio applications as they offer high linearity over the operational range. Currently, they being replaced due to their large power consumption.

Fig. 2.2 shows a practical implementation of a Class A amplifier and Fig. 2.3 shows the transfer characteristic of the Class A amplifier. Observe that the positive value of the output voltage saturates at $I_{MP}R_L$, as the maximum

current delivered by Mp is I_{Bias} and is constant. Here we are assuming that $R_L \cdot I_{Bias} < V_{dd} - V_{DSMp}^{sat}$. This represents an important limitation for some applications, as it introduces distortion in the upper half of an input signal. The graphic of the output current is a replica of the transfer characteristic in Fig. 2.3 scaled by a factor R_L. Fig. 2.4 shows its operation when a sinusoid signal is applied at the input.
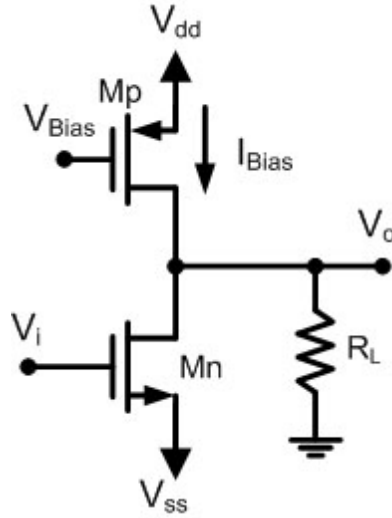
Figure 2.2: Implementation of a Class A amplifier.

An optimal amplifier design can avoid the presence of harmonic frequencies. The use of valves, of vacuum tubes, offer a higher fidelity and are still used these days, even if the cost of implementation is high. However, the use of transistors has become very popular due to cost reduction. MOSFET's have similar characteristics to valves. For this reason, they are often used in high quality amplifiers, rather than bipolar transistors.
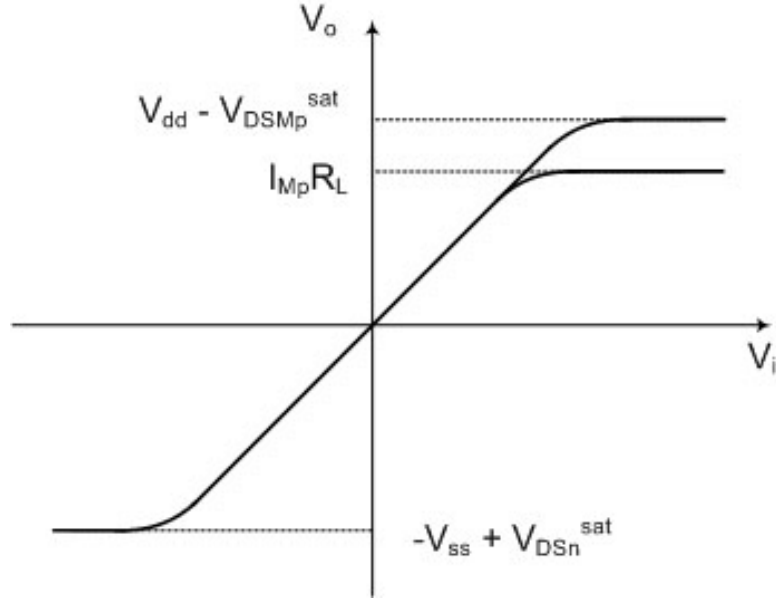
Figure 2.3: DC transfer characteristic of the Class A amplifier.

As transistors become cheaper, the complexity of the design of the amplifiers increases, so as to offer greater efficiency. A very common application for the Class A amplifier is the differential pair [1], which is exceptionally linear. It has another very attractive characteristic, which is its common mode rejection ratio [1]. The differential pair is the core of many more complex circuits, including Operational Amplifiers (opamps), and Operational Transconductance Amplifiers (OTA).

2.2   CLASS B

Fig. 2.5 shows the basic configuration of a Class B amplifier [1,8]. These amplifiers only amplify during half of the cycle of the input signal. Therefore, it has a conduction angle that is less than or equal to 180°. This leads to consid-
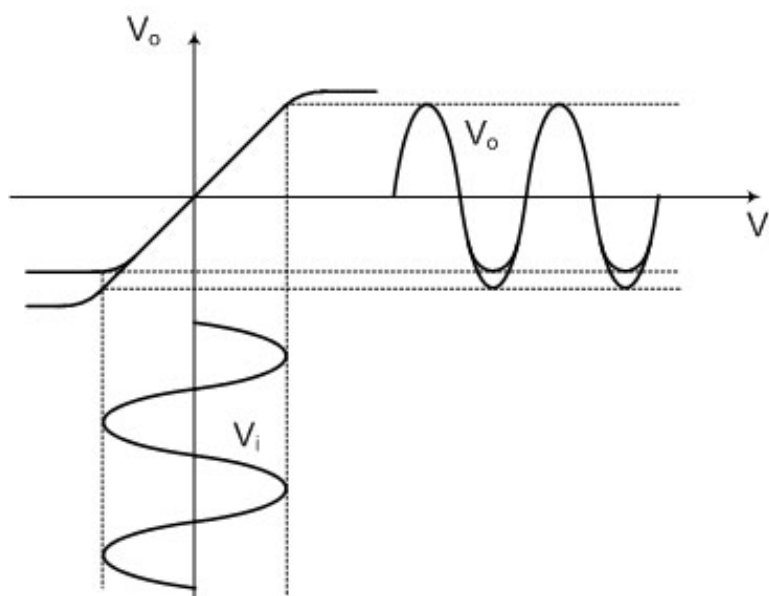
Figure 2.4: Operation of the Class A amplifier when a sinusoidal signal is applied at the input.

erable distortion, but their efficiency is greatly improved compared to the Class A amplifier. This is due to the fact that the amplifying device does not conduct half of one cycle of the input signal. Therefore, it does not consume power during that time. This amplifier has a theoretical efficiency of 78.5% [4, 7, 8].

A single Class B device is not very common, although it is useful for some applications where the distortion is not important, such as RF power amplifiers. A practical design using Class B amplifiers is the complementary pair, also known as a "push-pull" amplifier as shown in Fig. 2.6(a). In this design, each one of the devices is used to amplify one half of the input signal.

Fig. 2.6(b) shows a practical implementation of a Class B amplifier driving a load. Fig. 2.7(a) shows the transfer characteristic of the Class B amplifier and
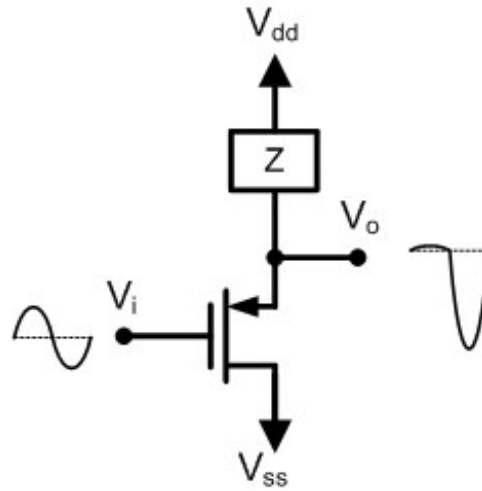
Figure 2.5: Basic configuration of a Class B amplifier buffer.

Fig. 2.7(b) the current through transistors Mp and Mn. This structure enhances the efficiency substantially, although it presents a drawback. Observe from Fig. 2.5(b) there is a small region where both devices do not conduct, centered around the midpoint of the operational range. This results in a null output voltage in Fig. 2.5(a). This dead band is known as crossover distortion.

Fig. 2.8 shows its operation when a sinusoid signal is applied at the input. A versatile solution to this constrain is to bias both devices to conduct all the time, even when an input signal is not present, rather than let the device turn off when they are not in use. This operation is called Class AB, and is discussed in the next section.
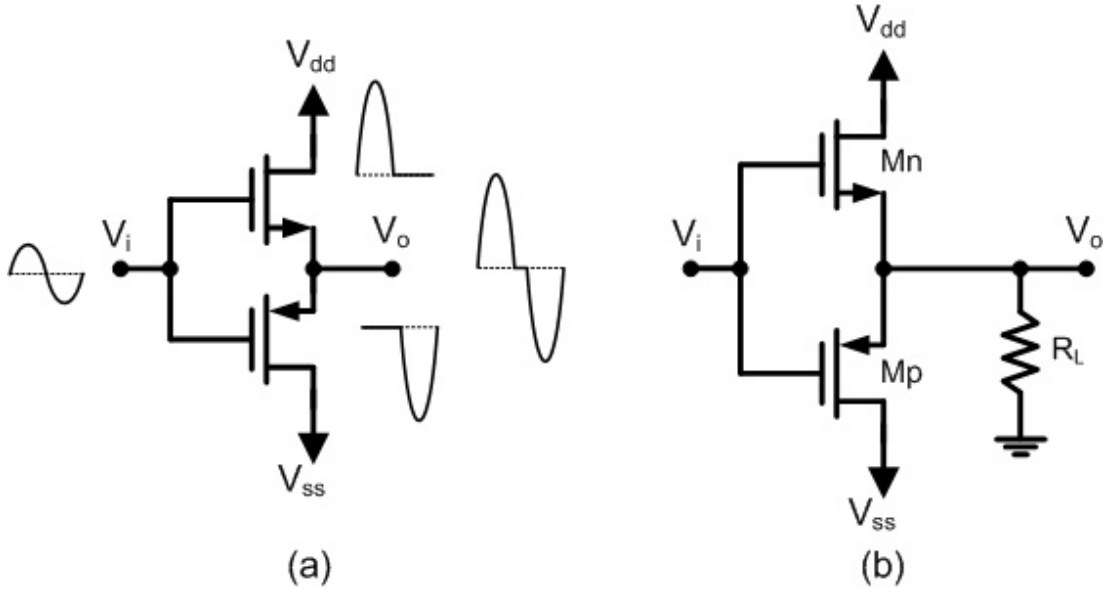
Figure 2.6: a) Basic configuration of a push-pull Class B amplifier and b) practical implementation driving a load.

2.3 CLASS AB

As mentioned in the previous section, the Class AB amplifier is designed to bias two Class-B amplifying devices on all the time, rather than off when they are not in use. Fig. 2.9 shows the basic configuration of a Class AB amplifier [1,2,4,9]. Each of the transistors has a conducting cycle between 180 and 360°. We should mention that the efficiency of a Class AB is greater than a Class A, but it is less than a Class B.

Fig. 2.10 shows a practical implementation of a Class AB amplifier. Fig. 2.11(a) shows the transfer characteristic of the Class B amplifier and Fig. 2.11(b) shows the currents through transistors Mp and Mn. Note that the voltages V_{bat} are included in the design, so as to overlap the conduction region of operation of

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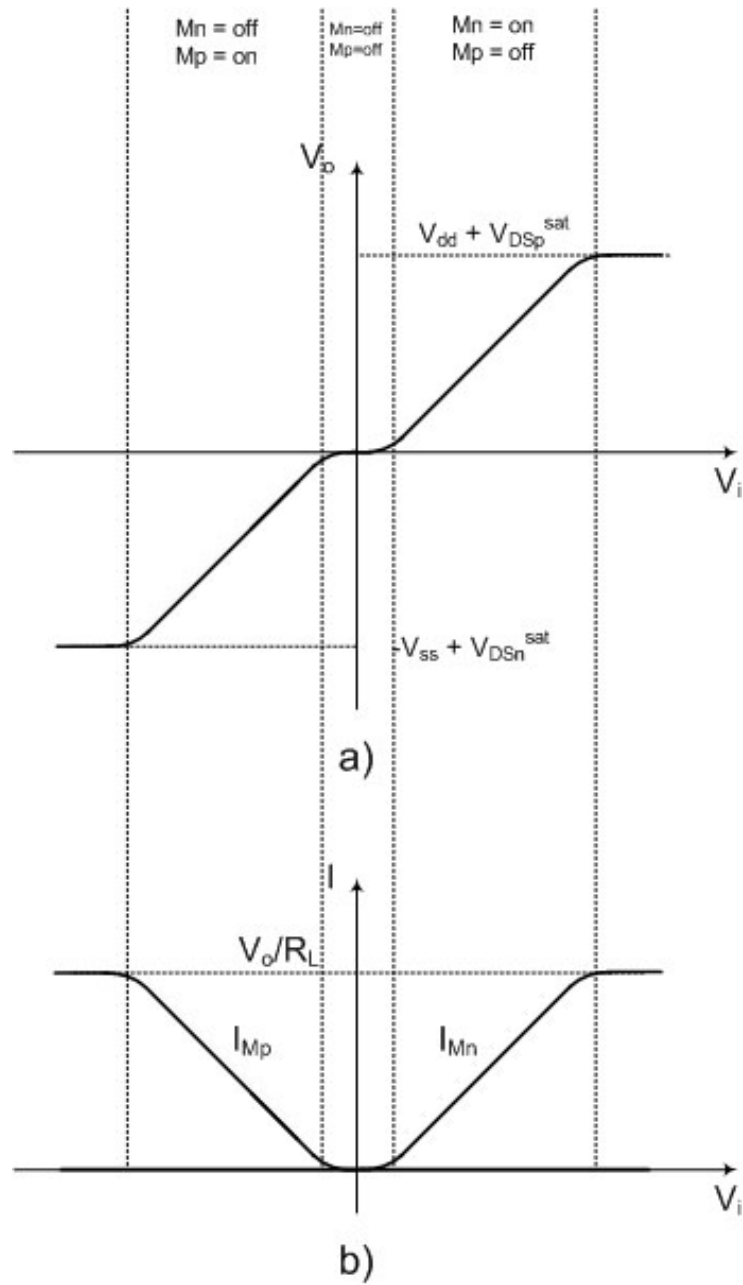
Figure 2.7: DC transfer characteristic of the Class B amplifier. a) Output Voltage and b) currents through the amplifying devices.
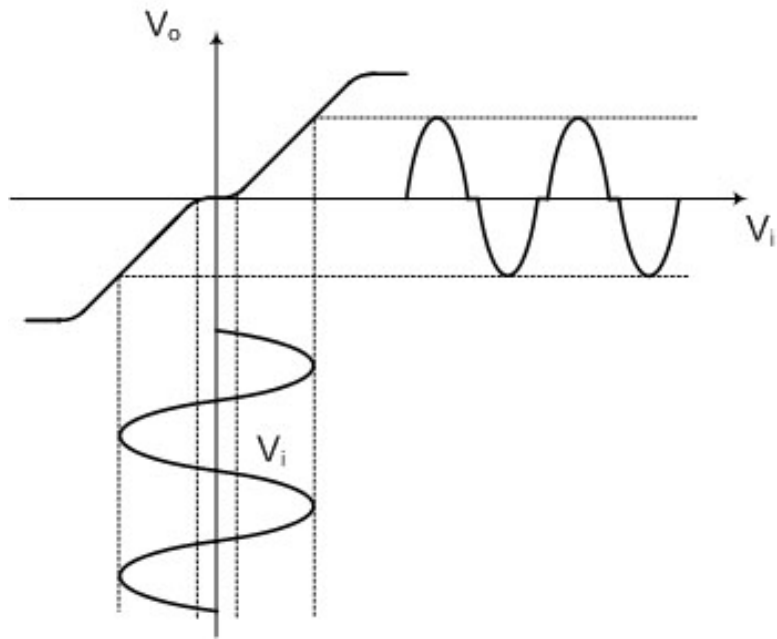
Figure 2.8: Operation of the Class B amplifier when a sinusoid signal is applied at the input.
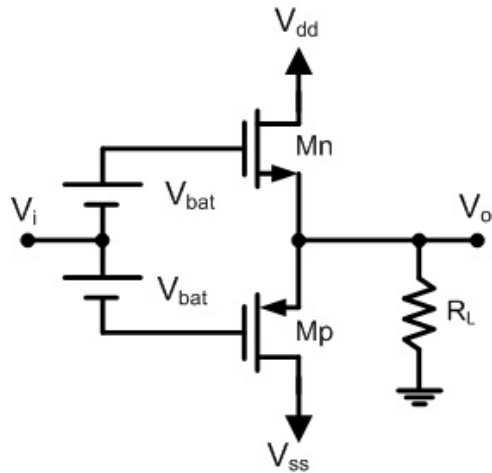
Figure 2.9: Basic configuration of a Class AB amplifier buffer.

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both transistors and eliminate the dead band region. Here, each device operates in a non-linear region; it is only linear over one half of the waveform, but still conducts a small amount in the other half. This amplifier behaves as a Class A amplifier in the region where both transistors are on, but beyond that point only one device remains in its linear region and the device turns off. The result is that when the transfer characteristic of the two transistors is combined, the crossover is greatly minimized. Fig. 2.12 shows its operation when a sinusoidal signal is applied at the input.
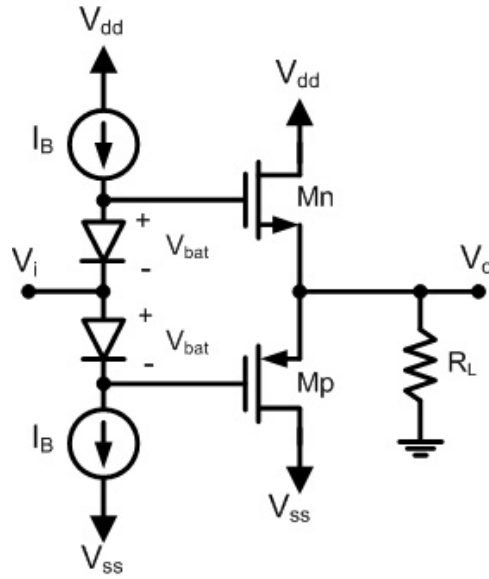
Figure 2.10: Implementation of a Class AB amplifier.

Class AB push-pull circuits are the most common type of amplifiers used in audio power amplifiers. This type of amplifier is preferred for audio amplifiers, since often the music is quiet enough that the signal stays in the Class A region, where it is reproduced with good fidelity. If it goes beyond this region, the dis-

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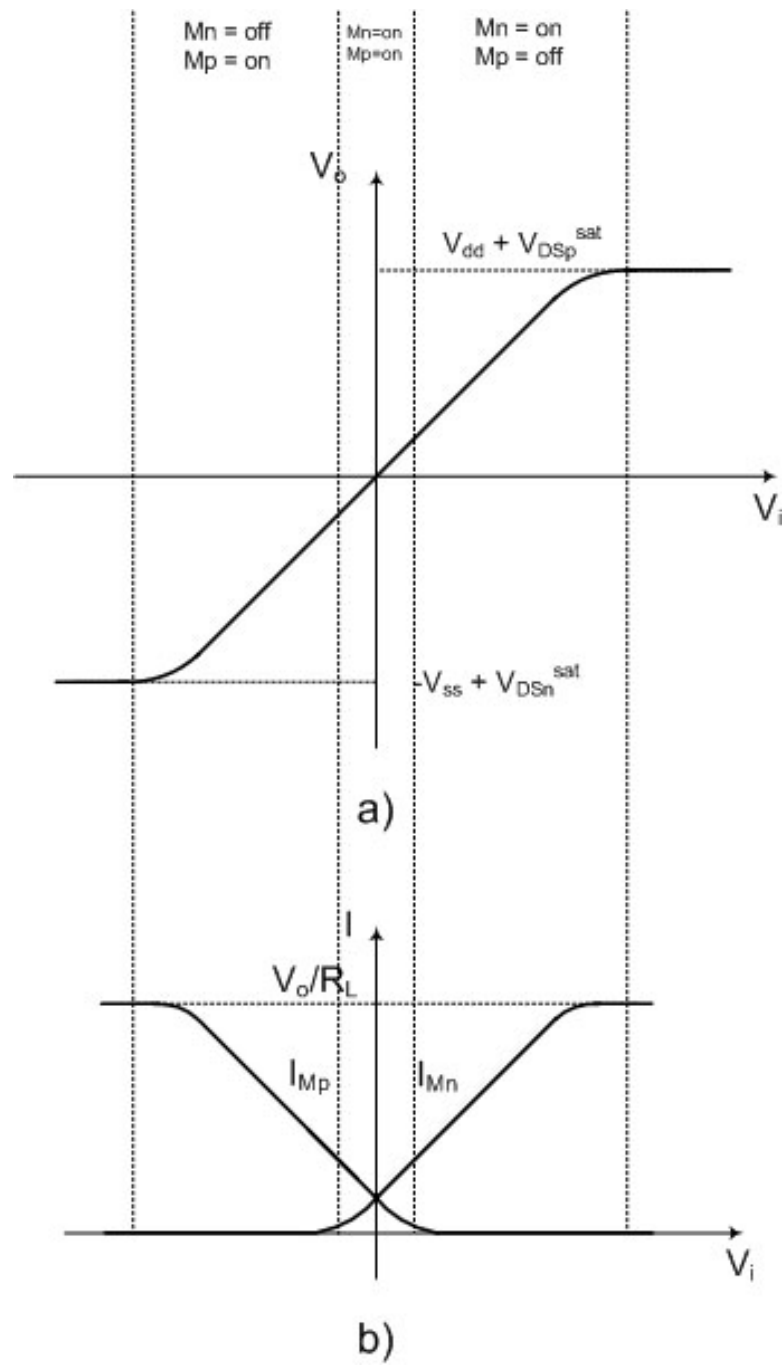
Figure 2.11: DC transfer characteristic of the Class AB amplifier. a) Output Voltage and b) currents through the amplifying devices.

tortion when operated in Class B operation is relatively small. These amplifiers are also used for RF linear amplifiers.
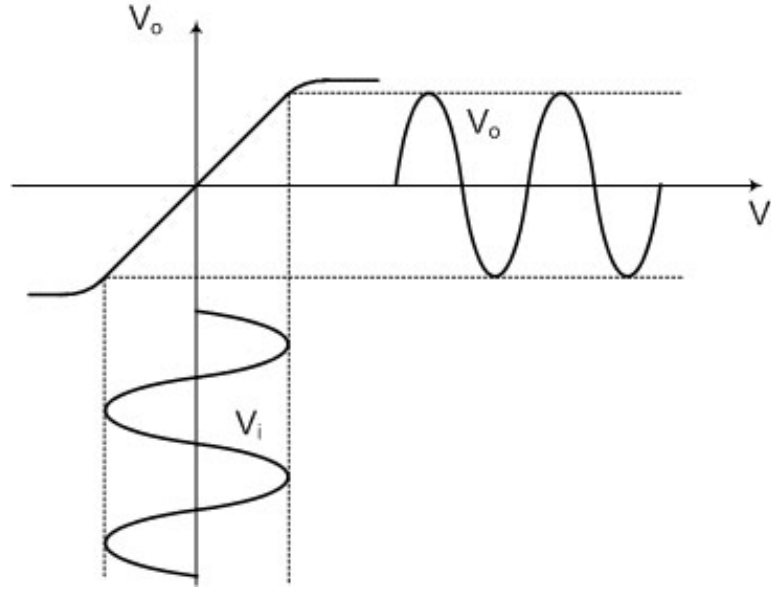
Figure 2.12: Operation of the Class AB amplifier when a sinusoid signal is applied at the input.

2.4 CLASS C

In Class C amplifiers, the amplifying device is deliberately not operated linearly. Instead, it is operated as a switch in order to reduce resistance loss. The conduction angle of this amplifier is usually made as short as possible, generally less than 180°. A typical Class C amplifier and operation is illustrated in Fig. 2.13 [4, 10].

Fig. 2.14 shows the implementation of the basic Class C amplifier and Fig. 2.15 shows the input and output voltage waveforms. From the schematic
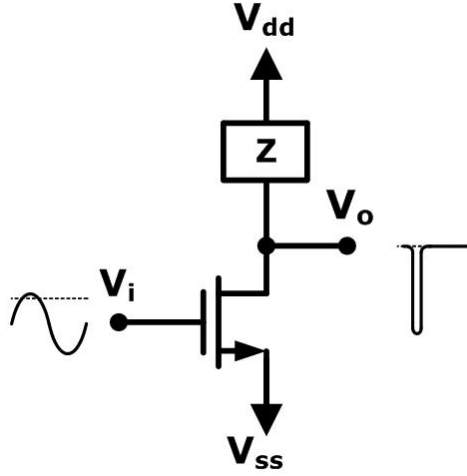
Figure 2.13: Basic configuration of a Class C amplifier.

one can see that the drain terminal of the transistor is connected to the positive power supply through an inductor L, and it is also connected to the load R_L through a capacitor C. This capacitor is used to remove the DC voltage. When the transistor is conducting, behaving as a closed switch, current starts flowing through the inductor L into the transistor. A magnetic field builds up in the inductor L depending on the magnitude of the current. At the same time the capacitor C delivers charge to the load R_L, generating a current also through the transistor. When the transistor is off, behaving as an open switch, the magnetic field in the inductor, which was built up during the previous state, generates a current that flows through the capacitor into the load.

Class C amplifiers amplify less than half of a cycle of the input signal and the distortion they present is high, although they can achieve a theoretical efficiency of 90% [10]. Some applications tolerate such high distortion, such as power
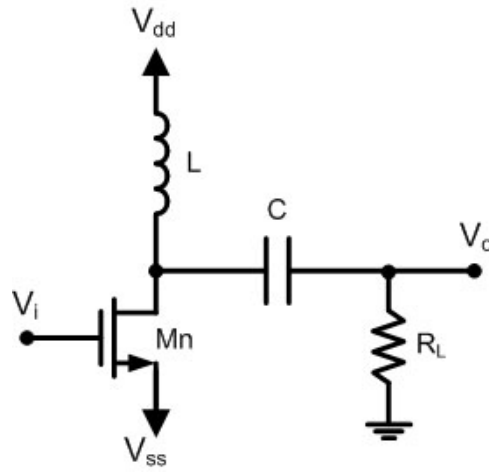
Figure 2.14: Implementation of a Class C amplifier.

megaphones and RF transmitters, where other methods are applied afterwards to decrease the distortion. Such is the case when using tuned loads instead of the capacitor C in Fig. 2.14. The input signal is used to switch the amplifier on and off and generate pulses of current in the tuned load. Thus, it will resonate only at particular frequencies, eliminating undesired signals. Therefore, the desired frequency can be generated by the tuned load.
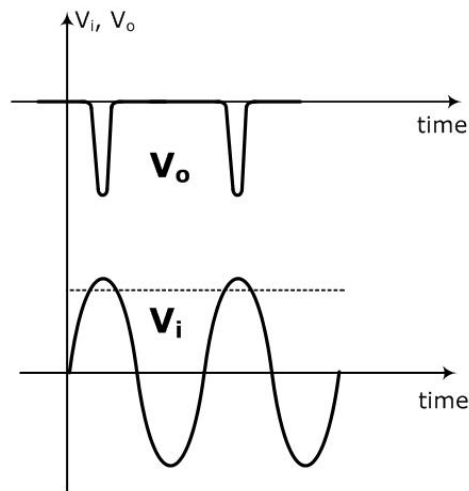
Figure 2.15: Operation of a Class B amplifier.

2.5 CLASS D

Class D amplifiers are power amplifiers where all the power devices are either on or off [4,11]. Applications of Class D amplifiers are pulse generators and low-power audio amplifiers. The purpose of this type of amplifier is to reproduce signals with a bandwidth much lower than the switching frequency. They use Pulse Width Modulation (PWM), Pulse Density Modulation (PDM) (also known as Pulse Frequency Modulation), or a more advanced form of modulation, such as Sigma Delta modulation.

Fig. 2.16 shows the basic configuration of a Class D amplifier [11]. The operation of these amplifiers is as follows. The input signal is converted into a sequence of pulses, where the averaged value of the pulses is directly proportional to the amplitude of the input signal at that time, as illustrated in Fig. 2.17. The frequency of the pulses is typically ten or more times the highest frequency of the input signal. Usually the output includes undesired harmonics, which can be removed with a passive filter.

The main advantage of Class D amplifiers is their power efficiency. The output pulses have a fixed amplitude, and the switching devices are either on or off most of the time. The only time they are conducting is when they transition between one state and another. In this case the power dissipation is the product of the voltage and current being delivered to the output, which depends on the capacitive or resistive load. But the transition usually occurs in a very short inter-
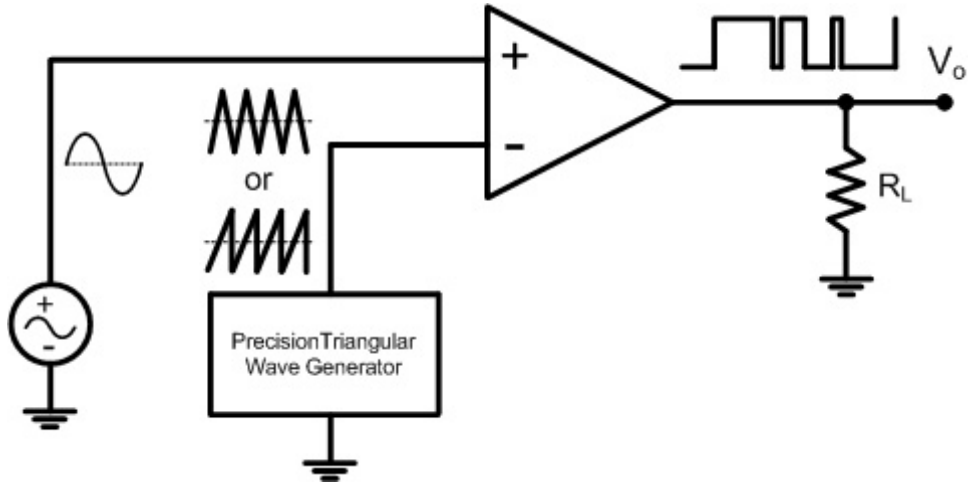
Figure 2.16: Basic configuration of a Class D amplifier.

val; therefore the power dissipation is reduced dramatically. Other characteristics of the Class D amplifier is its capacity to drive a large capacitive or low resistive load. In this case, slew rate plays an important role in the speed and efficiency.
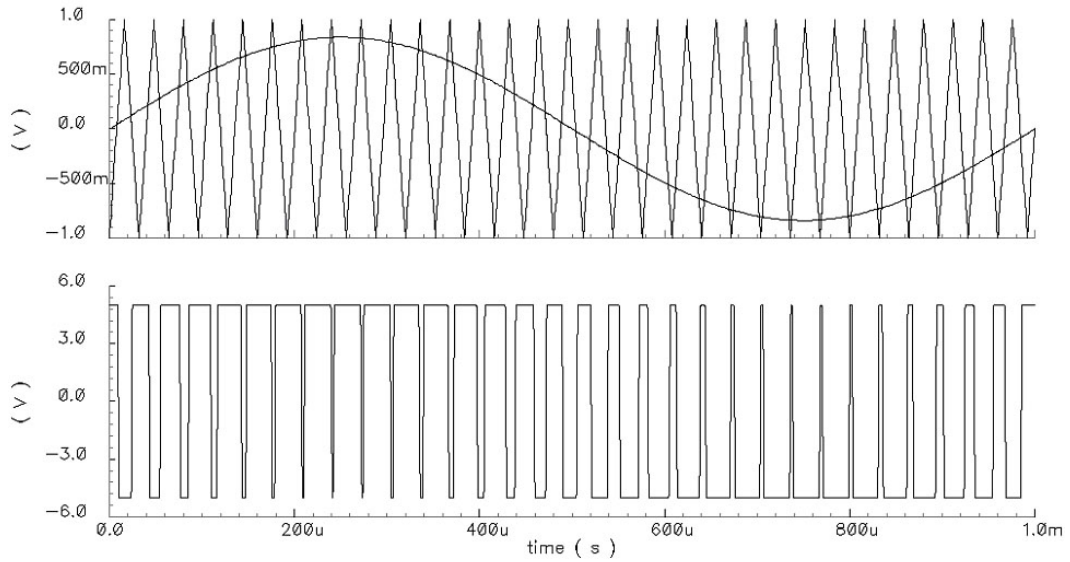
Figure 2.17: Voltage waveforms of a Class D amplifier.

Class D amplifiers can be controlled by either analog or digital circuits. A drawback of a digital controller is that it presents additional distortion called

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"quantization error" caused by the conversion of the input signal to a digital value. These amplifiers were very common to control small DC motors, such as the popular "stepper motors." They are now also used in low-power audio amplifiers, where additional circuitry is needed to convert the analog signal into a much higher frequency pulse width modulated signal. These amplifiers obtain efficiencies between 80 and 95%. Although Class D amplifiers offer a very high efficiency, an important limitation is the Power Supply Rejection Ratio. As the output devices are either on or off, and the voltage delivered to the output is one of the supply voltages, noise in the power supply is reflected at the output.

As a note, sometimes the letter D used to designate this type of amplifier is misinterpreted. It is just the next letter after C; it does not stand for digital.

2.6   OTHER CLASSES

The Class E amplifier is a switching power amplifier with very high efficiency. These amplifiers have gained acceptance since their introduction, due to their simplicity, high efficiency, easy design and tolerance to circuit variations. Typically it is used at such high frequencies that the switching time becomes comparable to duty cycle time . Fig. 2.18 illustrates the most common Class E configuration [12, 13]. Observe that the drain terminal of the transistor is connected to the load R_L through an LC circuit composed by the capacitor C_1 and

the inductor L_1 in series. It is also connected to the power supply V_{dd} through the inductor L_2 and to ground through the capacitor C_2.
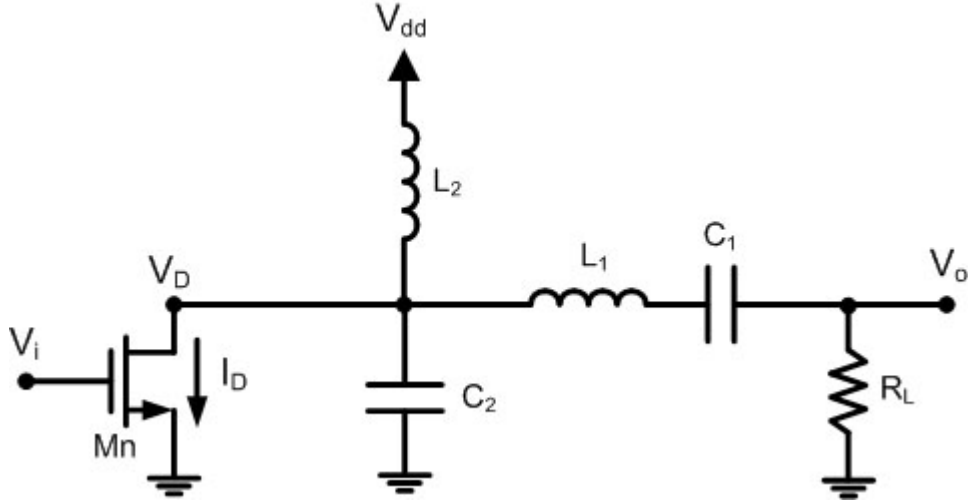
Figure 2.18: Basic configuration of a Class E amplifier.

In this design the transistor acts as a switch, rather than as an amplifier. When the transistor is on (switch is closed), the voltage of the drain terminal is close to zero, and current flows through the series L_1C_1-circuit into the transistor; also, some current begins to flow to the parallel L_2C_2-circuit to ground. When the transistor is off (switch is open), the current through the transistor is zero, but a voltage in the drain can exist. In this situation the series L_1C_1-circuit swings back and compensates for the current in the parallel L_2C_2-circuit. The entire circuit performs a damped oscillation. Note that the damping by the load is adjusted so that some time later the energy from the inductors goes into the load. But the energy in both capacitors peaks at the original value to restore the original voltage, so that the voltage across the transistor is zero and it can be switched on again.

Typical drain voltage and current waveforms are shown in Fig. 2.19. Observe that simultaneous nonzero voltage and current is avoided, eliminating transistor power losses when the transistor is either completely open or close. Capacitor C_2 acts to hold the drain voltage V_D at 0V during the on-to-off transition, to avoid power losses during the switching period.
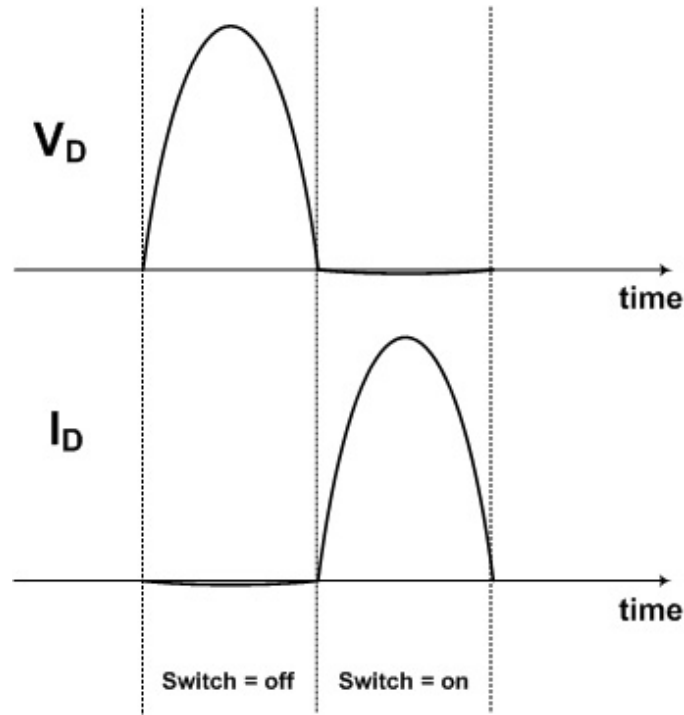
Figure 2.19: Basic configuration of a Class D amplifier.

The Class F amplifier is also a switching power amplifier, similar to the Class E amplifier. The Class F amplifiers uses an output filter to control the harmonic content of the drain voltage and the drain current waveforms of the transistor, thereby shaping them to reduce power dissipation in the transistor and, thus, to increase efficiency. Fig. 2.20 illustrates the most common Class F

configuration [4]. From the schematic, it is noticed that the output voltage V_o is a square waveform, while the drain current I_D is a half-rectified sinusoid. There is no overlapping between the output voltage and the current waveform, which leads to a maximum achievable power efficiency of 100% under ideal conditions. To accomplish this, the transistor has a bias point at the cutoff region of the switching operation. Also, from Fourier analysis, the voltage square waveform only has the fundamental and odd harmonics [13]. Therefore, the transistor behaves as an open switch at even harmonics and as a closed switch at odd harmonics.
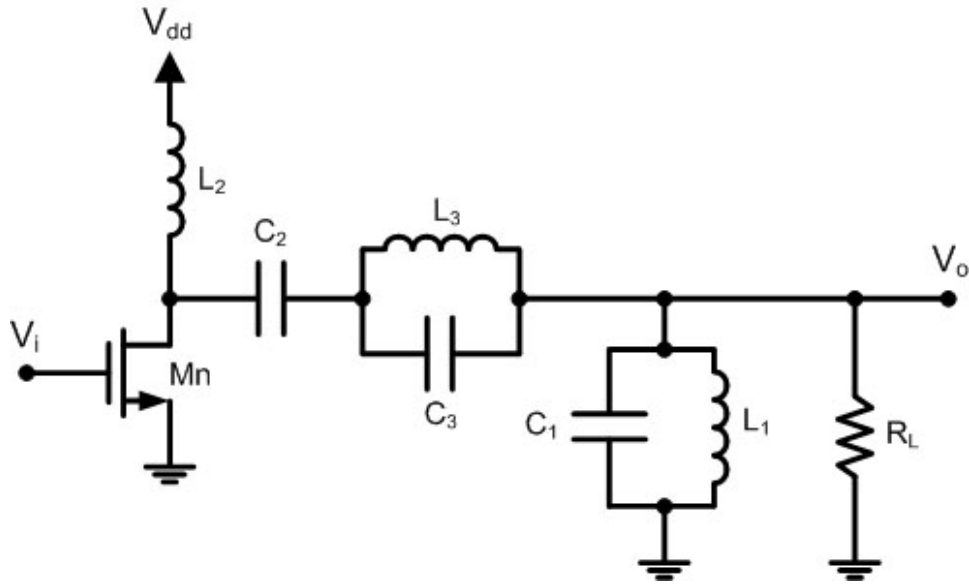
Figure 2.20: Basic configuration of a Class E amplifier.

Class G amplifiers are a more efficient version of class AB amplifiers, which are driven by a multi-rail power supplies to decrease power consumption and increase efficiency. This amplifier has several power rails at different voltages. The operation of a Class G amplifier is illustrated in Fig. 2.21 [6]. Observe that the

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amplifier switches between rails as the output signal approaches the corresponding rail. Thus the amplifier increases the efficiency by reducing the "wasted" power at the output transistors. Note that this case has two values for each power supply, although in some designs the amplifier includes more than two values.
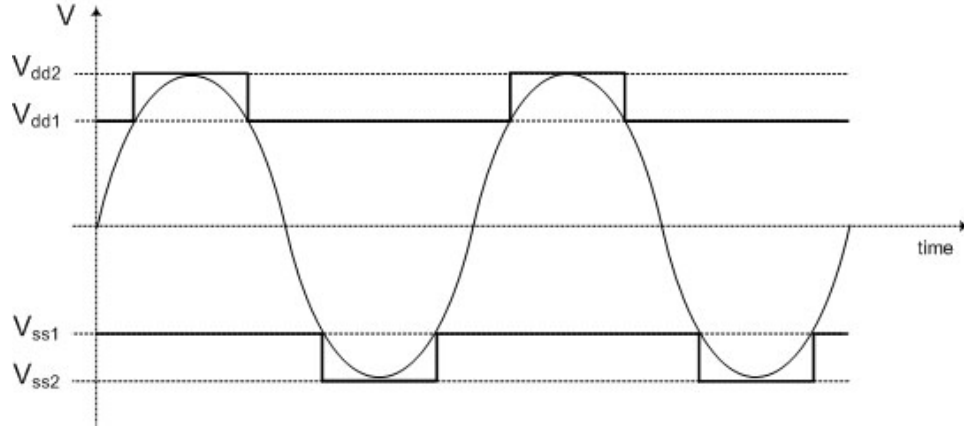
Figure 2.21: Basic configuration of a Class G amplifier.

A Class H amplifier is a more complex version of the Class G amplifier, in which the rail voltage is modulated by the input signal. The operation is illustrated in Fig 2.22 [13]. This is done by modulating the supply rails so that the rails are only a few volts larger than the output signal at any given time, keeping the voltage across the transistors small and the output transistors cool. The output stage operates at its maximum efficiency all the time. Switched mode power supplies can be used to create the tracking rails. The efficiency is considerably increased and it reduces THD performance, but it has the limitation that a complicated power supply design is required.
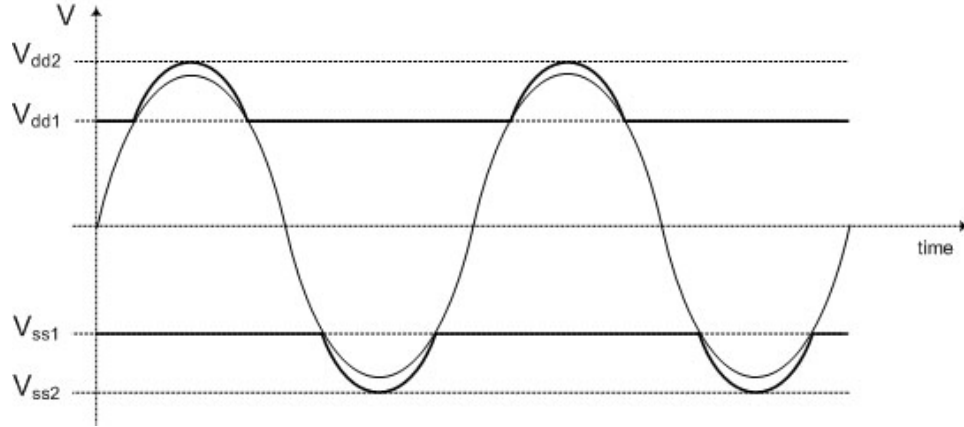
Figure 2.22: Basic configuration of a Class H amplifier.

2.7 EFFICIENCY

An amplifier's efficiency is a measure of its ability to convert the dc power of the supply into signal power delivered to the load. The definition of efficiency can be represented in an equation form as

$$\eta = \frac{Signal\ power\ delivered\ to\ load}{DC\ power\ supplied\ to\ output\ stage} \qquad (2.1)$$

For an ideal amplifier, the efficiency is one. Thus, the power delivered to the load is equal to the power taken from the DC supply. In this case, no power would be consumed by the amplifier. In reality, this is not possible, especially in high frequency RF circuits. In many high frequency systems, the output stage and driver stage of an amplifier consume power in the amplification process.

The output power level is an important aspect in evaluating the power amplifier. The output power capability factor, P_{max}, is the output power that would be produced with stresses of 1 Volt and 1 Amp on the drain of the amplifying

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transistor. Multiplication of P_{max} by the drain voltage and current ratings of a real device produces the maximum output power available from that device, given by the expression

$$P_{max} = \frac{Maximum\ output\ power}{Peak\ drain\ voltage\ \cdot\ Peak\ drain\ current} \tag{2.2}$$

The amplifiers previously described have been classified according to their circuit configuration and methods of operation. These classes range from entirely linear with low efficiency to entirely non-linear with high efficiency. Amplifiers Classes A, AB, B, and C can be defined in terms of the conduction angle Y as follows:

$$Class\ A \quad \Rightarrow \quad y\ =\ \pi \tag{2.3}$$

$$Class\ B \quad \Rightarrow \quad y\ =\ \frac{\pi}{2} \tag{2.4}$$

$$Class\ AB \quad \Rightarrow \quad \frac{\pi}{2} < y < \pi \tag{2.5}$$

$$Class\ C \quad \Rightarrow \quad y < \frac{\pi}{2} \tag{2.6}$$

The conduction angle is defined as

$$Y = arccos\left(-\frac{I_D^Q}{I_{V_{dd}}}\right) \tag{2.7}$$

The current through the load is

$$\begin{aligned}
I_{R_L} &= \frac{1}{2\pi}\int_0^{2\pi} i_D\left(\Theta\right)\cdot d\Theta = \frac{1}{\pi}\left(y \cdot I_D^Q - I_{V_{dd}} \cdot sin(y)\right) \\
&= \frac{I_{V_{dd}}}{\pi}\left(sin(y) - y \cdot cos(y)\right)
\end{aligned} \tag{2.8}$$

Also, the output voltage, V_o, can be obtained in terms of Y as

$$
\begin{aligned}
V_o &= \frac{1}{2\pi} \int_0^{2\pi} i_D(\Theta) \cdot R \cdot d\Theta \\
&= \frac{R}{2\pi} \left(4I_D^Q \cdot sin(y) + 2I_{V_{dd}} \cdot y + I_{V_{dd}} \cdot sin(2y) \right) \\
&= \frac{I_{V_{dd}} \cdot R}{2\pi} (2y - sin(2y))
\end{aligned}
\tag{2.9}
$$

The output power delivered to the load is

$$
P_o = \frac{V_o^2}{R}
\tag{2.10}
$$

The power delivered by the supply is

$$
P_{dc} = (V_{dd} - V_{ss}) \cdot I_{V_{dd}}
\tag{2.11}
$$

The maximum output voltage V_o is

$$
V_o^{max} = V_{dd}
\tag{2.12}
$$

From the above equations, the maximum efficiency is

$$
\eta_{max} = \frac{P_o^{max}}{P_i} = \frac{2y - sin(2y)}{4 \left(sin(y) - y \cdot cos(y) \right)}
\tag{2.13}
$$

Since the peak drain current I_D is

$$
I_D^{max} = I_D^Q + I_{V_{dd}}
\tag{2.14}
$$

The output power capability factor is

$$
P_{max} = \frac{P_o^{max}}{V_D^{max} \cdot I_D^{max}} = \frac{2y - sin(2y)}{8\pi \cdot [1 - cos(y)]}
\tag{2.15}
$$

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For example, the output power of the Class B shown in Fig. 2.5 when using a resistive load R_L is

$$P_o = \frac{1}{2} I_{R_L} \cdot V_o \tag{2.16}$$

Therefore, the drain current I_D of the transistor is

$$I_D^Q = 2 \frac{I_{R_L}}{\pi} \tag{2.17}$$

The power it consumes is

$$P_{dc} = 2 \frac{I_{R_L} \cdot V_{dd}}{\pi} \tag{2.18}$$

Which gives a maximum efficiency when $V_o^{max} = V_{dd}$ of

$$\eta = \frac{P_o}{P_{dc}} \cdot 100 = \frac{\pi}{4} \cdot \frac{V_o^{max}}{V_{dd}} \cdot 100 \leq 78.53\% \tag{2.19}$$

2.8 COMPARISON

Table 2.1 shows a comparison of the amplifiers discussed in this chapter. The amplifier should be chosen according to the requirements of a given design. If efficiency is a critical aspect of a given design, and distortion can be traded for efficiency, therefore a Class D or a C should be chosen. On the other hand, if distortion is not allowed, even if the power consumption is increased, an amplifier such as a Class A or AB should be chosen. This is typical of power audio amplifiers.

2.9 LITERATURE SURVEY OF OUTPUT STAGES

The study of the output stages in amplifiers includes research done by some authors for applications in industry. During a recent literature survey in

Table 2.1: Comparison of the types of amplifiers.

Amplifier	Efficiency	Power	Conduction angle	distortion
Class A	50	high	$y = \pi$	very low
Class B	78.5	medium	$y = \frac{\pi}{2}$	high
Class AB	$50 < x < 78.5$	medium	$\frac{\pi}{2} < y < \pi$	low
Class C	90	low	$y < \frac{\pi}{2}$	very low
Class D	$95 < x$	very low	$y = 2\pi$	high
Class E	$95 < x$	low	$y < \frac{\pi}{2}$	low
Class F	$95 < x$	low	$y < \frac{\pi}{2}$	low
Class G	$95 < x$	high	$y = 2\pi$	high
Class H	$95 < x$	high	$y = 2\pi$	high

output stages we discover that there is considerable research in Classes AB and F amplifiers, but even more extensive research being done in Class E amplifiers. This chapter presents a brief description of where research is leading with the corresponding citations.

Class AB amplifiers are still an important part of research in the past few years, as they are utilized in audio power amplifiers. Some modifications to conventional Class AB amplifiers to increase the performance are presented next.

Fig. 2.23 shows a pseudo-differential-input differential-output amplifier operating in Class AB reported in [14] by Giustolisi, et. al. in 2007. This amplifier has a high-current drive capability. This circuit operates from a minimum supply of $V_T + 2V_{DS}^{sat}$, provides fast settling response, and is also characterized by a wide input differential range with high linearity that enables its use even as a transconductor for filtering applications. It includes two complementary versions of a conventional pseudo-differential pair working in class AB operation.
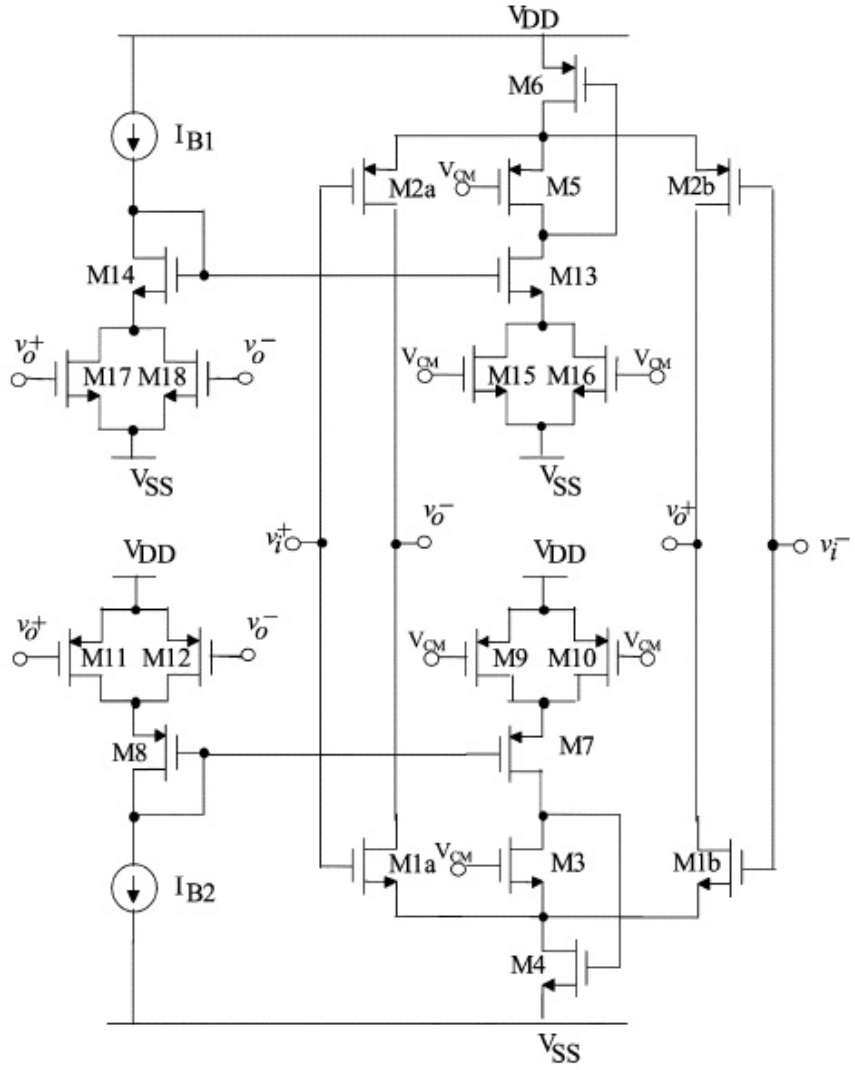
Figure 2.23: Class AB pseudo-differential-input differential-output amplifier [14].

Due to negative feedback in the current sources of both of the input differential pairs, transistors M4 and M6 form a Flipped Voltage Follower (FVF) [15]. This allows the source terminal of the transistors in the differential pairs to be at a constant voltage. Also, a large current can be achieved between both differential pairs when driving large capacitive or small resistive loads in the output. In addition, under large signal conditions, one transistor of the differential pair turns off when the other one still conducts.

Another recently reported Class AB two-stage opamp is shown in Fig. 2.24 [16], reported by Ramirez, et. al. in 2006. In this case an RC circuit is included between the gate terminal of the output transistor, to allow voltage swing in both of them. It is a very-low cost implementation, although it works for current peaks only when driving a square wave signal at the input. For constant demand of current, it does not behave as a Class AB amplifier. It is this suitable, for example, for audio amplifiers, where the lowest frequency of interest is 20Hz.

Class F amplifiers also play an important role in the research of the past few years. The circuit shown in Fig. 2.25 [17], reported by Jia-Liang Chen, et. al. in 2006, shows a SiGe BiCMOS Class F Power Amplifier for Bluetooth applications. The schematic shows that the circuit integrates both, the input matching network and the output fundamental and third harmonic loading networks. It improves the efficiency of the power amplifier by changing the load filter resonators in order to present a short circuit at even harmonics and an open circuit at odd harmonics.
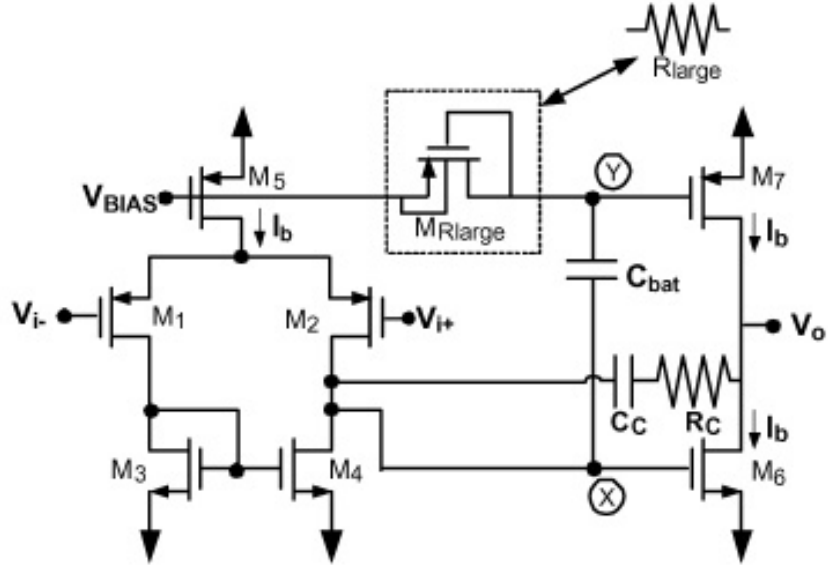
Figure 2.24: Class AB two-stage opamp [16].
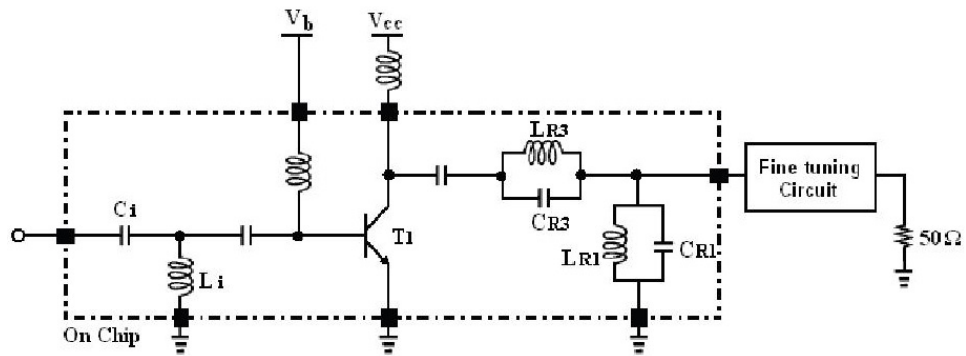
Figure 2.25: SiGe BiCMOS Class F Power Amplifier for Bluetooth applications [17].
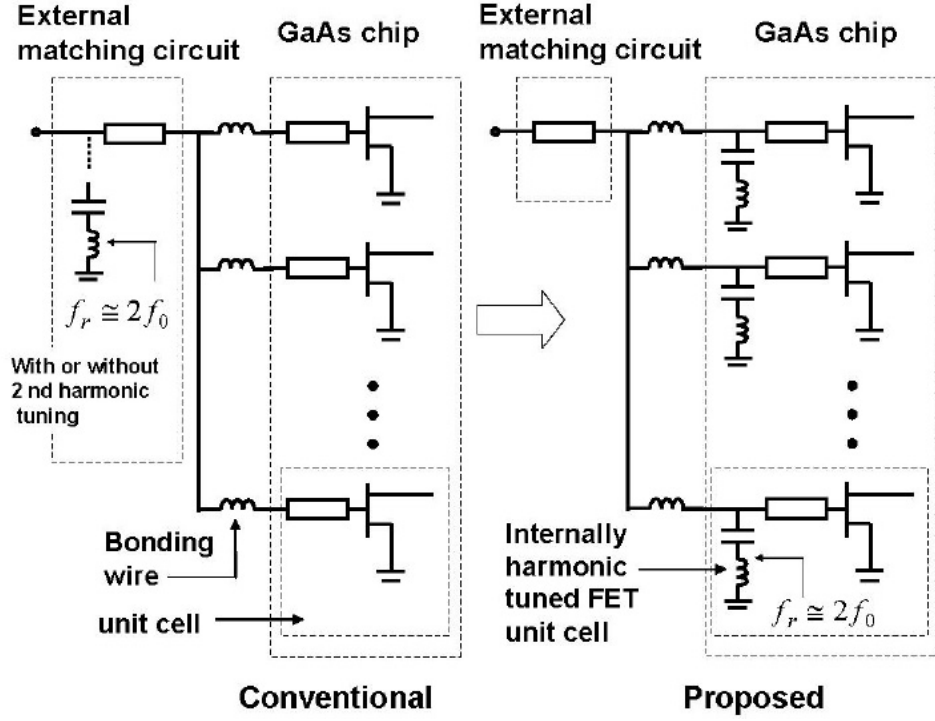
Figure 2.26: very low distortion class-F power amplifier for base stations of broadband access systems [18].

Another Class F architecture presented recently is shown in Fig. 2.26 [18] by Goto, et. al. in 2006. It is a very low distortion class-F power amplifier for base stations of broadband access systems. It uses an internally-tuned harmonic CMOS architecture (IHT-FET) to improve the linearity under class AB operating conditions. This feature is provided by the second-harmonic tuning circuit placed in front of each CMOS transistor as shown in the schematic. This allows accurate control of the input second-harmonic impedance.

Classes AB and F have been described so far. These types of amplifiers represent an important part of current research, although most research is cur-
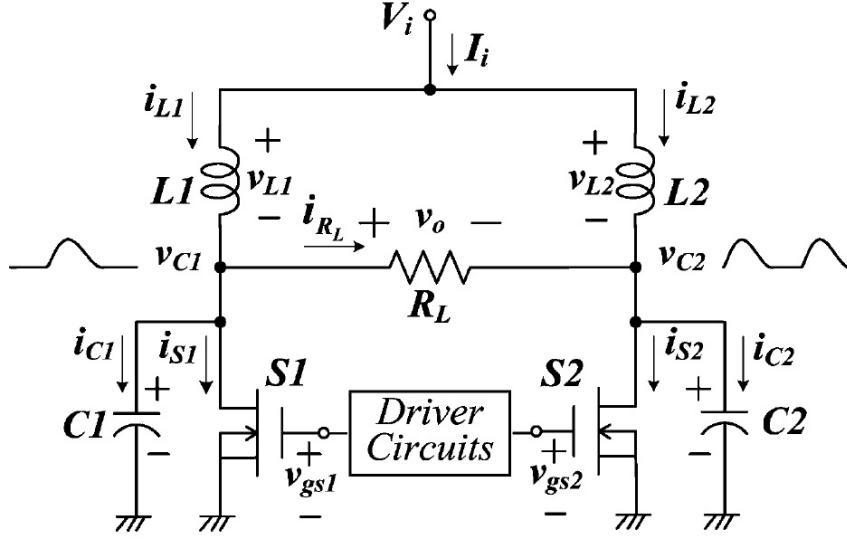
Figure 2.27: Pushpull Class-E series-parallel resonant power amplifier [19].

rently taking place with Class E amplifiers. Some recently reported architectures are discussed next.

Fig. 2.27 shows a pushpull Class-E series-parallel resonant power amplifier (PA) [19] reported by Feng-Yin Chen, et. al. in 2007. This topology parallels two basic one-inductor, one-capacitor Class-E high-efficiency switching-mode tuned PA circuits. This design realizes a faithful sinusoidal output voltage where the harmonic content in the output is an important criterion. The operation of this amplifier, including two series-parallel resonant load networks, allows sinusoidal output voltage to be achieved by associating with the positive and negative quasi-sinusoidal waveforms.

Fig. 2.28 shows the implementation of a new technique reported in [20], by Ortega-Gonzlez, et. al. in 2007, to design wide band Class E power amplifiers
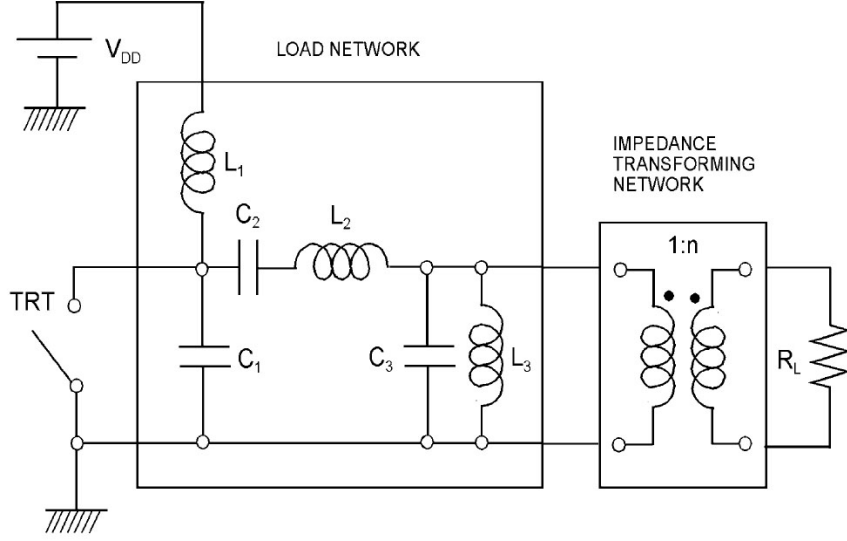
Figure 2.28: wide band Class E power amplifiers based on the synthesis of load admittances [20].

based on the synthesis of specific load admittances at fundamental and harmonic frequencies. This technique simplifies the design of wide band Class E amplifier by making it independent of any specific load, either capacitive or resistive. Results obtained in this reference show 35% fractional bandwidth and 80% efficiency.

Fig. 2.29 shows the implementation of a Class E amplifier reported in [21] by Saito, et. al. in 2006. The design utilizes a high-voltage Gallium Nitride (GaN) High Electron-Mobility Transistor (HEMT) transistor as the main switching device. Results show that this transistor can be operated in high-frequency switching power applications such as RF power-supply applications. Results also show an output power of 13.4 W and an efficiency of 91% under a drain-peak voltage as high as 330V.
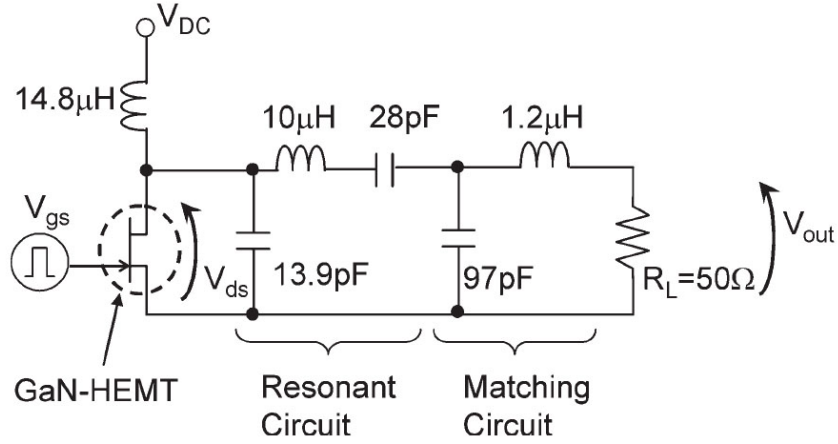
Figure 2.29: Class E amplifier using high-voltage GaN HEMT transistors [21].

Fig. 2.30 shows a Class E Injection-Locked Power Amplifier(Class-E ILPA) [22], reported by Hyoung-Seok Oh, et. al. in 2006, suitable for 2.4-GHz wireless sensor network applications where the maximum transmit-power is typically about 10dBm. In such a low transmit-power application, it is a great challenge to achieve a high transmit efficiency because the driving power and dc power consumption in the previous stage are no longer negligible compared with the transmitted signal power. Results in [22] show that this scheme has an efficiency of 44.5% with a drain efficiency of 49.3% when operating with a 1.2V supply voltage.

It was shown that many modifications and variations to the conventional types of amplifiers described in previous sections have been reported recently. Results show that these variations enhance the performance of the amplifiers, whether it is in reduced power consumption, increased efficiency, reduced power supply or increased operation at higher frequencies. Such is the result of using newer technologies, topologies or combinations of stages to achieve more desirable
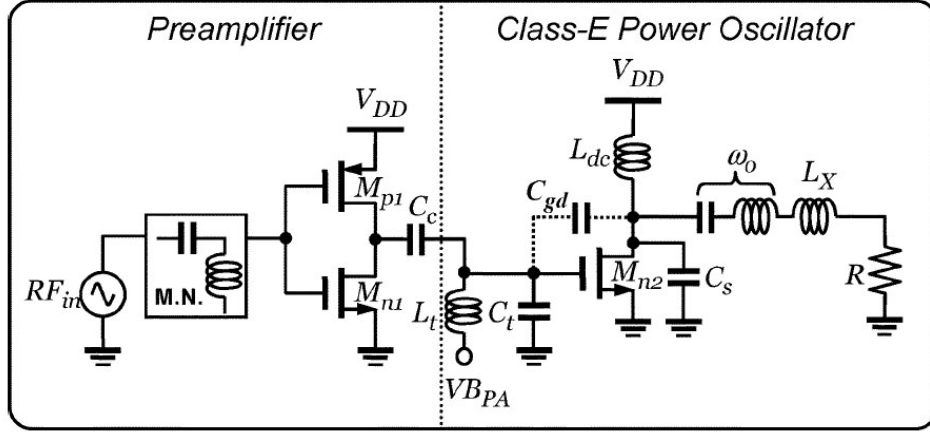
Figure 2.30: injection-locked Class-E power amplifier [22].

operation.

Class AB opamp using floating current sources

In this section we describe the Class AB opamp shown in Fig. 2.31 presented in [23]. We describe this amplifier in a more detailed manner as we will be using it in a comparison with others amplifiers described in this document. Observe from Fig. 2.31 that the input stage is composed by complementary differential pairs to provide rail-to-rail operation, formed by transistors Mn1-Mn3 and Mp1-Mp3. The output of this stage goes to the current mirrors formed by Mn4-Mn7 and Mp4-Mp7. These current mirrors are biased by the floating current sources composed by Mn8-Mn9 and Mp8-Mp9, which provides a constant current I_B. The biasing voltages of the floating current sources are determined by the biasing branches formed by Mn10-Mn13 and Mp10-Mp13, which set a voltage offset to have a static current I_B in the floating current sources. The output of

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the floating current sources bias the second stage formed by transistors Mn14 and
Mp14.
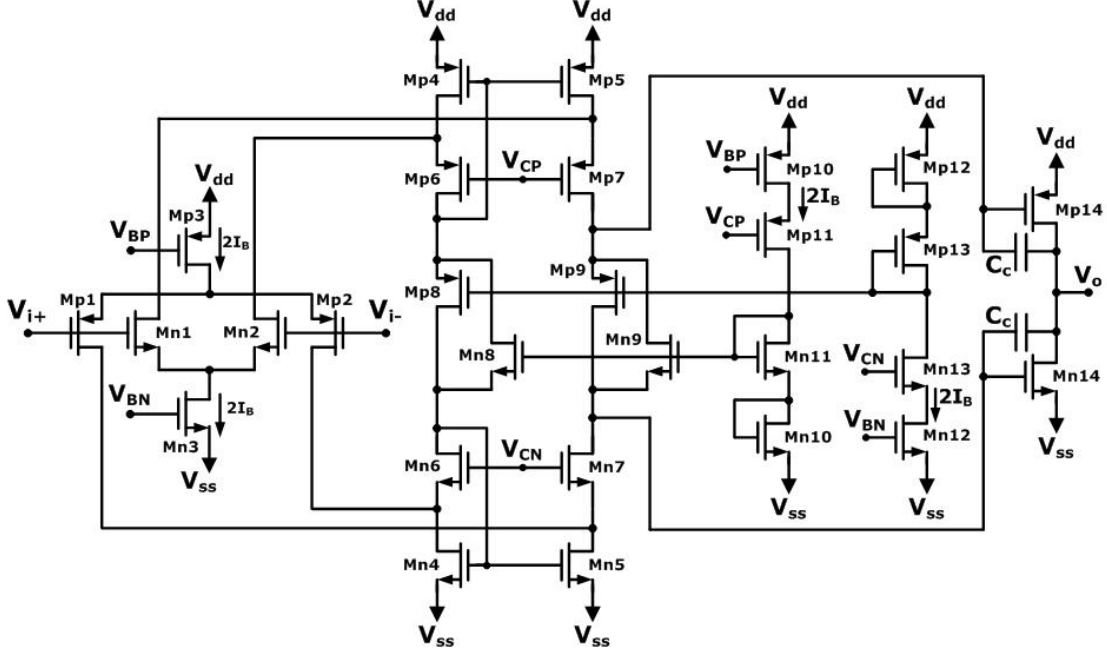
Figure 2.31: Class AB opamp using floating current sources.

Figs. 2.32(a) shows the DC transfer characteristic, (b) the Class AB opera-
tion of the output stage, (c) the frequency response and (d) the transient response
of the circuit in Fig. 2.31. The frequency response shows an open-loop gain A_v
= 104.3dB, a bandwidth of BW = 60Hz, a Gain-Bandwidth product of GBW =
10.47MHz and a phase margin of 45deg when driving a load of 15pF. The transient
analysis shows a measured slew rate SR+ = 10.65V/μsec and SR- = 8.1V/μsec.
The measured settling times are t_{s+} = 188.4nsec and t_{s-} = 193.8nsec. A square
signal of 1Vpp at 1MHz was applied at the input when driving a loading capacitor
of C_L = 15pF.
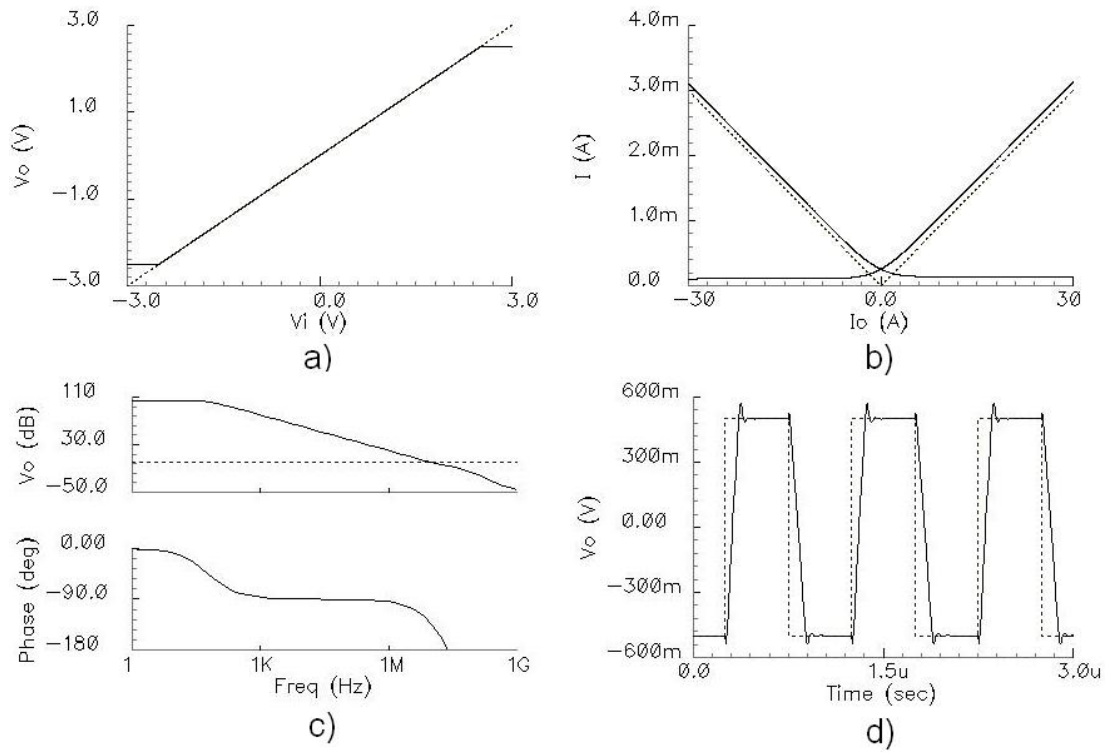
Figure 2.32: Operation of the circuit shown in Fig. 2.31 showing a) DC transfer characteristic, b) Class AB operation of the output stage, c) frequency response and d) transient analysis when using a square wave form of $1V_{pp}$ at 1MHz.

3 OBJECTIVE

The previous chapter presents a description of several types of output stages, including their advantages and limitations. For example, consider the case of amplifier Classes C, E and F, where the transistor is used as a switch rather than an amplifying device. As such, the power consumption is reduced dramatically, and the current across the transistor is set by other devices in the circuit. In the case of the Class D amplifier, the output stage saturates to either rail most of the time, dissipating power only during the transition where the slew rate plays a very important role. In the case of Classes A and B, the current is well defined by a current source, commonly implemented using another transistor. Let's now consider the case of the Class AB amplifier. A very important design criteria is setting the current in the output stage, which represents a considerable challenge for some implementations of this type of amplifier.

This challenge is due to the fact that both devices in the output stage have the capability to adjust their currents and in some designs it is not well controlled. Therefore the bias current can be dependent on various conditions in the circuit, such as the common-mode input voltage and the supply voltage. Moreover, the output devices tend to have very large sizes.

This document proposes a technique to control the quiescent bias current in the output stage of Class AB amplifiers. This technique consists in making a

Class AB Amplifier

V_{i+}

V_{i-}

+

-

V_o

Control signal

Control Circuit
operating under
static conditions
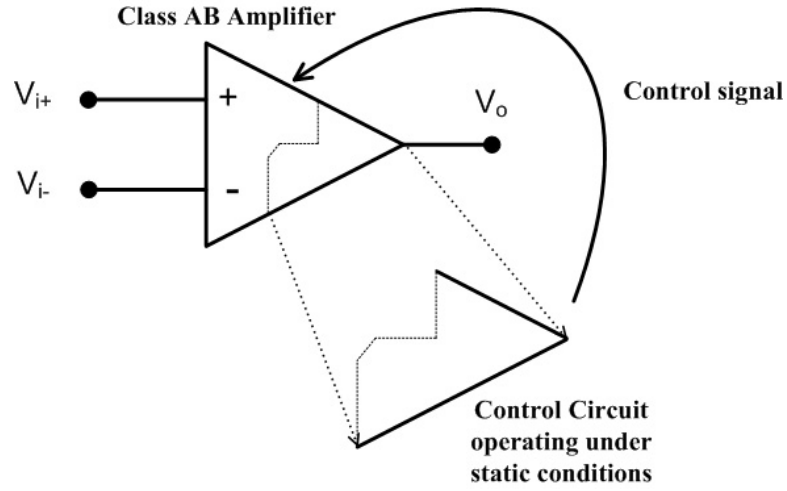
Figure 3.1: Block diagram of the technique to control the quiescent bias current in the amplifier.

replica of part of the circuit, as shown in Fig. 3.1, and having it operate under the desired bias conditions to obtain the proper state for the output devices in the operational part.

The following chapters present a more detailed description of the implementation of this technique, as well as how it achieves the desired quiescent bias current and how the performance of the amplifier is enhanced.

4 CONTROL CIRCUIT IMPLEMENTED IN CLASS-AB OPERATIONAL AMPLIFIERS WITH 2 AND 3 AMPLIFYING STAGES

This chapter presents the basic two-stage opamp composed of a differential pair as the first stage and a common-source configuration as the second stage. Then the biasing technique, described in Chapter 3 is implemented in a 2-stage amplifier as to provide Class-AB operation. Also, the same implementation is discussed for a 3-stage amplifier.

Opamps are one of the most popular basic cells used in many analog applications, such as Digital-to-Analog converters, RF receivers and transmitters. Yet there is another type of amplifier which is becoming more popular. Its name is based on the ratio of the output current to the input voltage, called the transconductance. Some authors refer to them as Operational Transconductance Amplifiers (OTAs) [3]. Several applications of transconductors have been reported in the past [24, 25].

There have been many variations of amplifiers reported in the past where the authors address different methods of enhancing their performance, such as increasing the number of amplifying stages, introducing Class-AB operation and/or rail-to-rail operation, and decreasing the supply requirements for low voltage applications.

Fig. 4.1 shows the schematic for a conventional two-stage opamp [2]. The first stage consists of a differential pair where the gain is determined by transistors M3 and M5. The gain provided by M2 is unity due to the diode connection of M4. These transistors operate in a common-source configuration; therefore, the gain provided by each one of them is given by their transconductance g_m multiplied by the impedance at the output node x. That impedance is the parallel combination of the impedance looking into the drain of each transistor $(r_{o3}||r_{o5})$. Thus, the overall gain of the first stage at node x is given by the expression:

$$A_{v1} = \frac{V_x}{V_{i+} - V_{i-}} = \frac{(g_{mM3} + g_{mM5})}{2} (r_{oM3}||r_{oM5}) \qquad (4.1)$$

Observe that node x is effected by both of the differential input signals; this node is referred to as a single-ended output. The gain of the second stage is given by transistor M6, which also operates in the common-source configuration. Thus, the overall gain of the amplifier is given by the expression:

$$\begin{aligned} A_v &= \frac{V_o}{V_{i+} - V_{i-}} = A_{v1}A_{v2} \\ &= g_{mM6} (r_{oM6}||r_{oM7}) \left(\frac{g_{mM3} + g_{mM5}}{2} \right) (r_{oM3}||r_{oM5}) \qquad (4.2) \end{aligned}$$

Note that the signal path at the output node is only through transistor M6. Therefore, considering the case that the amplifier is driving a load which requires sinking and sourcing large currents, this opamp would be able to source a large current, although it is not capable of sinking a current greater than I_B,
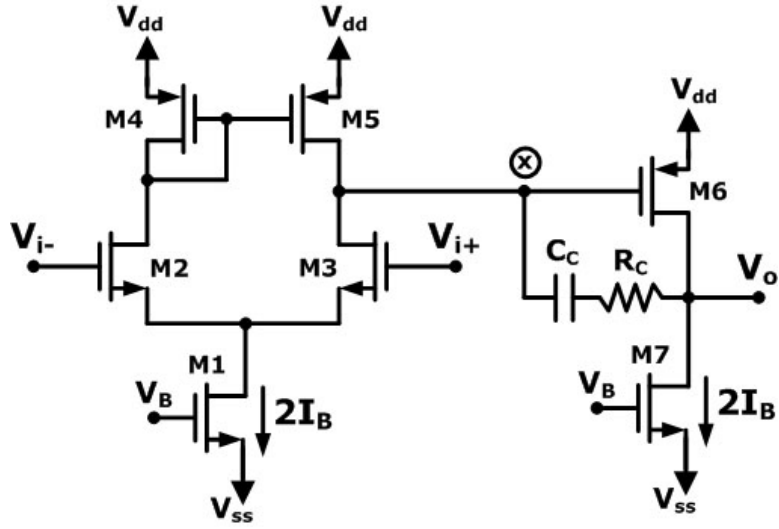
Figure 4.1: Conventional 2-stage Operational Amplifier.

the quiescent current in M7. In this design the devices R_C and C_C are needed for frequency compensation.

Observe that it is a 2-stage amplifier, which has two high-impedance nodes, x and the output node. Therefore, it requires frequency compensation, which is achieved through Miller compensation composed, of C_c and R_c. For a more detailed description of Miller compensation refer to Appendix A.

Let's now consider the case of the conventional Operational Transconductance Amplifier (OTA), as shown in Fig. 4.2. This amplifier is capable of sinking and sourcing $2I_B$ at the output node. Transistors M8 and M9 are the only transistors that offer significant gain. Therefore, it is a one-stage amplifier. Note that transistors M4, M5 and M7 are diode connected. Thus, the gain given by transistors M2, M3 and M6 is approximately unity. The OTA does not offer as high a gain as the conventional opamp, and it has only one high-impedance node.
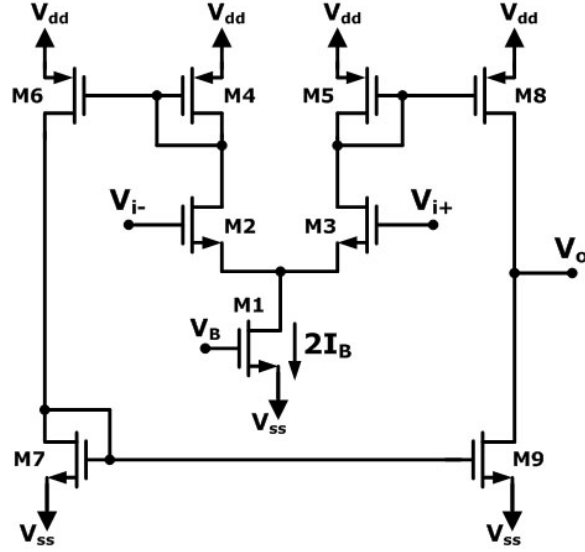
Figure 4.2: Conventional Operational Transconductance Amplifier

Therefore, the OTA does not require frequency compensation, which in some cases occupies considerable silicon area.

The OTA shown in Fig. 4.2 has only one gain stage. We can get a second gain stage using the transistors in the differential pair in the same manner as in circuit in Fig. 4.1 by eliminating the diode connections in transistors M4 and M5, which creates high impedance at nodes x and y. The resulting scheme is shown in Fig. 4.3(a) where the first stage consists of transistors M1 through M5, whereas the second stage is composed of M6 through M9. This structure now behaves as a Class-AB two-stage differential amplifier with a single-ended output. Observe that M1 sets the biasing current for the differential pair but the quiescent current in transistors M6-M9 is uncertain; therefore, it has to be controlled in some manner. Note that by controlling the voltage V_{ctrl} we can control the source-to-
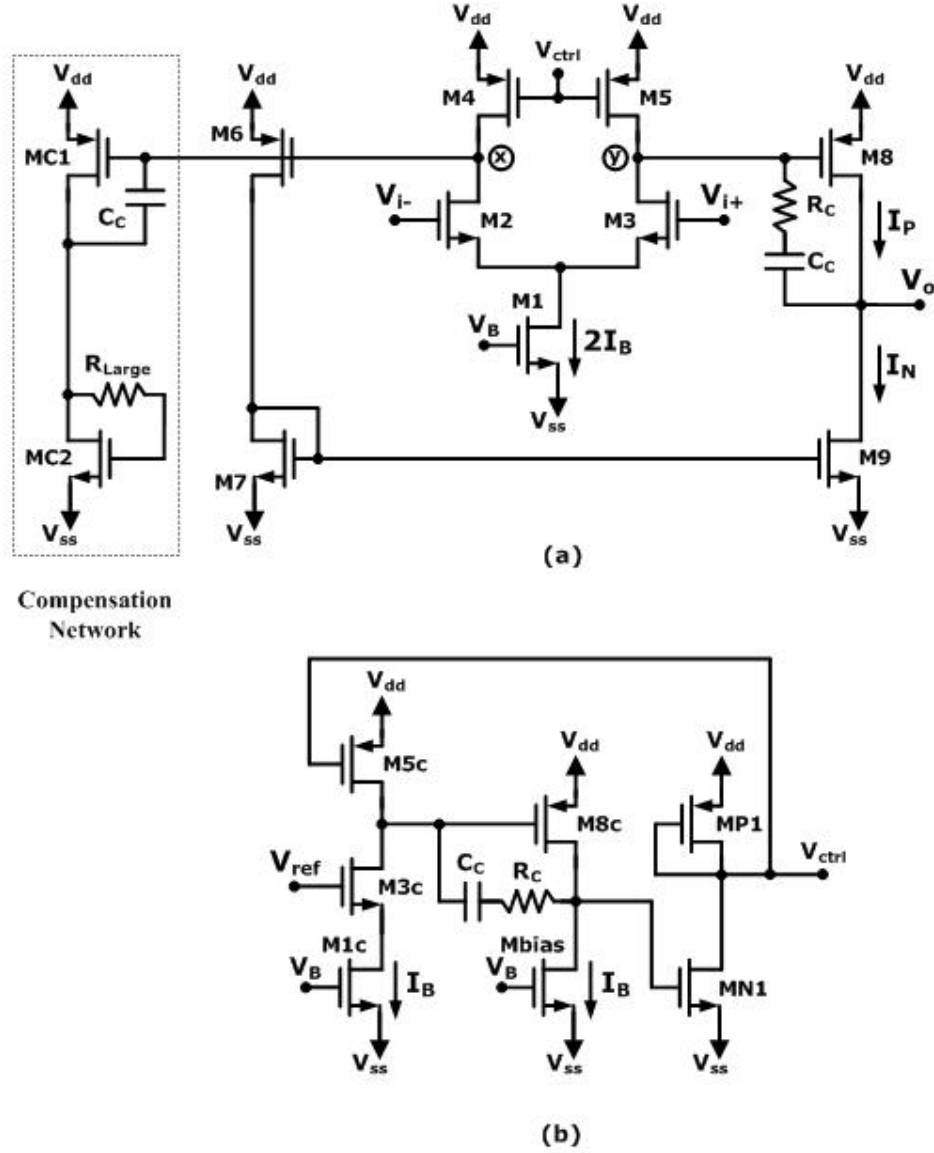
Figure 4.3: a) Proposed differential 2-stage Class-AB amplifier with b) quiescent current control circuit.

gate voltages of transistors M4 and M5. V_{SGM4} and V_{SGM5} control the currents

going into nodes x and y and, thus, indirectly control the V_{SG}'s of transistors M6

and M8, in order to set their quiescent currents.

For that purpose, we used the quiescent control circuit reported in [26]. A control circuit adapted to this design is shown in Fig. 4.3(b). Observe that it replicates part of the operating circuit. Transistors M1c, M3c and M5c replicate transistors M1, M3 and M5 in the differential pair in Fig. 4.3(a). M8c replicates M8 in the second stage and Mbias acts as a current source, which sets the desired biasing current in M8. MN1 and MP1 are included to give a third unity-gain stage, in order to achieve negative feedback. The negative feedback sets the correct voltage V_{SG} in M5. By this approach, V_{ctrl} has the right value to let V_{SGM5} give the proper current to set the right V_{SGM8c} in order for M8 to have the current I_B. Thus, we can use V_{ctrl} to set the biasing current in M6 and M8 in the circuit in Fig. 4.3(a).

Observe that this circuit has three high impedance nodes, x, y and the output node. A large capacitance can be created at node y using Miller compensation with the gain provided by M8. Unfortunately, the same approach cannot be used for node x, as transistor M6 has unity gain. And using the gain from transistor M9 would result in positive feedback if the compensation goes from node x to the output. Therefore we can use the "Capacitance Multiplication" [27] technique to achieve a large effective capacitance at node x. It consists of a transistor MC1 which provides gain for a Miller compensation with the capacitor C_C. the resistor R_{large} has zero current under DC conditions. This allows transistor MC2 to be diode connected and have the smae bias current as M7, and in small signal it

reflects a large impedance, of the value R_{large}. With this, we can get the same 3dB frequency at both nodes, x and y.

Simulations were performed using SpectreS in a 0.5μm CMOS technology. The design parameters are as specified in Table 4.1. The total supply voltage is 3V in order to achieve a wide input-output operational range. The minimum power supply requirements are merely $V_{GSM2,3} + V_{DSM1}^{sat} + V_{in}^{swing}$, the same as in a regular amplifier based on an NMOS differential pair in the input stage. The values for the compensating capacitor C_C and resistor R_C are 20pF and 0.5kΩ, respectively, following the frequency compensation criteria described in Appendix A.

Table 4.1: Design Parameters of the Circuits in Fig. 4.3.

Parameter	Value
I_B	100μA
$V_{DS}^{sat} = V_{GS} - V_T$	0.5V
$V_{T_{NMOS,PMOS}}$	0.7V, 0.9V
$(w/l)_{NMOS}$	9μm / 1.2μm
$(w/l)_{PMOS}$	26μm / 1.2μm
$V_{dd} - V_{ss}$	3V
C_L	15pF

The circuit in Fig. 4.3 was tested as a voltage follower. Fig. 4.4 shows the DC transfer characteristic of the circuit in Fig. 4.3 and its derivative, which demonstrates a very high linearity. Fig. 4.5 shows the experimental results of the DC transfer characteristic. The Total Harmonic Distortion was calculated to

get a more precise measure of linearity. The proposed structure has a THD of 0.00795% for a sinusoid input signal of $0.5V_p$.
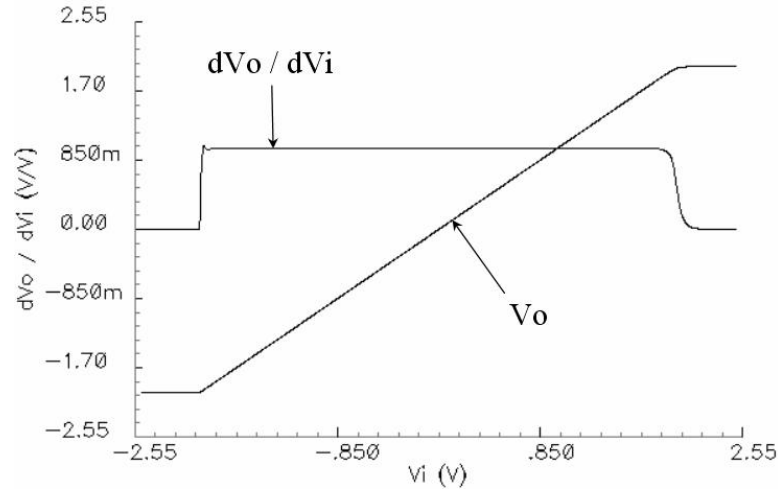
Figure 4.4: DC transfer characteristic and its derivative for the circuit in Fig. 4.3.
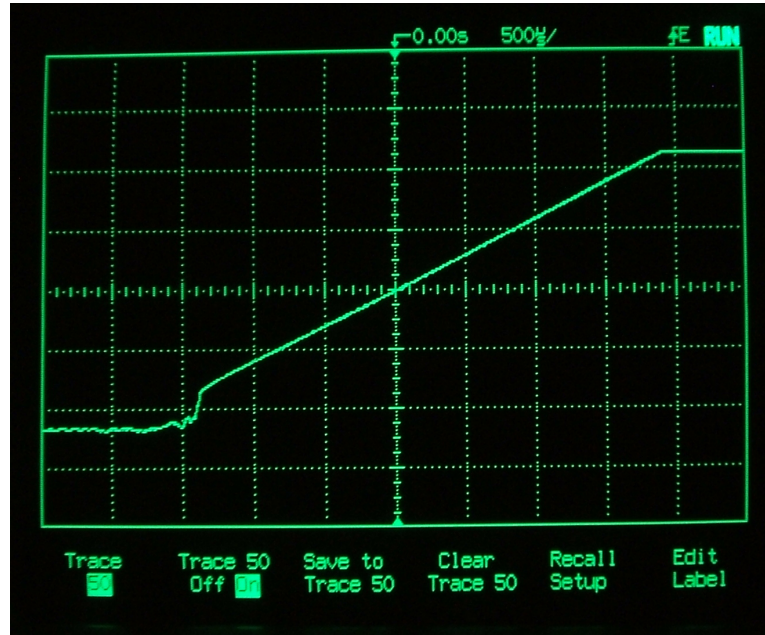
Figure 4.5: Experimental results of the DC transfer characteristic of the circuit in Fig. 4.3.

Fig. 4.6 shows the Class AB operation of the circuit in Fig. 4.3. Currents I_P and I_N are the currents across transistors M8 and M9, respectively. Transistors M8 and M9 are two times the size of the other transistors, in order to satisfy the requirements of large currents at the output. Fig. 4.7 shows the AC analysis of the circuit. It has an open-loop gain A_v = 68dB, a bandwidth of BW = 2kHz, a Gain-Bandwidth product of GBW = 5MHz and a phase margin of 76deg when driving a load of 15pF. Fig. 4.8 shows the simulation results of a transient analysis. A square signal of 1Vpp at 5MHz was applied at the input. Observe the Class AB operation, as the output node is sourcing and sinking large currents when driving a loading capacitor of C_L = 15pF. The measured slew rate SR+ = 4.01V/μsec and SR- = 5.83V/μsec. The measured settling times are t_{s+} = 474.4nsec and t_{s-} = 275nsec. Fig. 4.9 shows the experimental results of the transient analysis for the same parameters as for simulation. In this case the measured slew rate is SR+ = 3.73V/μsec and SR- = 4.87V/μsec. Fig. 4.10 shows the microphotograph of the fabricated circuit. As we mentioned before, the Class AB operation allows to source and sink large currents at the output node, which permits the output voltage to reach the desired value in a small period of time. Observe that the conventional two-stage amplifier in Fig. 4.1 is a Class A amplifier. It can source a large current, but the maximum current it can sink is I_B. This enhances the falling settling time, which is around 275nsec, compared to the conventional of 478nsec. In this case the settling time is enhanced in a factor 2.
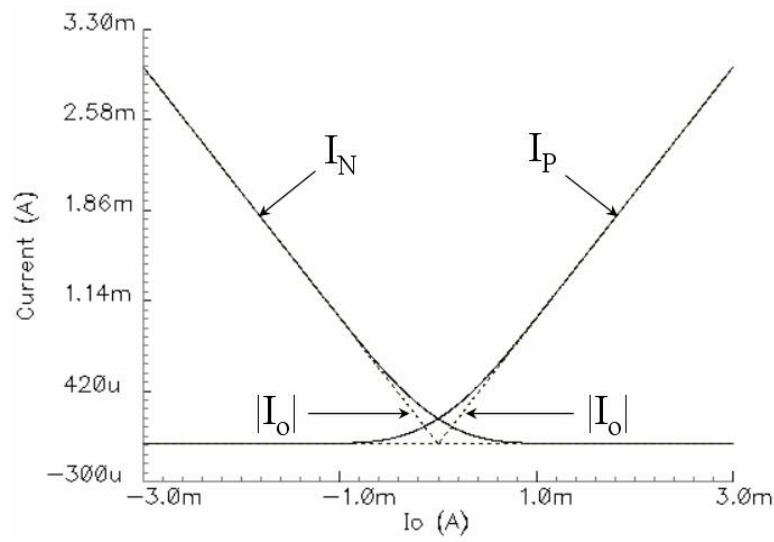
Figure 4.6: Currents in the output stage showing the Class-AB operation of circuit in Fig. 4.3.
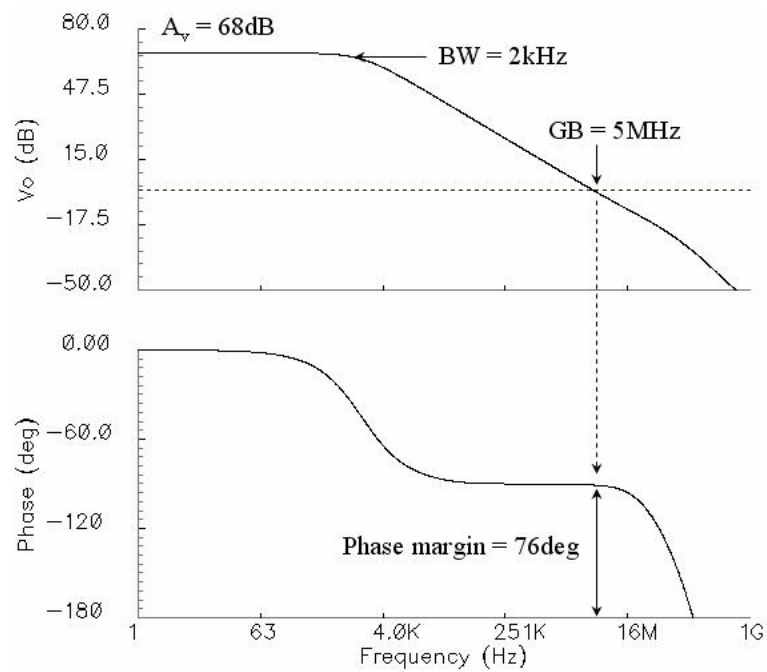
Figure 4.7: Frequency response of the circuit in Fig. 4.3.
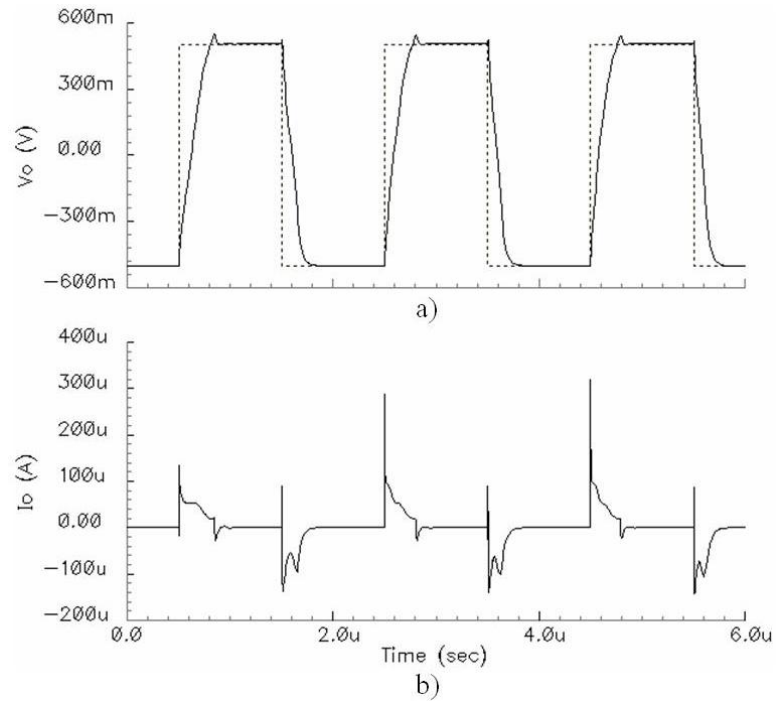
Figure 4.8: a) Output voltage and b) output current of the circuit in Fig. 4.3 when performing a transient analysis using a $1V_{pp}$ square wave at 5MHz.
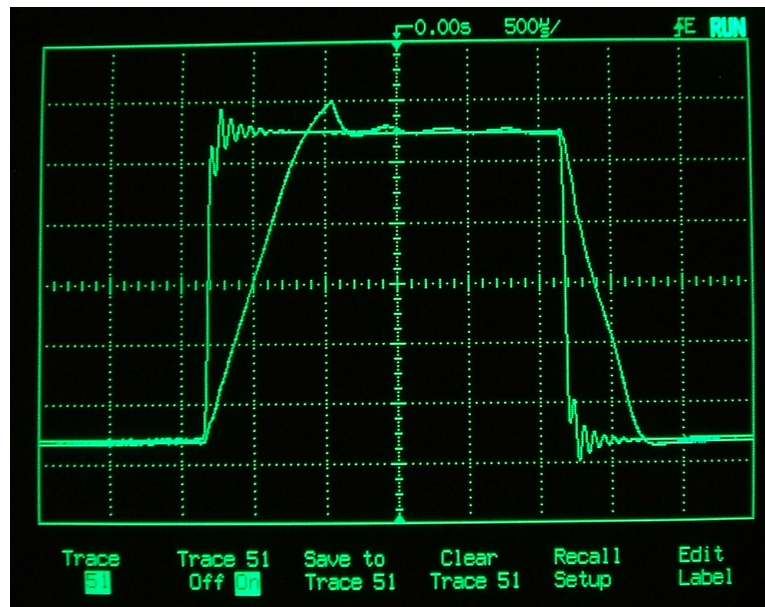
Figure 4.9: Experimental results of the output voltage of the circuit in Fig. 4.3 when performing a transient analysis using a $1V_{pp}$ square wave at 500kHz.
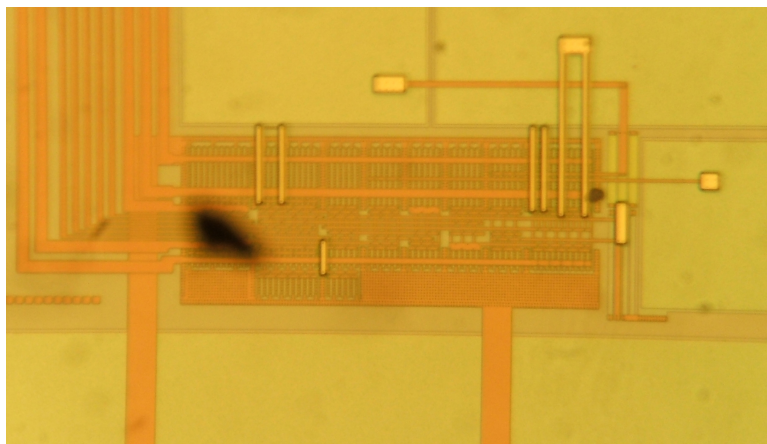
Figure 4.10: Microphotograph of the fabricated circuit in Fig. 4.3, 220μm x 90μm.

Another approach proposed for this structure is to include a third gain stage at both nodes x and y, as shown in Fig. 4.11(a). According to the compensation schemes presented in [28], also described in Appendix A. For a three-stage amplifier, only the second stage needs to be compensated to get a stable system. On the other hand, the control circuit used in [28] to set biasing conditions also needs compensation.

The design parameters are the same as those specified in Table 4.1. In this case, as it is a three-stage amplifier, the a capacitor $C_C = $ 30pF and a resistor $R_C = $ 1kΩ were used. The circuit in Fig. 4.11 was tested in the same manner. Fig. 4.12 shows the DC transfer characteristic of the circuit in Fig. 4.11 and its derivative, which shows a very high linearity. Fig. 4.13 shows the experimental results of the fabricated circuit. The Total Harmonic Distortion was calculated to get a more precise measure of linearity. The proposed structure has a THD of 0.00795% for a sinusoid input signal of $0.5V_p$.
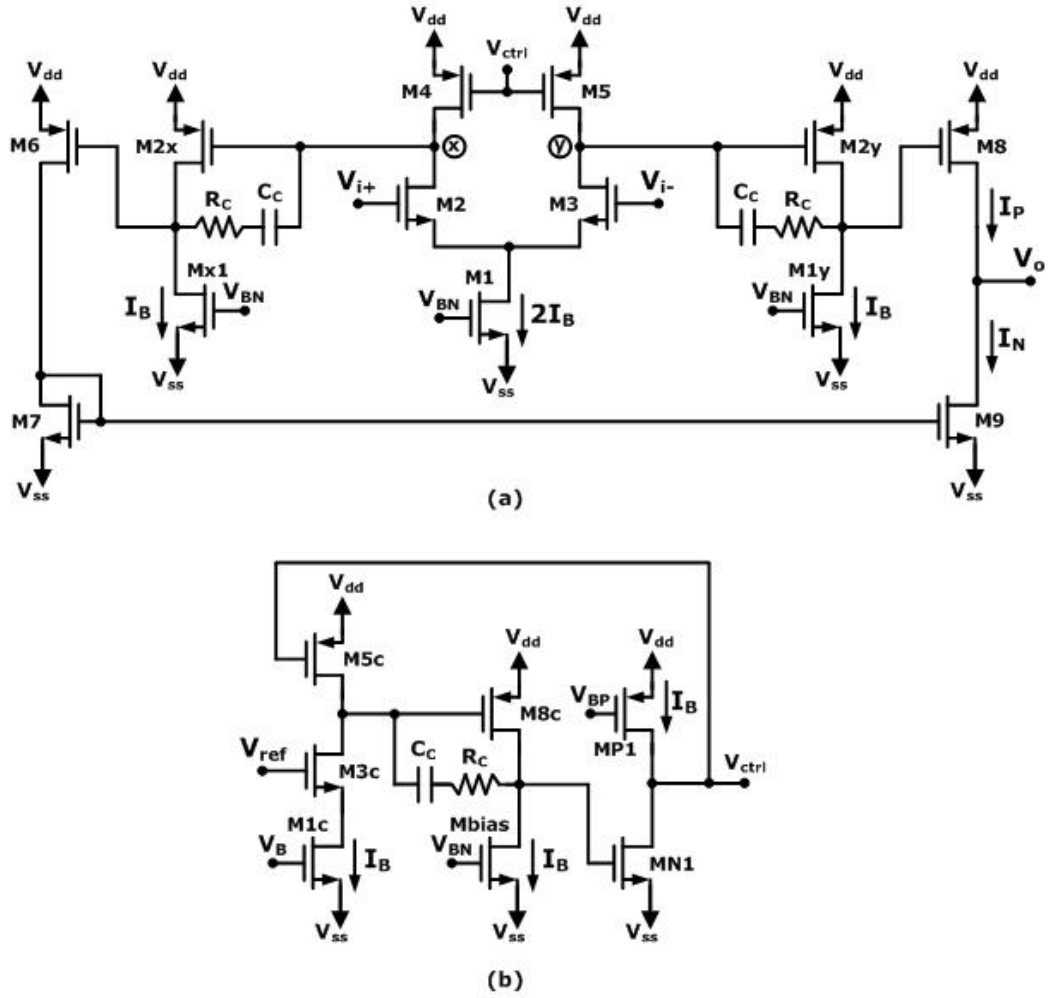
Figure 4.11: a) Proposed differential 3-stage Class-AB amplifier with b) quiescent current control circuit.

Fig. 4.14 shows the Class-AB operation. Currents I_P and I_N are the currents across transistors M8 and M9, respectively. Transistors M8 and M9 are two times the size of the other transistors, in order to satisfy the requirements of large currents at the output. Transistors M1x, M2x, M1y and M2y are three times the size of the other transistors in order to sink and source the charge from the compensating capacitors C_C whenever abrupt changes occur in the output
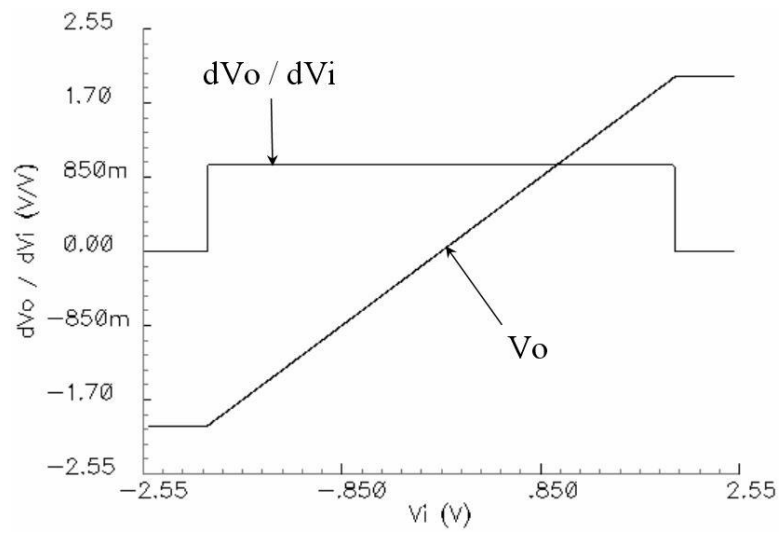
Figure 4.12: DC transfer characteristic and its derivative of the circuit in Fig. 4.11.

Figure 4.13: Experimental results of the DC transfer characteristic of the circuit in Fig. 4.11.
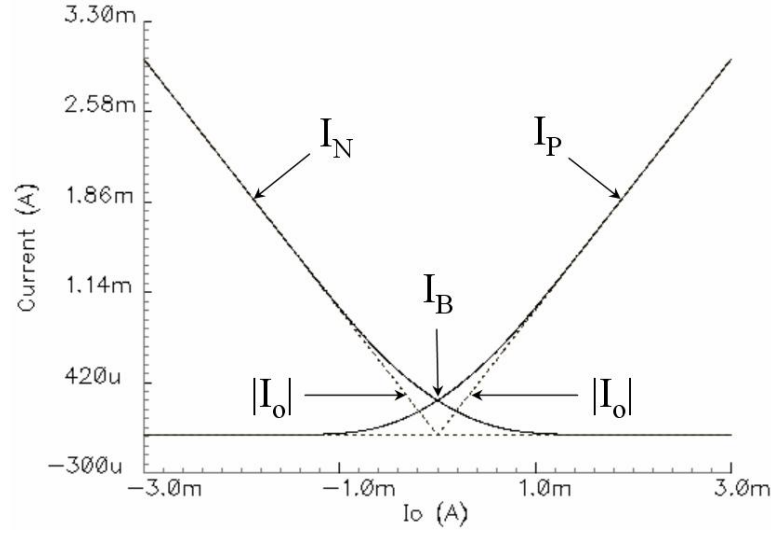
Figure 4.14: Currents in the output stage showing the Class-AB operation of circuit in Fig. 4.11.

node. Fig. 4.15 shows the AC analysis of the circuit. It has an open-loop gain $A_v = 102$dB, a bandwidth of BW $= 350$Hz, a Gain-Bandwidth product of GBW $= 45$MHz and a phase margin of 55deg when driving a load of $C_L = 15$pF. Fig. 4.16 shows the simulation result of a transient analysis. A square signal of $1V_{pp}$ at 5MHz was applied at the input. Observe the Class AB operation as the output node is sourcing and sinking large currents when driving a loading capacitor of $C_L = 15$pF. The measured slew rate SR+ $= 23.06$V/μsec and SR- $= 21.7$V/μsec. Fig. 4.17 shows the experimental results of the transient analysis for the same parameters as for simulation. In this case the measured slew rate is SR+ $= 19.04$V/μsec and SR- $= 19.04$V/μsec. Fig. 4.18 shows the microphotograph of the fabricated circuit.
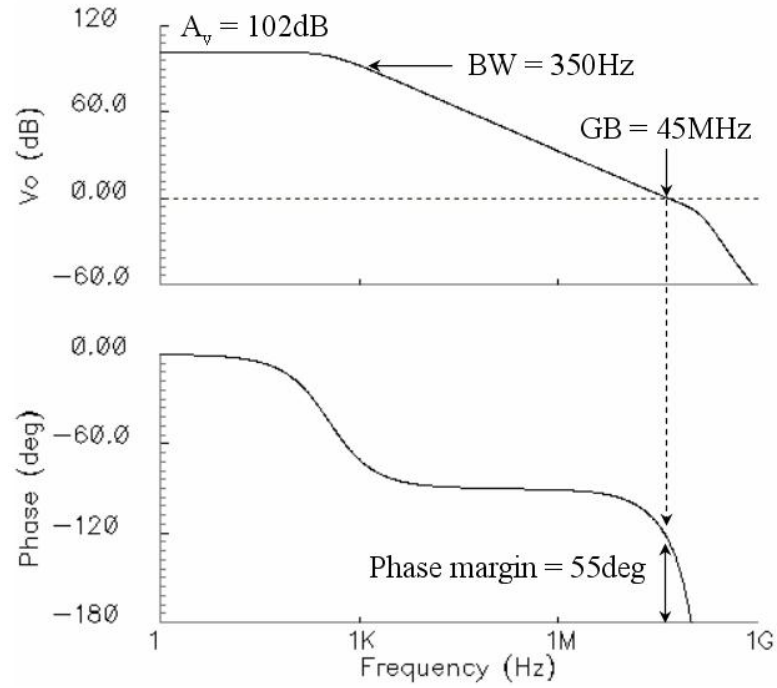
Figure 4.15: Frequency response of the circuit in Fig. 4.11.

The Class AB operation provides the capability of a fast charge and discharge of the load capacitance. This architecture has three gain stages, which provide a higher transconductance to the amplifier. The slew rates are SR+ = 23.06V/μsec and SR- = 21.7V/μ compared to the conventional two-stage opamp in Fig. 4.1 which has SR+ = 10.21V/μsec and SR- = 4.71V/μ. This enhances the SR+ in a factor 2.5 and the SR- in a factor 5.
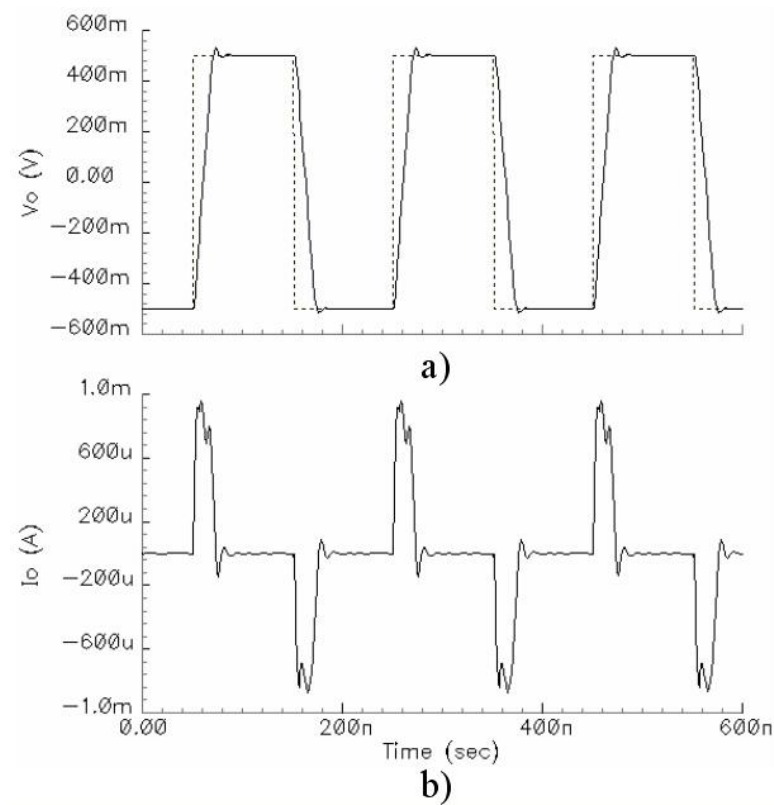
Figure 4.16: a) Output voltage and b) output current of the circuit in Fig. 4.11 when performing a transient analysis using a $1V_{pp}$ square wave at 5MHz.
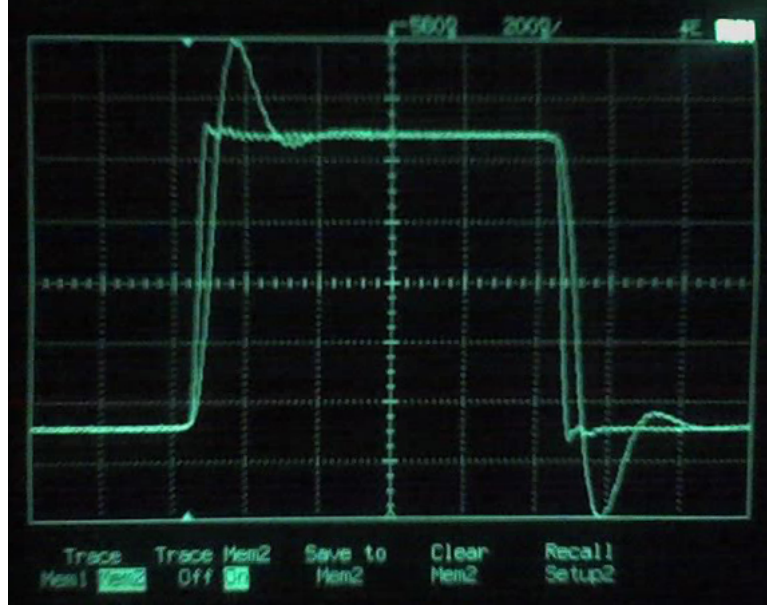
Figure 4.17: Experimental results of the output voltage of the circuit in Fig. 4.11 when performing a transient analysis using a $1V_{pp}$ square wave at 500kHz.
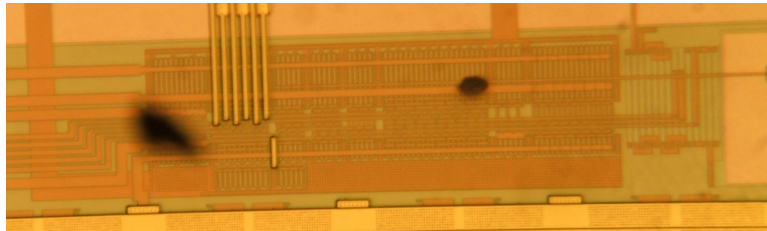
Figure 4.18: Microphotograph of the fabricated circuit in Fig. 4.3, 280μm x 90μm.

5 CONTROL CIRCUIT IMPLEMENTED USING DUAL-POLARITY FLOATING BATTERY FOR CLASS AB OUTPUT STAGES

This chapter presents different structures of floating batteries reported in the past utilized to provide Class AB operation to output stages. The biasing technique described in Chapter 3 is utilized to obtain the design of a battery with the ability to adopt positive and negative values for high- and low-voltage applications.

One of the most commonly used low-voltage output buffers was proposed by Monticelli [29]. Modified structures of Monticelli's work have been reported in [23, 30], but their main limitation is the minimum power supply requirements. Monticelli's design is based on a floating battery that provides swing at the gate terminal of both of the output devices driving a capacitive or resistive load. Other modifications of floating batteries have also been reported in [31, 32], and other variations, such as the battery with negative voltage reported in [25] for low-voltage applications.

Fig. 5.1 shows the conceptual circuit that illustrates the principle of the floating battery. This circuit is often used in Class AB output stages where a large sourcing and sinking current is desirable. The purpose of this design is to ensure that both transistors have the capability to adjust their gate-to-source voltages V_{GS} to satisfy the current demand at the output node. Class AB output stages

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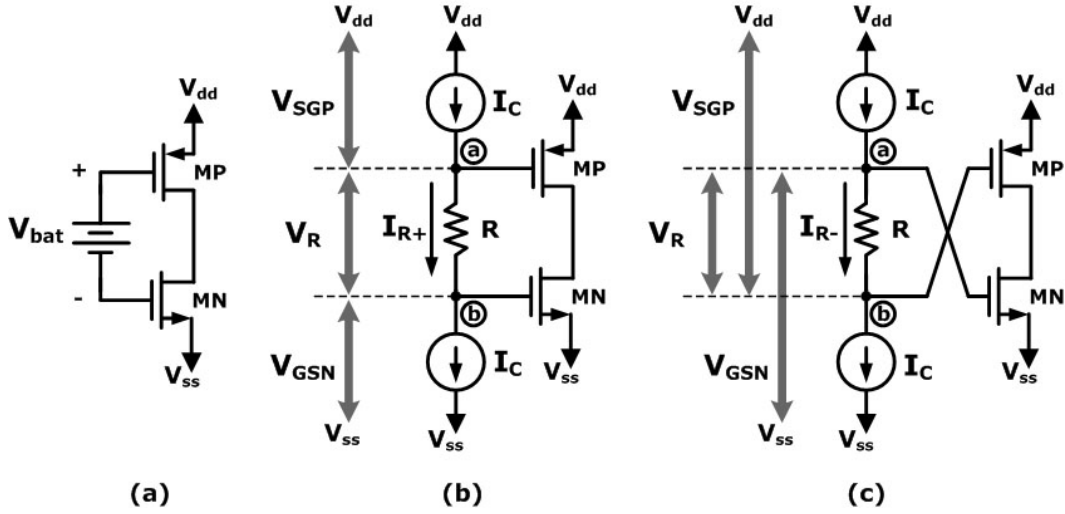
Figure 5.1: a) Conceptual circuit of a battery for Class AB operation, b) Positive battery, used when $V_{dd} > V_{SGP} + V_{GSN}$ and c) Negative battery used when $V_{dd} < V_{SGP} + V_{GSN}$.

offer an advantage over the Class-A output stages where only one transistor has that capability and the other is limited to sink or source a fixed bias current.

Some approaches use the voltage across a resistor or a gate-to-source voltage of a transistor to set the voltage V_{bat}, which necessitates a controlling circuit to set the current that adjusts that voltage V_{bat}. Note that V_{bat} must set the gate-to-source voltages of transistors MN and MP to the correct value, in order to give the desired quiescent current in the output transistors.

The voltage V_{bat} depends on the supply voltages V_{dd} and V_{ss}. Observe that the larger the difference between these two voltages, the larger the voltage V_{bat} must be. In quiescent conditions, V_{bat} is used to maintain a constant V_{SGP} and V_{GSN} at the output transistors, so as to keep their quiescent currents equal to I_B.

Fig. 5.1(b) shows the implementation of the floating battery using the voltage across a resistor R. Let us assume that the negative rail voltage V_{ss} is 0V. In this case, if the voltage V_{dd} increases, we would require the current I_R to increase in order to maintain the same bias current in the output transistors. The minimum voltage V_{dd} can take is $V_{GSMP} + V_{GSMN}$. In this case, the voltage V_{bat} would be 0V and the current across the resistor would need to be 0A.

The circuit in Fig. 5.1(c), reported in [25], is used in low-voltage applications. Here the gate terminals of MN and MP are switched compared to the previous case. They are connected to node a and b, respectively; therefore the gate terminal of transistor MP takes a value below the gate terminal of MN. Here the upper limit for V_{dd} is $V_{GSMP} + V_{GSMN}$; note that this is the lower limit of the previous case. The lower limit it can adopt is the greatest V_{GS} among transistors MN and MP plus one V_{DS}^{sat} for the current source I_C. For some technologies the PMOS threshold voltage is higher that that of the NMOS, therefore $V_{SGMP} + V_{DS}^{sat}$ would be the minimum value V_{dd} can take. This condition can be viewed as a negative voltage V_{bat} across the resistor, as illustrated in the schematic. A circuit that gets the desired value of I_C is reported in [26].

The purpose of the proposed circuit is to combine both approaches described in Fig. 5.2(a) and (b), so as to have a battery with the capability to adopt positive and negative voltages, that is, having a resistor that, under high

values for V_{dd}, passes current in one direction and, under low values for V_{dd}, passes current in the other direction.

Fig. 5.3 illustrates the implementation of the proposed circuit, which includes several stages. The first stage is the positive / negative battery. It includes transistors MP+ and MN+, which provide the current I+ which goes from nodes a to b and gives a positive value to the voltage V_{bat} following the design from Fig. 5.2(a). In the same manner, it includes transistors MP- and MN-, which provide the current I- that goes from nodes b to a and gives a negative value to V_{bat} as implemented in circuit in Fig. 5.2(b). The next stage sets the quiescent voltages V_{GSN} and V_{SGP} in transistors MQ1 and MQ4 at nodes a and b, respectively. Observe from Figs. 5.2(a) and (b) that this stage is common for both approaches; therefore, it is included only once in the proposed circuit. The next stage to be included is the third unity-gain stage, also common to both circuits in Figs. 5.2(a) and (b). Following the analogy from circuits in Fig. 5.2, transistor MQ4 leads to the subsequent stage that generates the signal V_{p+} in Fig. 5.2(a) and the signal V_{n-} in Fig. 5.2(b). In the same manner MQ1 leads to the stage that generates the signal V_{n+} from Fig. 5.2(a) and V_{p-} from Fig. 5.2(b), as illustrated in the schematic. Note that the output generated by MQ4 is a gate-to-source voltage for the NMOS transistor MP1 when generating V_{p+} and at the same time generates the source-to-gate voltage for the PMOS transistor MN4 when generating V_{n-}; therefore, having the gate terminal of these two transistors connected may result
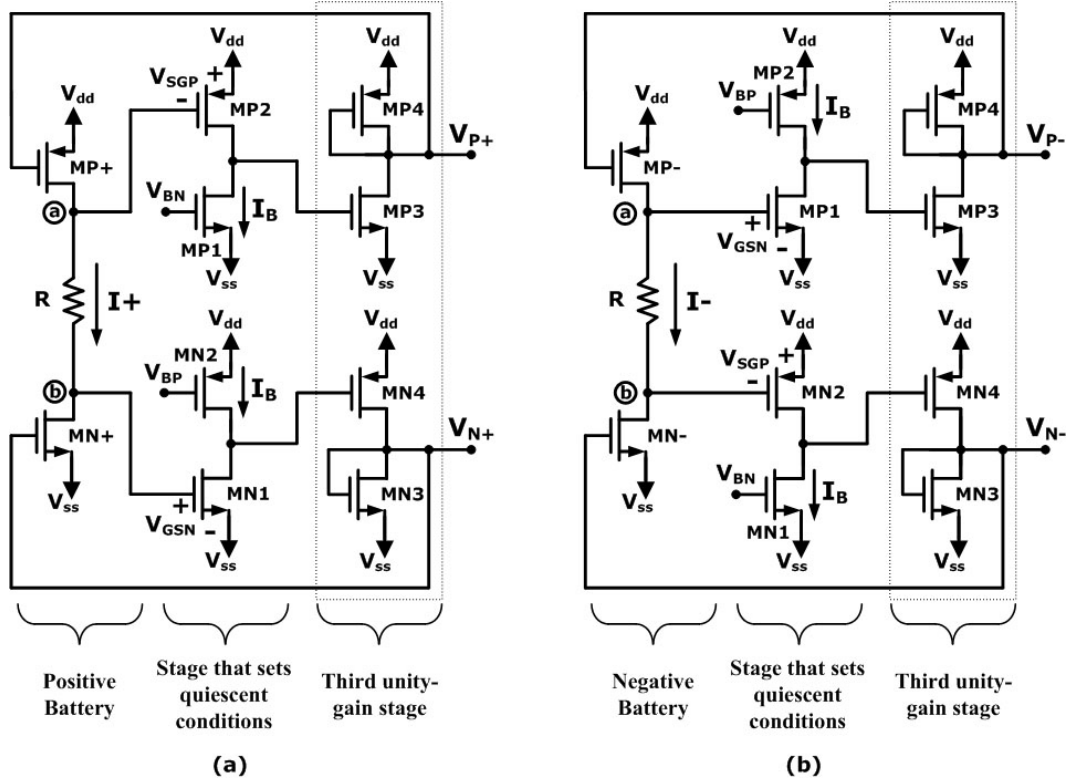
Figure 5.2: a) and b) implementation of circuits in Figs. 5.1(a) and (b), respectively.

in a large gate-to-source voltage if V_{dd} also increases. The result would be large DC currents. Thus, an extra positive battery with the same currents generated by V_{p+} and V_{n+} has to be included to maintain the currents in MP1 and MP4 constant and equal to I_B. In the same manner another positive battery must be added to keep the currents in MN2 and MP3 constant and equal to I_B.

Simulations were performed using SpectreS in a $0.5\mu m$ CMOS technology. The design parameters are as specified in Table 5.1. Fig. 5.4 shows the simulated DC transfer characteristic of the circuit in Fig. 5.3. Here, V_{dd} is swept from 0V to 4V, whereas V_{ss} is kept constant at 0V. It can be inferred from the plot that the
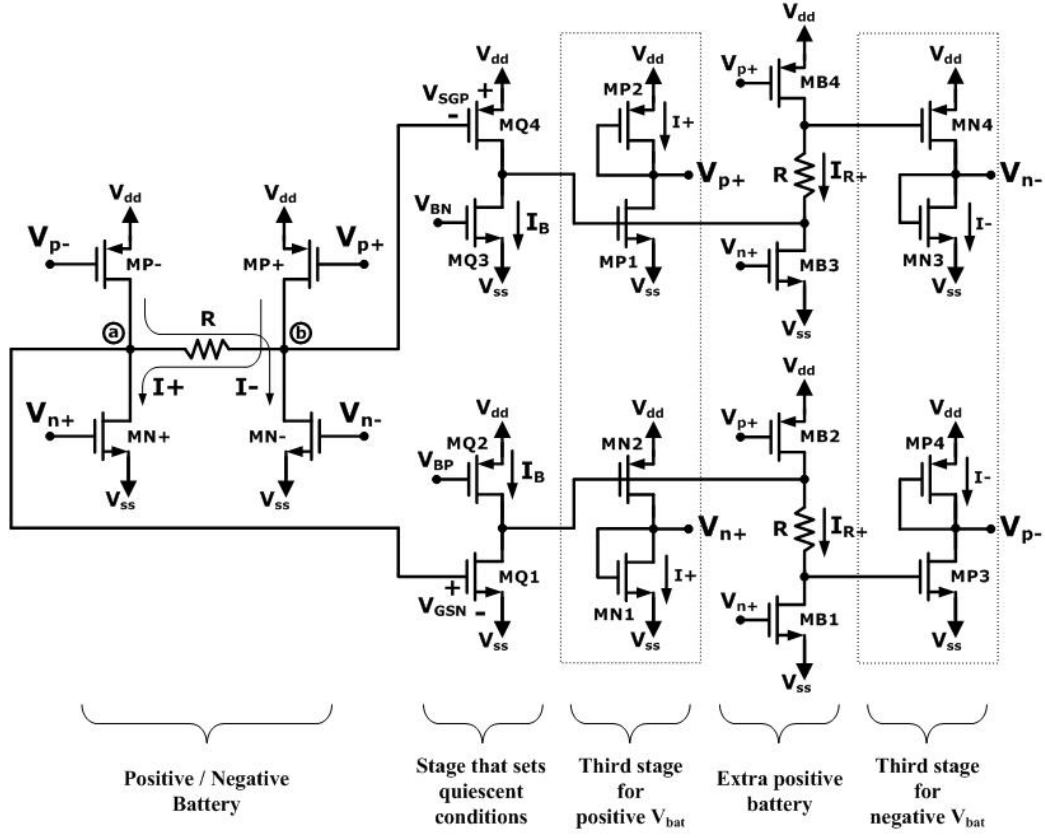
Figure 5.3: Proposed circuit using a combination of circuits in Figs. 5.2(a) and (b).

voltage at node b, V_b, follows the voltage V_{dd} level-shifted by V_{SGP}, the quiescent V_{SG} of MQ4. Similarly, the voltage at node a remains constant with respect to V_{ss}, level-shifted by V_{GSN}, the quiescent V_{GS} of MQ1. Consider the fact that, since MN1 and MP2 are diode connected, they consume the same current as I+ as well; therefore for large values of V_{dd} the power consumption becomes rather large.

Note that by having transistors MN1, MN3, MP2 and MP4 diode connected, they will have the same current I+ as found in MP+ and MN+. If V_{dd} is

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Table 5.1: Design Parameters.

Parameter	Value
I_B	$100\mu A$
$V_{DS}^{sat} = V_{GS} - V_T$	0.5V
$V_{T_{NMOS,PMOS}}$	0.7V, 0.9V
$(w/l)_{NMOS}$	$9\mu m$ / $1.2\mu m$
$(w/l)_{PMOS}$	$26\mu m$ / $1.2\mu m$
V_{dd}	variable
V_{ss}	0V
R	$10k\Omega$
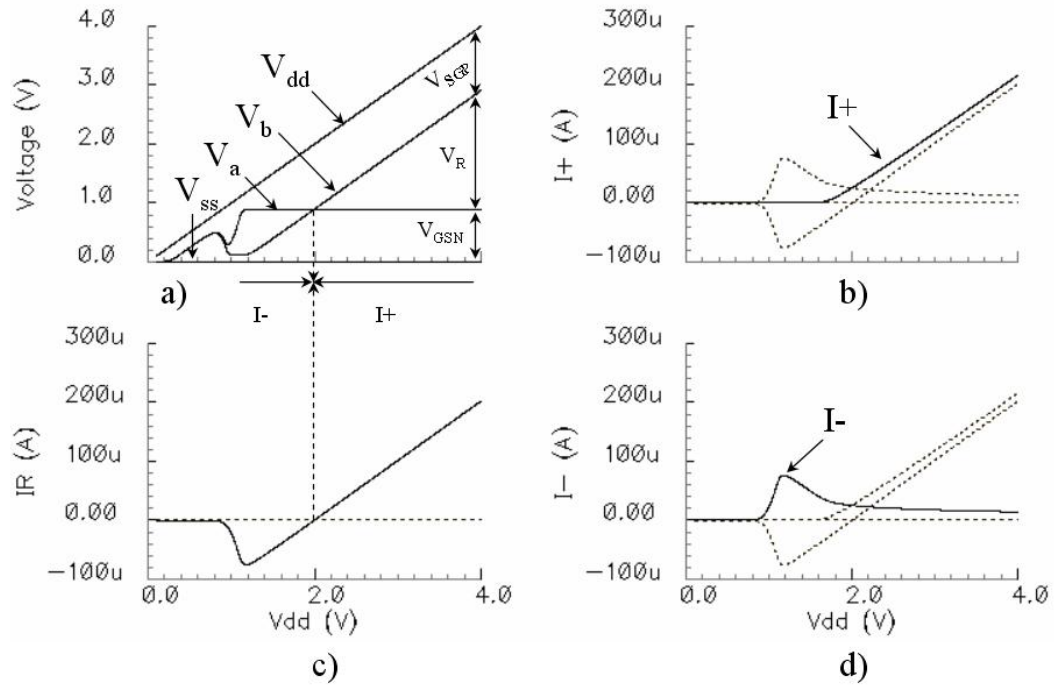
Figure 5.4: DC transfer characteristic of circuit in Fig. 5.3 showing a) voltages V_{GSN} and V_{SGP}, and currents b) I+, c) IR and d) I-.

increases considerably, the current I+ also increases. Therefore, the overall circuit would need to establish the current I+ in three different branches, instead of only one. Therefore, to save power, the unity-gain stage can be excluded in this scheme and transistors MN2, MN4, MP1 and MP3 can provide gain. However, the circuit now becomes a 3-stage amplifier, for which the compensation becomes rather difficult, if the circuit is intended to be used dynamically, rather than statically. The resulting structure is illustrated in Fig. 5.5. Fig. 5.6 shows the simulated DC transfer characteristic of the circuit in Fig. 5.5, where the diode connection of transistors MN1, MN3, MP2 and MP4 is eliminated and the power consumption is decreased.

Note that the voltage across the resistor R is negative for values of V_{dd} below $V_{GSP} + V_{GSN}$; in this range of operation, the current I- provided by transistors MP- and MN- has a non-zero value, whereas the current I+ provided by MP+ and MN+ is zero. At the point where V_{dd} is equal to $V_{GSP} + V_{GSN}$ currents I+ and I- are equal to zero. As V_{dd} goes above that value, I+ provided by MP+ and MN+ takes a non-zero value, whereas I- remains equal to zero. Fig. 5.7 shows the overlapped currents to illustrate the positive and negative values of the current IR provided by I+ and I-.

Fig. 5.8 shows the experimental DC transfer characteristic and Figs. 5.9 and 5.10 show the microphotograph of the fabricated circuits in Figs. 5.3 and 5.5, respectively.
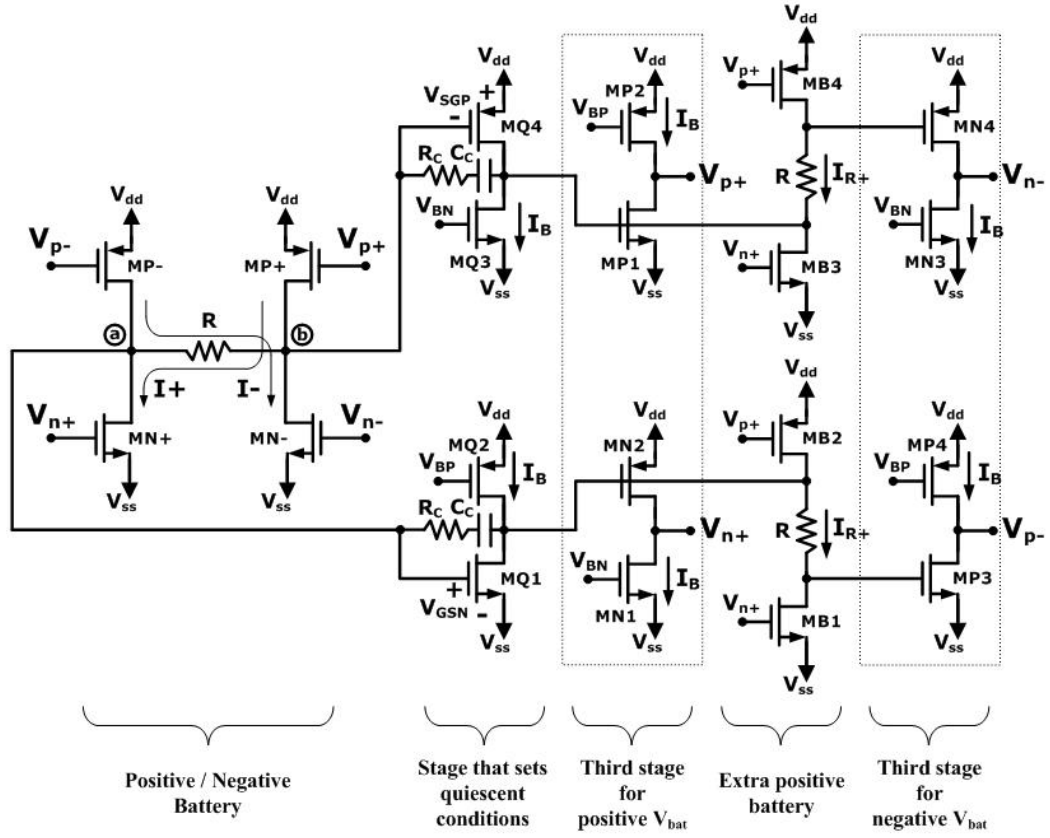
Figure 5.5: Proposed circuit using a combination of circuits in Fig. 5.2(a) and (b) and eliminating the diode connection in the third stage.

We used the compensation technique described in [28] for multi-stage amplifiers, in which the compensation for a three-stage amplifier is designed to have Miller compensation in the second stage only. The values for a compensating capacitor C_C and resistor R_C are 30pF and 1.75kΩ, respectively, following the pole-zero equations specified in [28]. A square input signal V_{in} of 200mV_{pp} at 100kHz was added to the biasing voltages V_{BP} and V_{BN}, in order to show the stability of the circuit. The results in Figs. 5.11 and 5.12 show the voltage wave-
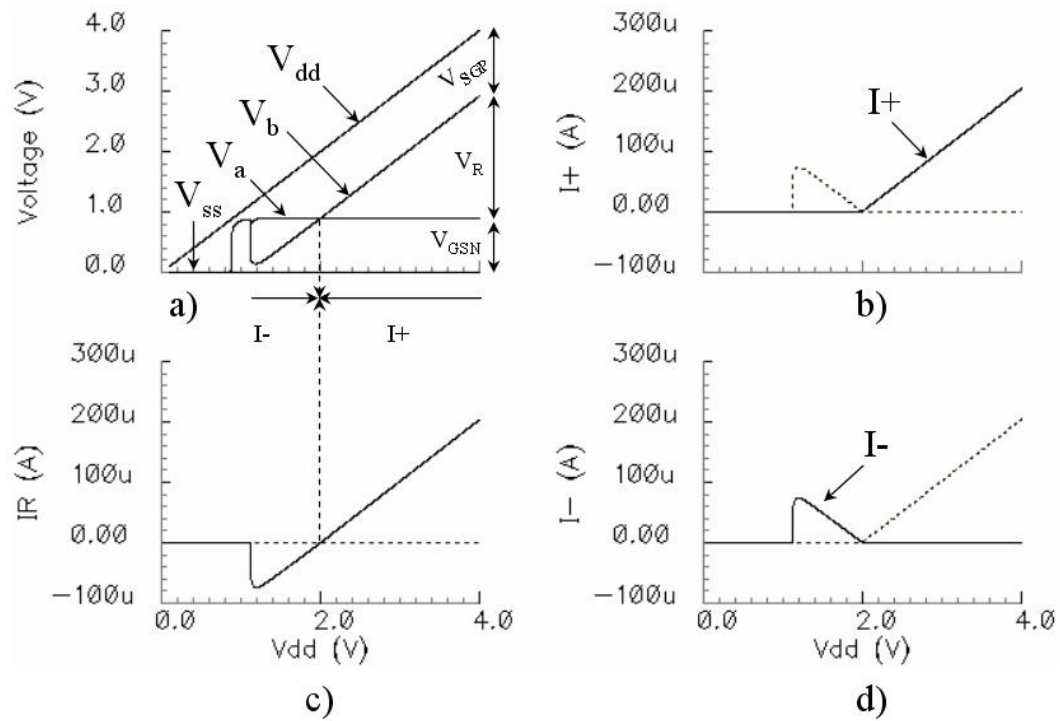
Figure 5.6: DC transfer characteristic of circuit in Fig. 5.5 showing a) voltages V_{GSN} and V_{GSP}, and currents b) I+, c) IR and d) I-.

forms at the input signal and at nodes a and b of the circuits in Figs. 5.3 and 5.5, respectively.

In order to test the capability of the battery to provide Class AB operation, we used it in a common Class A 2-stage amplifier. Fig. 5.13 shows the implementation. Fig. 5.13(a) is a conventional 2-stage amplifier, where the gates of M6 and M7 are connected through the battery. Fig. 5.13(b) is a replica of the voltage level shift from the circuits in Fig. 5.3 or Fig. 5.5. The voltages V_{oN} and V_{oP} are the nodes of the battery and are connected to the gate of transistors M6 and M7 in Fig. 5.13(a), so as to provide swing to both of these transistors. Then,
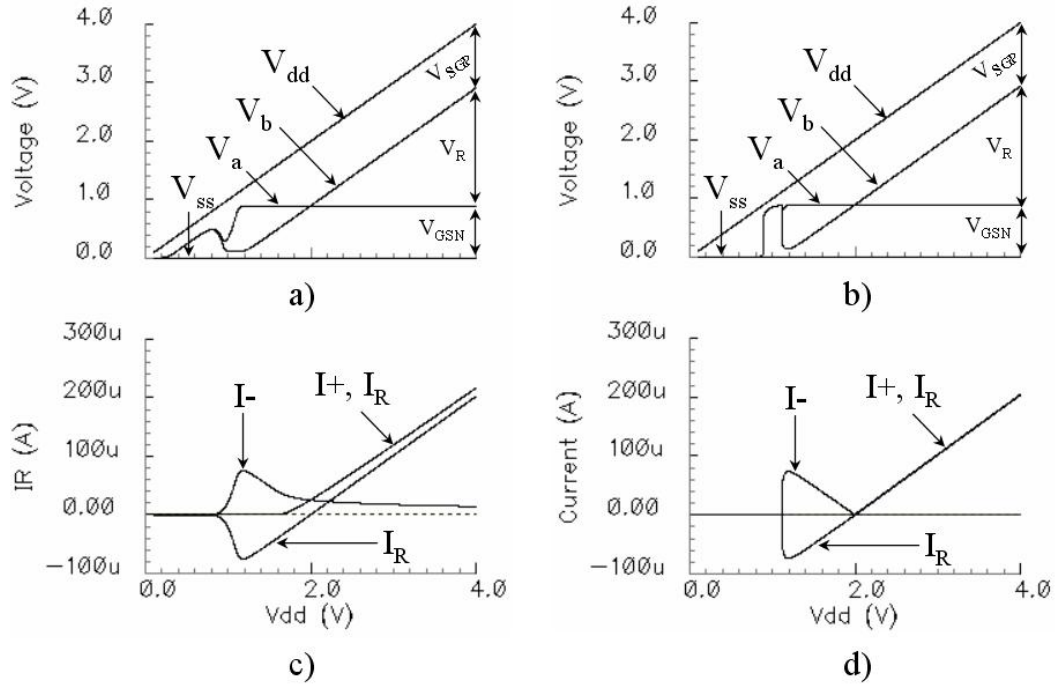
Figure 5.7: Comparison of the DC transfer characteristic of the proposed circuits, showing a) the voltages and b) currents of circuit in Fig. 5.3 and c) voltages and d) currents of circuit in Fig. 5.5
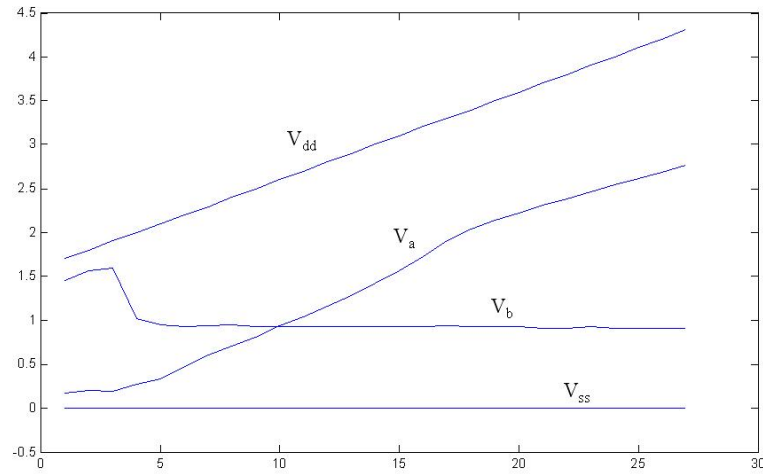
Figure 5.8: Experimental results of the DC transfer characteristic of circuits in Figs. 5.3 and 5.5
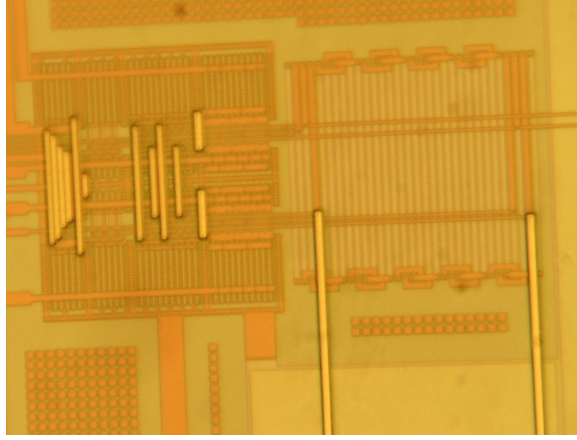
Figure 5.9: Microphotograph of the fabricated circuit in Fig. 5.3. 120μm x 133μm
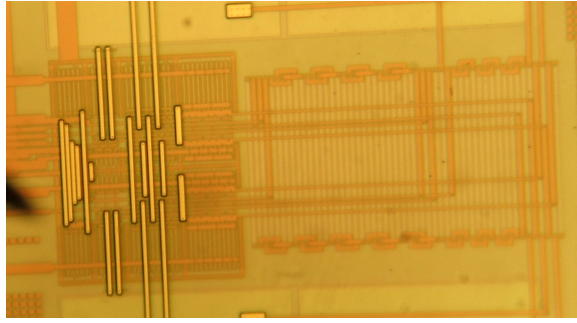
Figure 5.10: Microphotograph of the fabricated circuit in Fig. 5.5. 120μm x 133μm

voltages V_{p-}, V_{p+}, V_{n-} and V_{n+} are the voltages from the circuit in Fig. 5.3 or Fig. 5.5.

Figs. 5.14(a) and (b) show the Class AB operation of the circuit in Fig. 5.13 when using the battery in Fig. 5.3 and Fig. 5.5, respectively.

Figs. 5.15(a) and (b) show the transient analysis of the circuit in Fig. 5.13 when using the battery in Fig. 5.3 and Fig. 5.5, respectively. A pulse wave signal of $1V_{pp}$ at 500kHz was used as the input. It has a measured slew rates of SR+ = 4.77μsec and SR- = 4.73μsec when using the battery in Fig. 5.3 and SR+ =
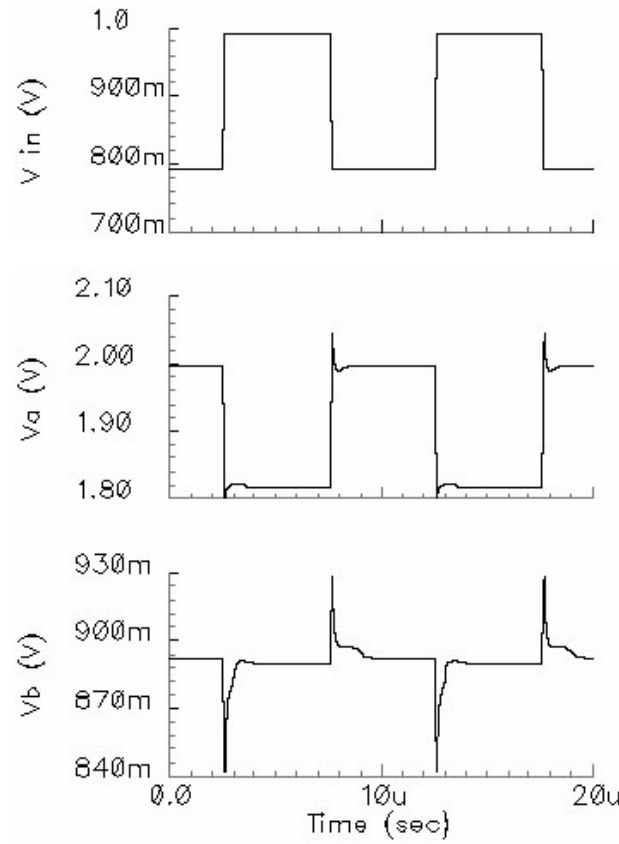
Figure 5.11: Transient analysis of circuit in Fig. 5.3 using a square input signal of 200mV at 100kHz and voltages at nodes a and b.

4.79μsec and SR- $= 4.73\mu$sec when using the battery in Fig. 5.5. The settling times are $t_{s+} = 773$nsec and $t_{s-} = 796$nsec when using the battery in Fig. 5.3, and $t_{s+} = 779$nsec and $t_{s-} = 790$nsec when using the battery in Fig. 5.5. Note that these numbers are very similar. The difference comes in power consumption in the case of the battery in Fig. 5.3 if the supplies are increased considerably, and stability in the case of the battery in Fig. 5.5 if a sinusoidal wave is being used as the input signal.
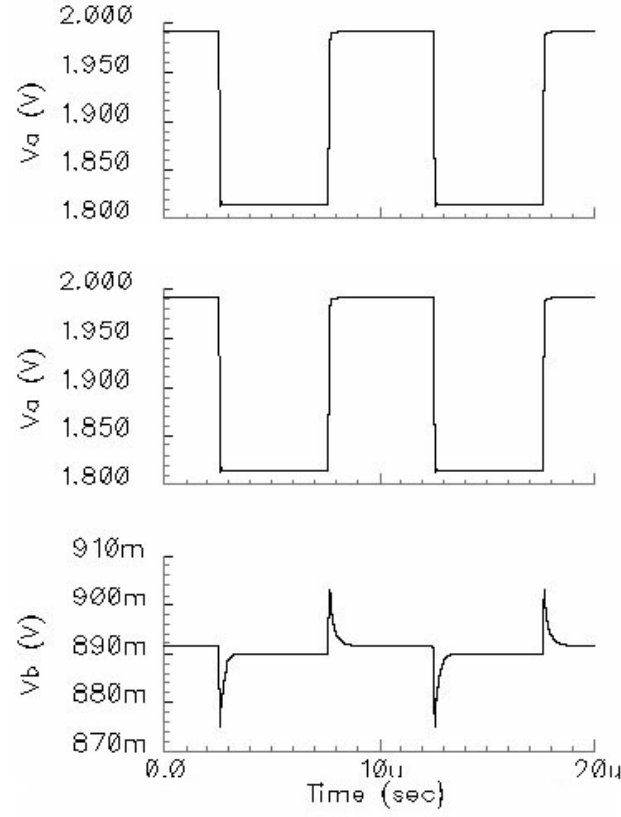
Figure 5.12: Transient analysis of circuit in Fig. 5.5 using a square input signal of 200mV at 100kHz and voltages at nodes a and b.
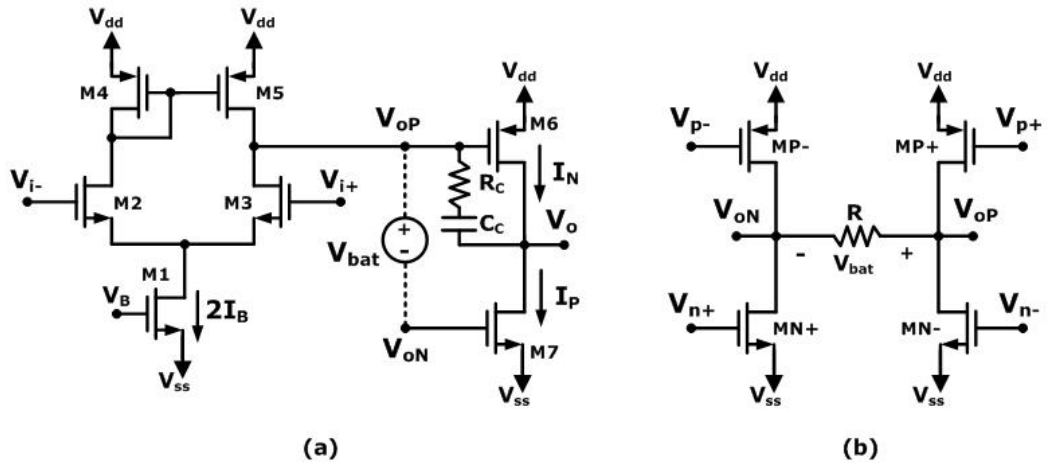
Figure 5.13: a) A Conventional 2-stage CMOS amplifier with b) the level-shift of circuit in Fig. 5.3 or Fig. 5.5.
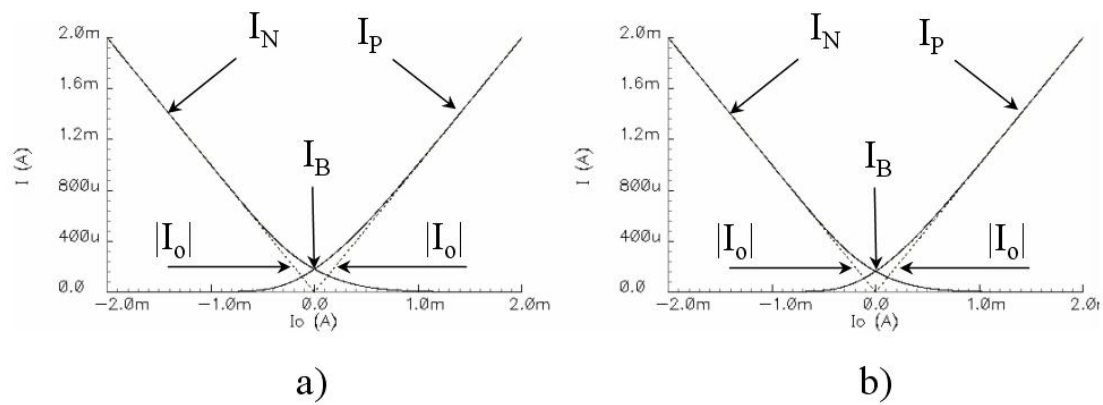
Figure 5.14: Class AB operation of circuit in Fig. 5.13 when using a) the battery in Fig. 5.3 and b) the battery in Fig. 5.5.
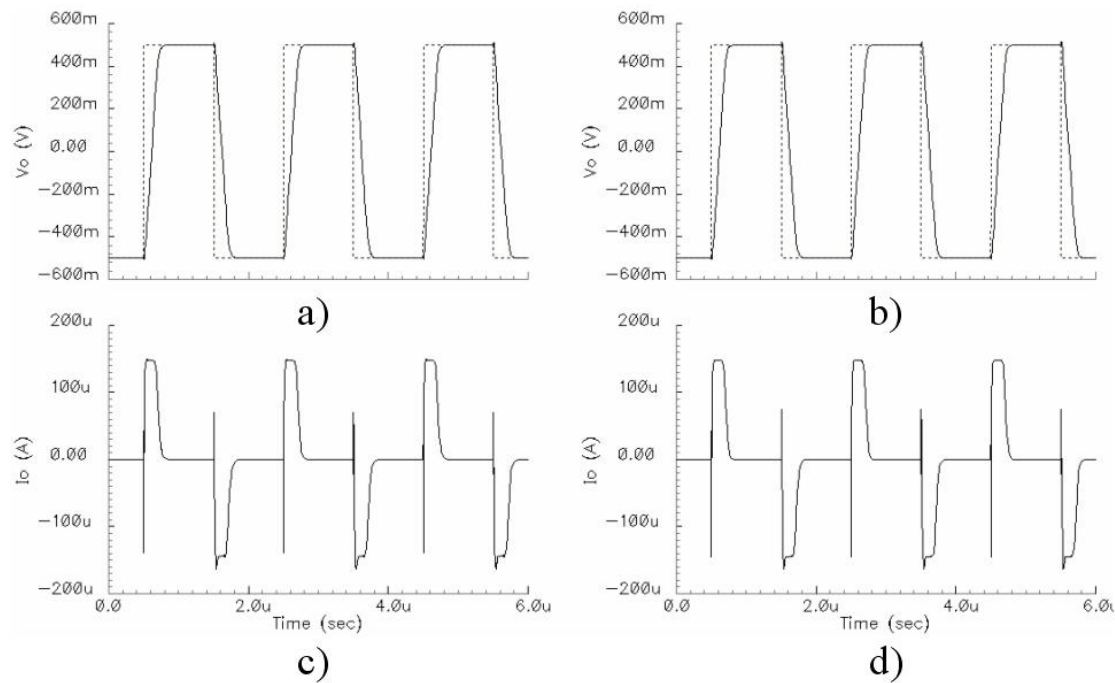
Figure 5.15: Transient analysis of circuit in Fig. 5.13 when using a) the battery in Fig. 5.3 and b) the battery in Fig. 5.5.

The Class AB operation provided by the batteries in Figs. 5.3 and 5.5 enhances the settling time of the amplifier in Fig. 5.13. The raising settling time is around 770nsec, and it remains very similar compared to the conventional amplifier, which is 670nsec. In the other hand, the falling settling time of the proposed structures is around 790nsec, compared to the conventional, which is 980nsec. In this case the settling time is enhanced in a 20%.

6   CONTROL CIRCUIT IMPLEMENTED IN CLASS AB OUTPUT BUFFER

This chapter describes the design of an output buffer using complementary common-source transistors in the output stage. Also, the difficulty of controlling the bias current in the output stage is identified. Then the biasing technique described in Chapter 3 is implemented on the Class AB buffer to control the quiescent current in the output stage, independent of the supply voltage.

One area of analog VLSI where a lot of research has been done is the design of buffers with a Class-AB output stage to drive capacitive or resistive loads [33, 34, 35].

The design of buffers presents a variety of requirements, such as the maximum size of the driving devices in the output stage and accurate control of their DC bias current. In order to control the biasing current in the output stage, many designs have been previously reported, such as in [33, 36, 37]; however, they introduce other limitations, such as reduced dynamic range or very large transistors in the output stage. In this chapter, we consider the design of a buffer with an output stage of moderate size, capable of driving large capacitive loads; also it consists of trhee gain stages which give it a very high open-loop gain, allowing the circuit to work at very high frequencies.

Fig. 6.1 shows a Class-AB output buffer using the output devices in a complementary common-source configuration [33, 34, 35]. The output transistors
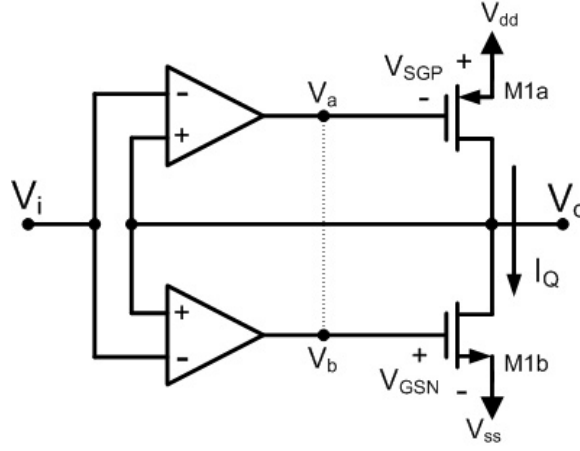
Figure 6.1: Class-AB output buffer with complementary common-source transistors in the output stage.

M1a and M1b are capable of providing large sourcing and sinking currents at the output node. The opamps sense the voltage difference between the input and the output of the buffer, in order to drive the gates of the output transistors so as to make this difference as small as possible. Some authors refer to this circuit as a common-source configuration with error amplifiers.

Note from the schematic that the opamps have the same input voltages. Therefore, neglecting mismatched parameters due to the fabrication process, the outputs also have approximately the same voltage. This can be viewed as a virtual connection between the outputs as shown in the diagram. This represents an important limitation in the design of the buffer, as the gate-to-source voltages V_{GS} in the output transistors, as well as the quiescent current across them, have a strong dependence on the supply voltages V_{dd} and V_{ss}. This relation is specified

Figure 6.2: DC operation of the circuit in Fig. 6.1 showing a) DC voltages as the voltage rails increase and b) currents in the output transistors.

in the expression in (6.1)

$$V_{dd} - V_{ss} = V_{SGP} + V_{GSN} \tag{6.1}$$

For this reason, the supply voltages must be well controlled to achieve the desired quiescent current at the output transistors M1a and M1b and prevent crossover distortion as the supply rails decrease and excessive power dissipation as the supply rails increase.

Fig. 6.2 shows the operation of the circuit in Fig. 6.1. Observe from Fig. 6.2(a) that V_a and V_b remain at the same potential as the voltage rails increase. This causes the voltages V_{SGP} and V_{GSN} to increase also, which leads to an increase in the static current, as shown in Fig. 6.2(b). This results in significant power consumption.
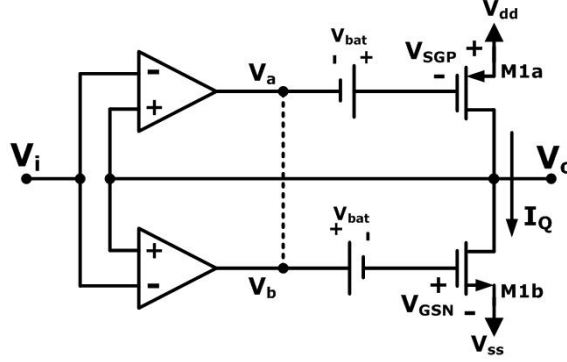
Figure 6.3: Diagram of the Class-AB output buffer with the implementation of batteries to control the static current in the output transistors.

The goal of implementing the technique described in Chapter 3 is to keep the voltages V_{SGP} and V_{GSN} constant to maintain the currents in the output transistors also constant. Therefore, we need to implement a battery between nodes a and b to adjust their voltages to the right value referred to the corresponding rail so as to give the desired value to V_{SGP} and V_{GSN}, as shown in Fig. 6.3.

Fig. 6.4 shows the block diagram of the proposed design. Opamps A_{1a} and A_{1b} provide the low impedance property at the output node by giving the capability to the output transistors to sink and source large currents, whereas the amplifiers A_{2a} and A_{2b} set the right DC voltage at nodes a and b to have the desired V_{SGP} and V_{GSN} of transistors M1a and M1b under static conditions. The operation of these amplifiers is based on comparing the V_{SGP} and V_{GSN} of the output transistors against the desired voltage under quiescent operation. If these voltages are not equal, the amplifiers make the correction to nodes a and b until

Figure 6.4: Block diagram of the implementation of the Class-AB output buffer and the batteries.

the two inputs are equal and the desired value is achieved, regardless of the value of the supply voltages.

Observe that the amplifiers A_{2a} and A_{2b} are used to give a voltage level shift to amplifiers A_{1a} and A_{1b}. Therefore, they can be implemented within the same cell. Fig. 6.5 shows the implementation. In this design the differential pair composed of M2a and M3a is used as a transconductance amplifier, whereas the differential pair composed of M2b and M3b is used to implement a voltage level shift on the transconductance amplifier, as shown in Fig. 6.6. Here, a differential input signal is applied to transistors M2a and M3a and a differential voltage level shift is applied to transistors M2b and M3b.

Figure 6.5: Error Amplifier with a differential pair for the input signal and a differential pair for a voltage level shift.
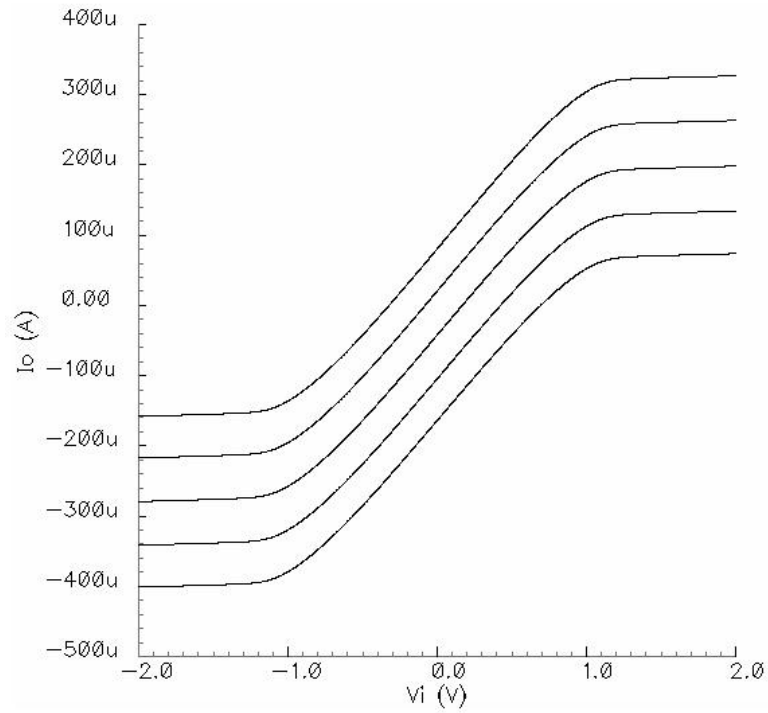
Figure 6.6: DC transconductance of amplifier in Fig. 6.5, as five different values of voltage level shift are applied to inputs V_{ctrl+} and V_{ctrl-}.
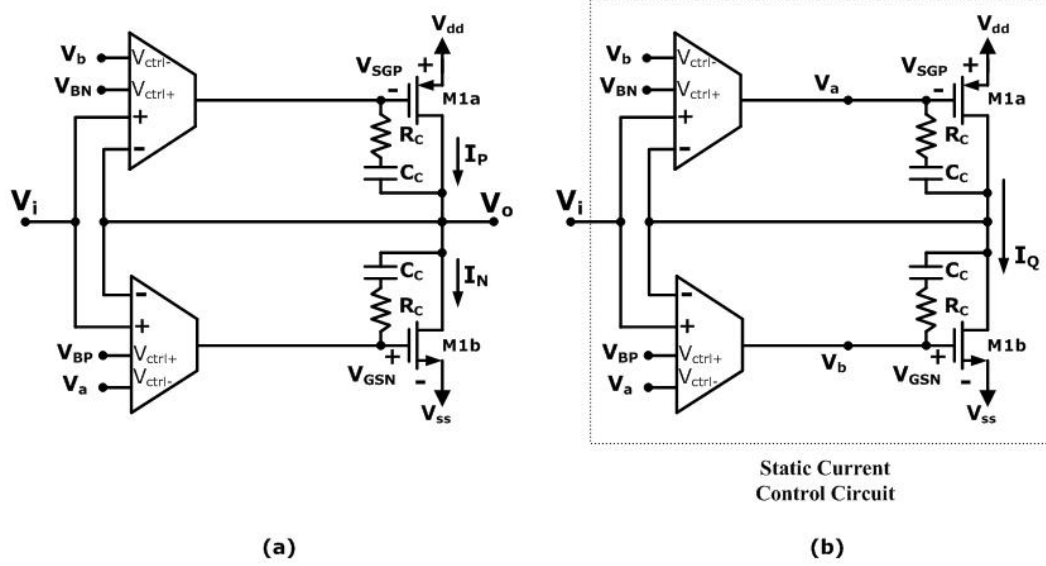
Figure 6.7: a) Class-AB output buffer with accurate current control and b) Control Circuit.

The overall circuit, including the amplifiers with the voltage level shift, is shown in Fig. 6.7. Here, V_{BP} and V_{BN} are the quiescent voltages, V_{SG} and V_{GS}, of a PMOS and an NMOS respectively, operating under quiescent bias conditions. Voltages V_a and V_b are the voltages at nodes a and b respectively. Fig. 6.7 is the output circuit, whereas Fig. 6.7(b) is the Control Circuit that sets the proper voltages V_{SGP} and V_{GSN} for the output circuit of Fig. 6.7(a). Note that the Control Circuit is a replica of the output circuit, working under static conditions, and can be scaled down, so as to reduce the silicon area and the power consumption.

The DC operation of the circuit in Fig. 6.7 is shown in Fig. 6.8. Observe in Fig. 6.8(a) that the values of V_{SGP} and V_{GSN} remain constant as the supply voltages increase. This causes the current in the output devices to remain constant, as shown in Fig. 6.8(b). The slight increase is due to channel length modulation
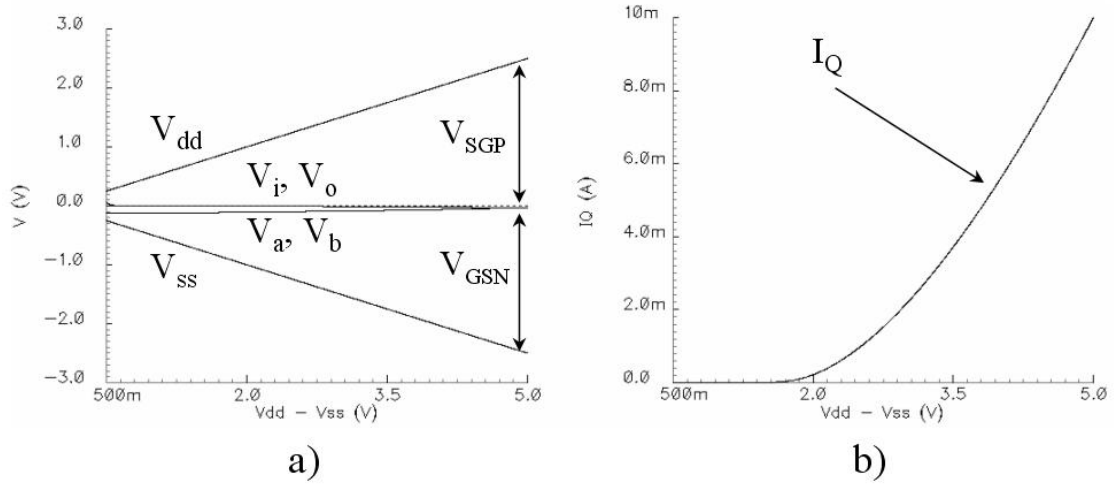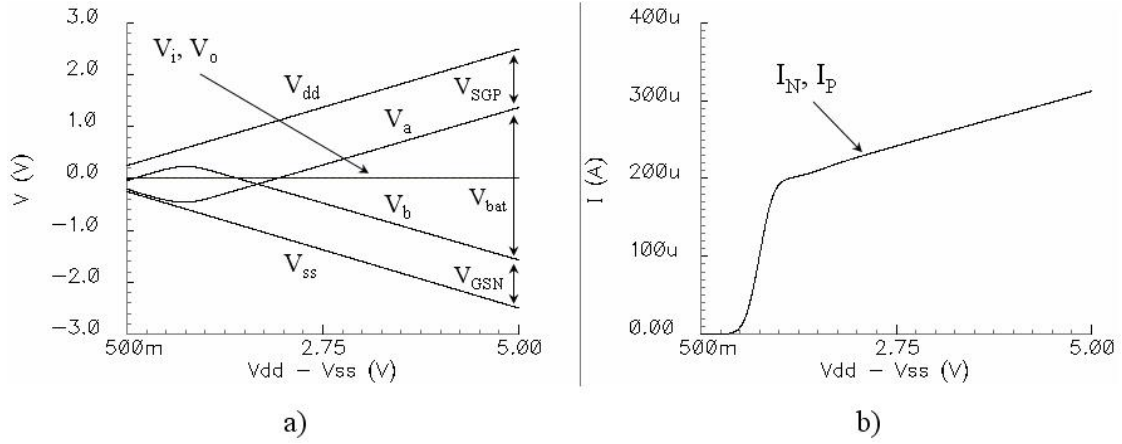
Figure 6.8: DC operation of the circuit in Fig. 6.7 showing a) DC voltages as the voltage rails increase and b) currents in the output transistors.

of the output transistors, which represents a very small variation compared to the case in Fig. 6.1.

Simulations were performed using SpectreS in a 0.5μm CMOS technology. The design parameters are as specified in Table 6.1. Fig. 6.9 shows the simulated DC transfer characteristic of the circuit in Fig. 6.7 and its derivative, which presents a very high linearity. Fig. 6.10 shows the experimental results of the DC transfer characteristic.

Table 6.1: Design Parameters of circuits in Figs. 4.3.

Parameter	Value
I_B	100μA
$V_{DS}^{sat} = V_{GS} - V_T$	0.5V
$V_{T_{NMOS,PMOS}}$	0.7V, 0.9V
$(w/l)_{NMOS}$	9μm / 1.2μm
$(w/l)_{PMOS}$	26μm / 1.2μm
$V_{dd} - V_{ss}$	3V
C_L	15pF

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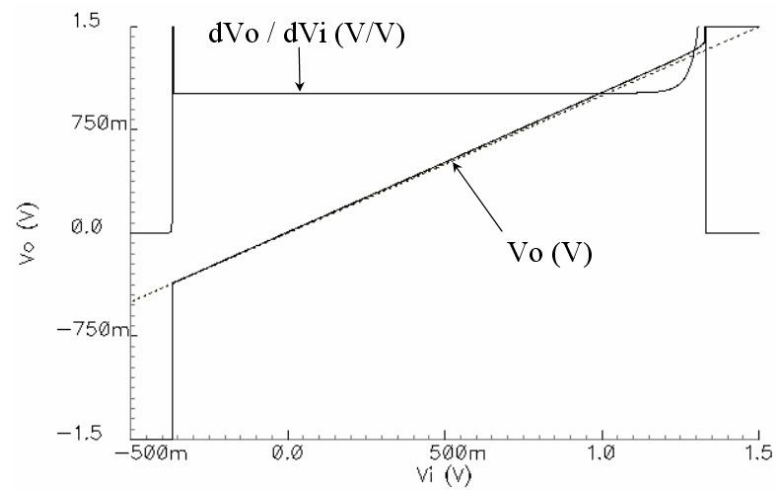
Figure 6.9: DC transfer characteristic of circuit in Fig. 6.7 and its derivative.

Figure 6.10: Experimental results of the DC transfer characteristic of the circuit in Fig. 6.7.
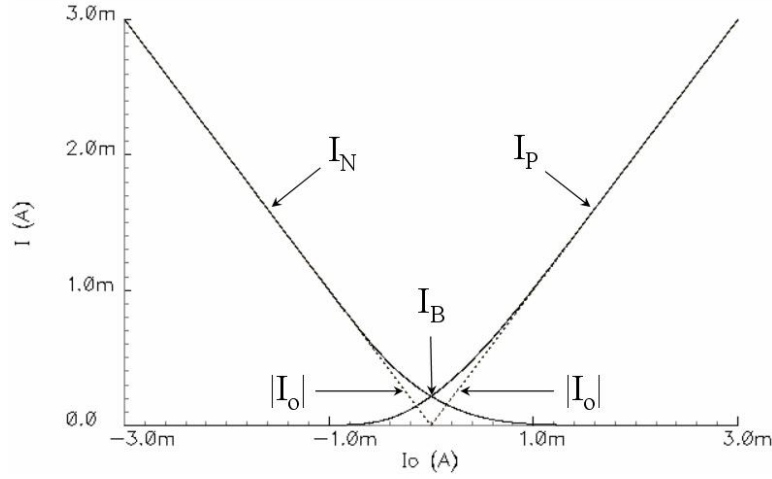
Figure 6.11: DC transfer characteristic of the circuit in Fig. 6.7 and its derivative.

Fig. 6.11 shows the Class AB operation. Currents I_P and I_N are the currents across transistors M1a and M1b, respectively. Fig. 6.12 shows the AC analysis of the circuit. It has an open-loop gain $A_v = 69$dB, a bandwidth of BW $= 6$kHz, a Gain-Bandwidth product of GBW $= 17$MHz and a phase margin of 70deg when dringinc a capacitive load of 15pF. Fig. 6.13 shows the simulation result of a transient analysis. A square signal of 1Vpp at 5MHz was applied at the input. Observe the Class-AB operation as the output node is sourcing and sinking large currents when driving a loading capacitor of $C_L = 15$pF. The measured slew rates are SR+ $= 28.8$V/μsec and SR- $= 23.13$V/μsec. Fig. 6.14 shows the experimental results for the transient characteristic, using the same parameters as in simulation. In this case the measured slew rate is SR+ $= 21.13$V/μsec and SR- $= 20.83$V/μsec. Fig. 6.15 shows the microphotograph of the fabricated circuit.
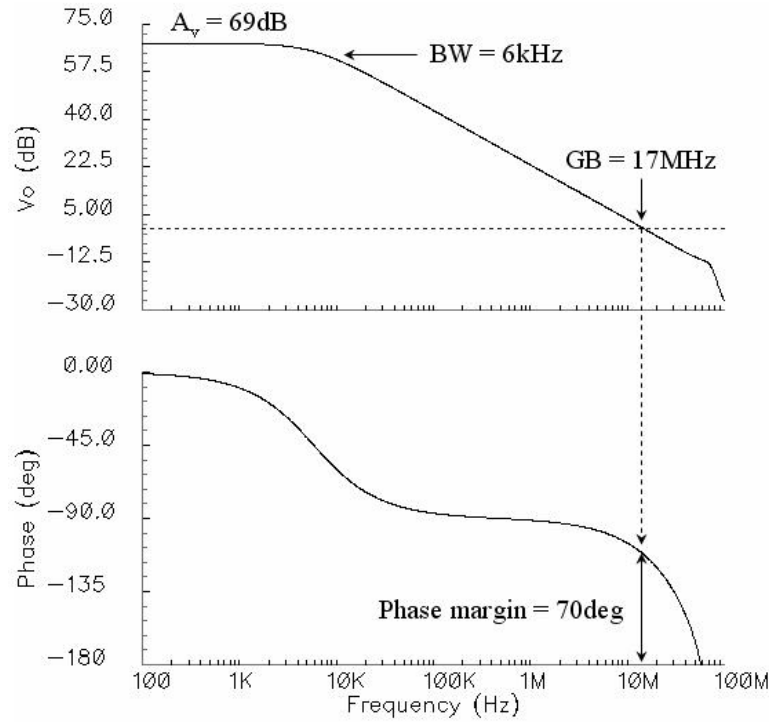
Figure 6.12: Frequency response of the circuit in Fig. 6.7.

Note that in the conventional buffer in Fig. 6.3 as the power supply increases linearly, the bias current in the output stage increases exponentially as shown in Fig. 6.2. This represents a considerable power consumption. Observe, from Fig. 6.8, that in the proposed circuit in Fig. 6.7 the bias current in the output stage remains constat, with a slight variation due to channel length modulation. This enhances the power consumption dramatically, especially for designs where for large power supply voltages.

We now present another approach to maintain the V_{SG} and V_{GS} of the output transistors equal to the desired values so as to provide a biasing current equal to I_B, regardless of the value of the supply voltages. Fig. 6.16 shows

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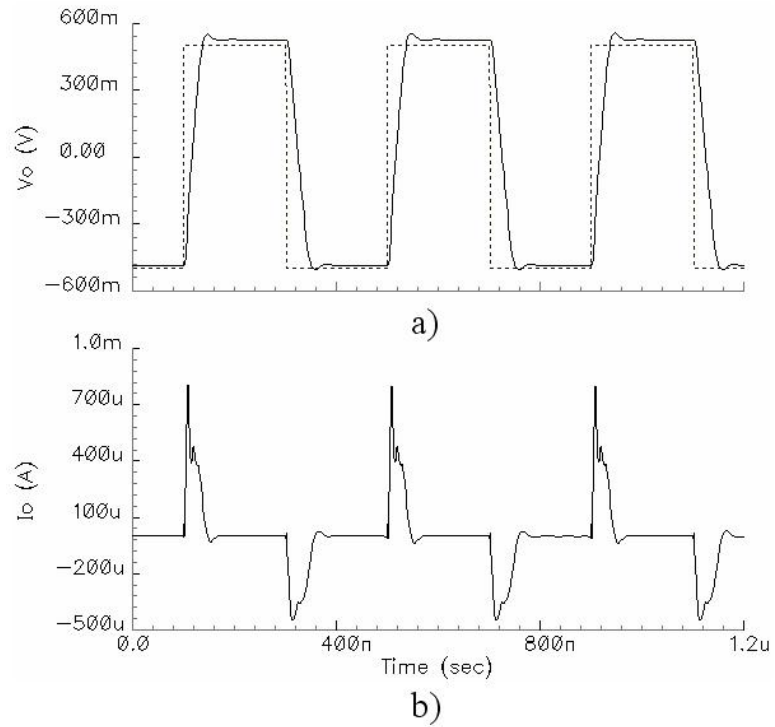
Figure 6.13: Output a) voltage and b) current of the circuit in Fig. 6.7 when performing a transient analysis using a $1V_{pp}$ at 5MHz.
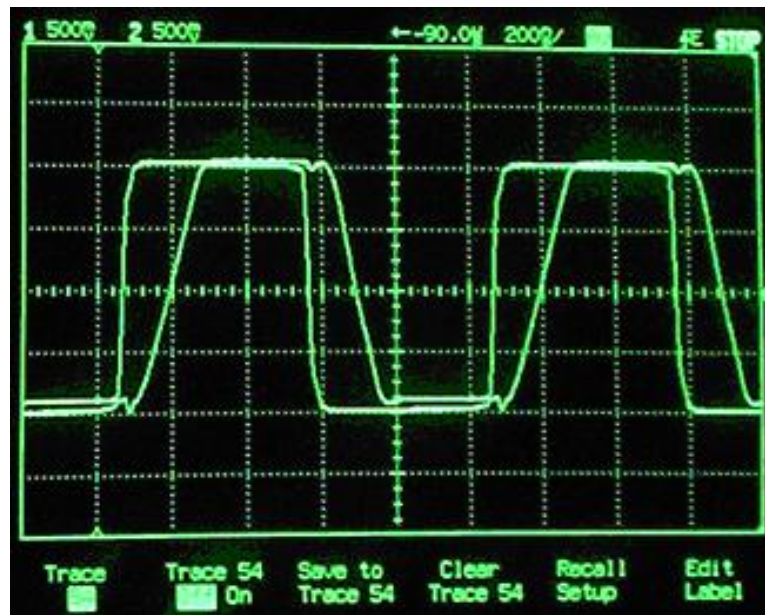
Figure 6.14: Experimental results of the output voltage of the circuit in Fig. 6.7 when performing a transient analysis using a $1V_{pp}$ at 500kHz.
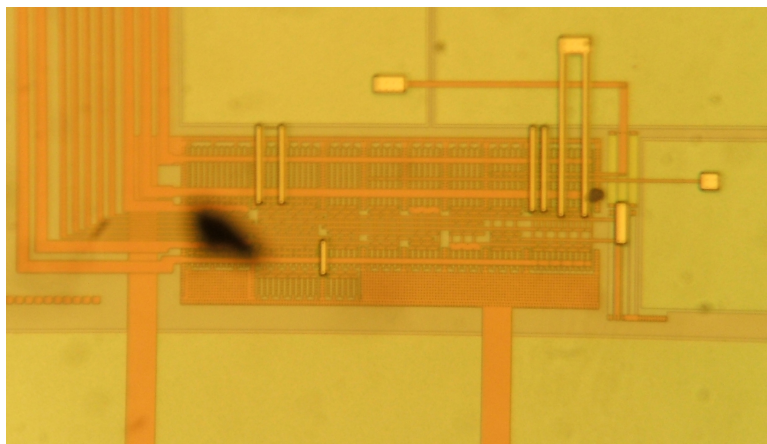
Figure 6.15: Microphotograph of the fabricated circuit in Fig. 6.7, 396μm x 174μm.
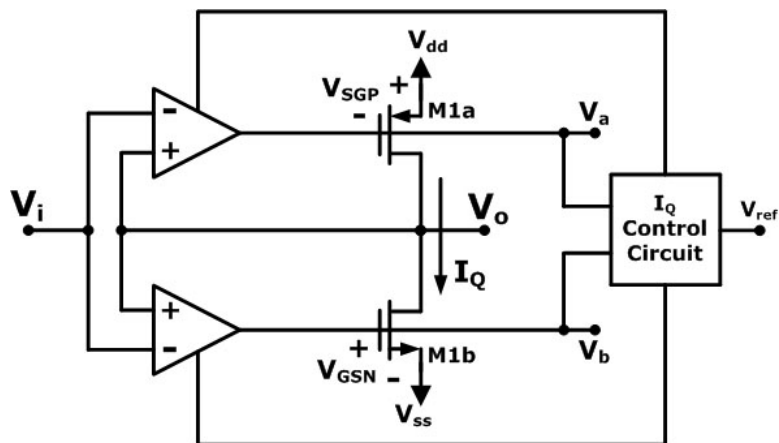
Figure 6.16: Conceptual circuit of the proposed output buffer with I_Q Control Circuit.

the conceptual circuit that illustrates the principle of operation of the proposed circuit. It includes a control circuit that senses the voltages V_a and V_b so as to control the opamps to provide the desired quiescent DC output voltage for V_{SG} and V_{GS} of the output transistors.

Fig. 6.17(a) shows the output buffer with the internal structure of the opamps. Assume the opamps are two-stage amplifiers composed of a PMOS dif-

ferential pair as the first stage and an NMOS transistor in a common-source configuration as the second stage. Fig. 6.17(b) shows a circuit that authors refer to as the common-mode feedback (CMFB) circuit [3]. It is often used in fully-differential operational amplifiers to determine the output common-mode voltage and control it to be equal to a reference voltage. Observe that the voltages at the gate terminal of transistors M2 and M6, are V_a and V_b', which are compared to a reference voltage V_{BP} which is the V_{SG} of a PMOS operating with a bias current I_{Bias}. When these voltages move in a differential manner, the same currents flow through transistors M2 and M5 and the same currents flow through M3 and M6. This causes the PMOS transistors M7 and M8 to have a constant current equal to I_B, maintaining the voltages V_{ctrla} and V_{ctrlb} constant and equal to V_{GS}^Q. Now consider the case where voltages V_a and V_b' move in the same direction. This causes the PMOS transistors M7 and M8 to increase or decrease their currents depending on what direction V_a and V_b' move. This causes a change in the voltages V_{ctrla} and V_{ctrlb} which is used in the proposed circuit to stabilize the quiescent output current.

The voltage V_{BP} is the quiescent voltage V_{SG}^Q of a PMOS transistor to provide the biasing current I_B. Voltages V_{ctrla} and V_{ctrlb} are used to control the source-to-gate voltage of transistors M3a and M3b. Thus, they control the desired voltages V_{SG} and V_{GS} of the output transistors. Voltages V_a and V_b correspond to voltages V_{SG} and V_{GS} from Fig. 6.17(a), respectively. Note that the voltage

Figure 6.17: a) Proposed Class-AB output buffer and b) CMFB as the Control Circuit.

V_b is applied to a common-source transistor of gain -1 to get the same gate-to-source voltage, but referred to a PMOS transistor. This eliminates the necessity of introducing a voltage shift as the minimum requirement of a differential pair is $V_{GS}^Q + V_{DS}^{sat}$. In addition, we can also use the same reference voltage V_{BP} in the CMFB circuit.

To describe the operation of the Control Circuit, let us consider the case where the quiescent current of both of the output transistors M1a and M1b increase, while voltages V_{SG} and V_{GS} also increase. Therefore, V_a and V_b go down in voltage. The CMFB circuit increases the current across M7 (I_{M7}) and increases the current in M8 (I_{M8}). Thus, V_{ctrlb} goes up and V_{ctrla} goes down in voltage. Note that if V_{ctrla} goes down, it causes V_{SG} in Fig. 6.17(a) to go up, decreasing I_{M1a}. Due to negative feedback, the CMFB maintains this voltage approximately equal to the reference voltage V_{BP}. It also maintains the current in M1a approximately equal to I_B. V_{ctrlb} operates similarly.

The DC operation is shown in Fig. 6.18. Observe in Fig. 6.18(a) that the values of V_{SG} and V_{GS} remain constant as the supply voltages increase. This causes the current in the output devices to remain constant as shown in Fig. 6.18(b). The slight increase is due to channel length modulation in the output transistors, which represents a very small variation compared to the case in Fig. 6.1.
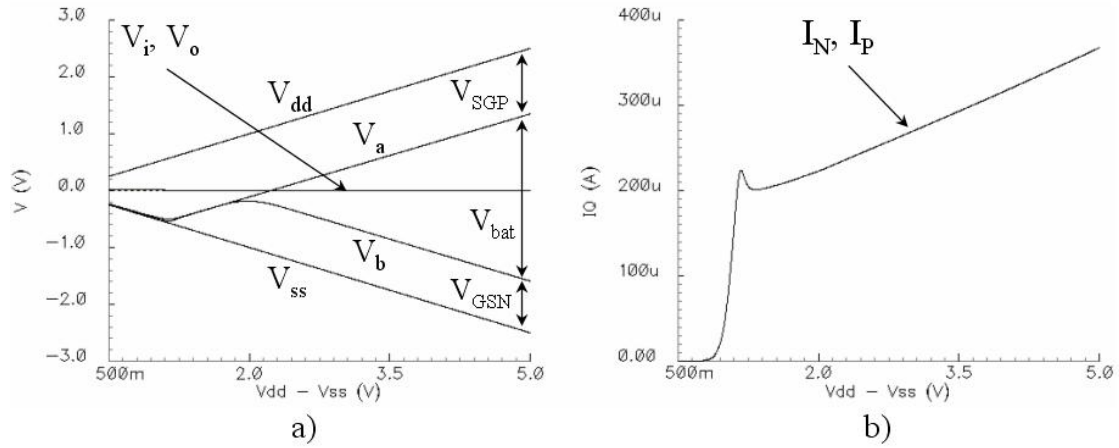
Figure 6.18: DC operation of the circuit in Fig. 6.17 showing a) DC voltages as the voltage rails increase and b) currents in the output transistors.

Simulations were performed using SpectreS in a 0.5μm CMOS technology. The design parameters are as specified in Table 6.1. The total supply voltage is 4V in order to show the wide input-output operational range. The minimum power supply requirement is $V_{GSM2,3} + V_{DSM1}^{sat} + V_{in}^{swing}$, just as in a regular amplifier based on a differential pair as the input stage. The values for the compensating capacitor and resistor C_C and R_C are 30pF and 1.7kΩ, respectively, following the pole-zero equations for a 3-stage amplifier specified

The circuit in Fig. 6.17 was tested as a voltage follower. Fig. 6.19 shows the DC transfer characteristic and its derivative which shows very high linearity. Besides the derivative the Total Harmonic Distortion was calculated to get a more precise measure of the linearity. The proposed structure has, for a sinusoidal input signal of $0.5V_p$, a THD of 0.00832%. Fig. 6.20 shows the experimental results of the circuit in Fig. 6.18.
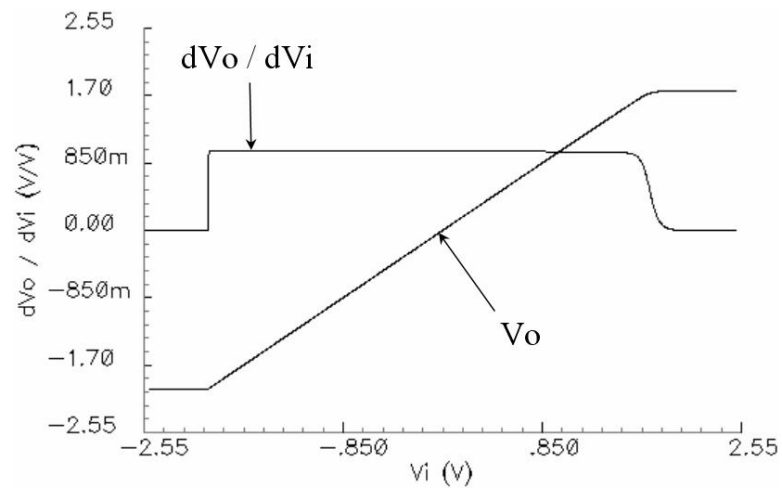
Figure 6.19: DC transfer characterisitc and its derivative of circuit in Fig. 6.17.
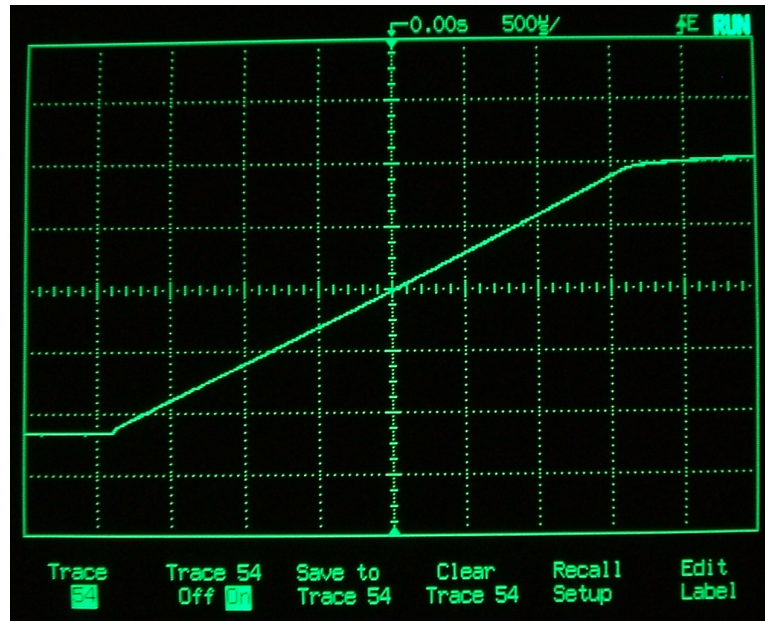
Figure 6.20: Experimental results of the DC operation of the circuit in Fig. 6.17.

Fig. 6.21 illustrates Class-AB operation. I_P and I_N are the currents across transistors M8 and M9, respectively. Observe that the CMFB circuit maintains the currents in M1a and M1b complementary to I_B when the output current is less than I_B. Transistors M1a and M1b are three times the size of the other transistors in order to satisfy the requirements of large currents at the output. Transistors M2a, M2b, M3a and M3b are also three times the size of the other transistors in order to sink and source currents from the large compensation capacitors C_C. Fig. 6.22 shows the AC analysis of the circuit. It has an open-loop gain $A_v = 110$dB, bandwidth BW = 223Hz, Gain Bandwidth product GBW = 68MHz and a phase margin of 52deg when driving a capacitive load of 15pF. Fig. 6.23 shows the simulation result of a transient analysis. A square signal of $1V_{pp}$ at 5MHz was applied at the input. Observe the Class-AB operation of sourcing and sinking large currents at the output node when applied to a load capacitor $C_L = 15$pF. The measured slew rates are SR+ = 0.201V/usec and SR- = 0.163V/usec. Fig. 6.24 shows the experimental results of the transient analysis for the same parameters as for simulation. In this case the measured slew rate is SR+ = 35.73V/μsec and SR- = 43.87V/μsec. Fig. 6.25 shows the microphotograph of the fabricated circuit.

As mentioned before, in the conventional buffer in Fig. 6.3, as the power supply increases linearly, the bias current in the output stage increases exponentially as shown in Fig. 6.2. This represents a considerable power consumption.
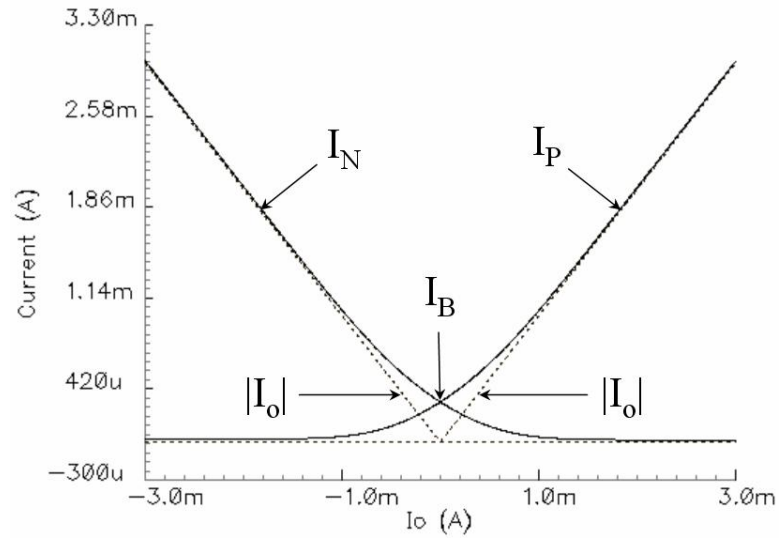
Figure 6.21: Currents in the output stage showing the Class AB operation of circuit in Fig. 6.17.
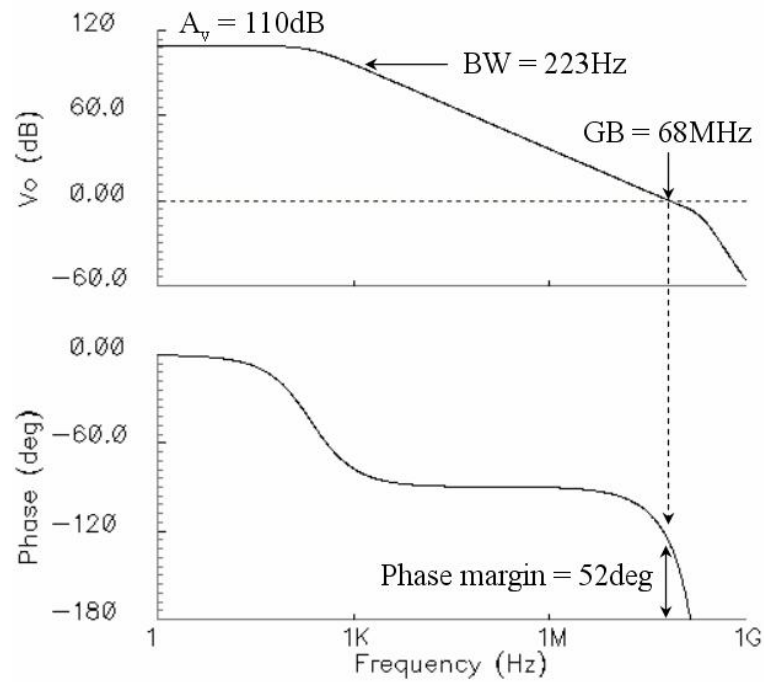
Figure 6.22: Frequency response of the circuit in Fig. 6.17.

a)

b)
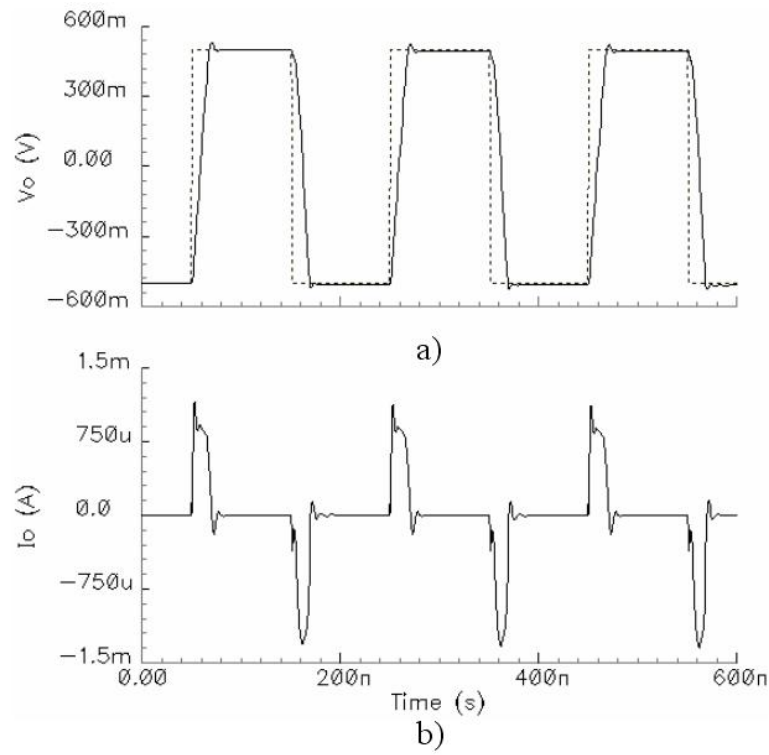
Figure 6.23: a) Output voltage and b) output current of the circuit in Fig. 6.17 when performing a transient analysis using a $1V_{pp}$ at 5MHz.
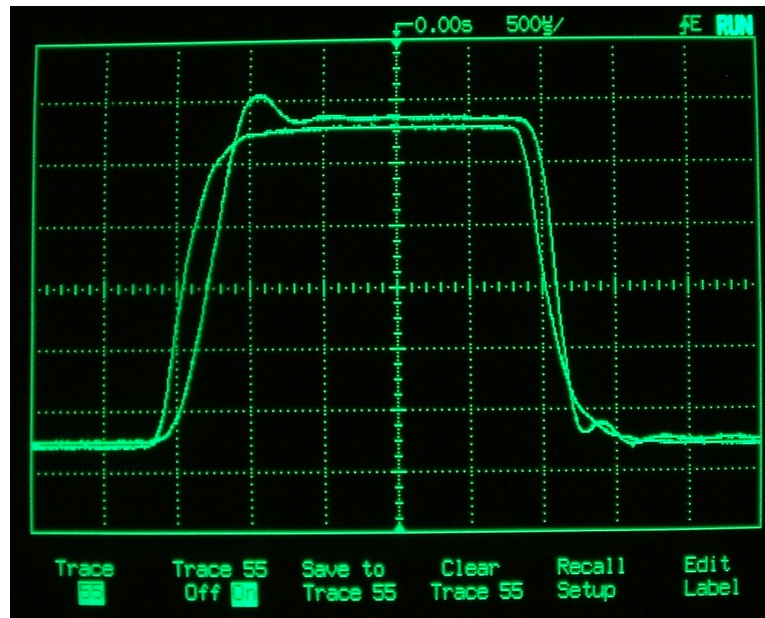
Figure 6.24: Experimental results of the output voltage of the circuit in Fig. 6.17 when performing a transient analysis using a $1V_{pp}$ at 500kHz.
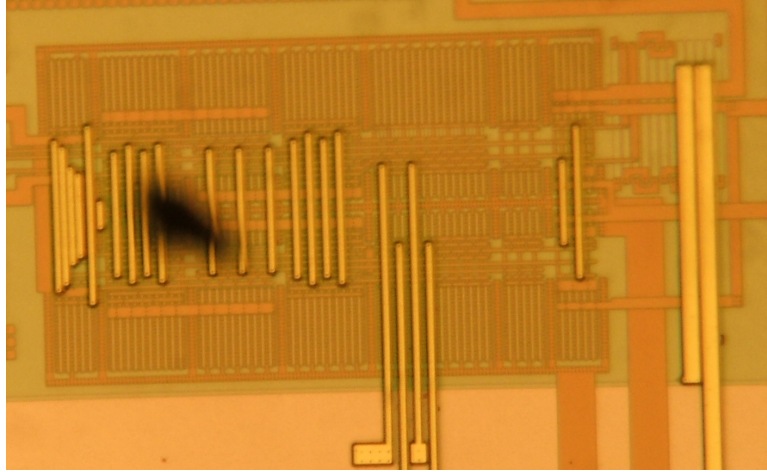
Figure 6.25: Microphotograph of the fabricated circuit in Fig. 6.17, 230μm x 138μm.

Observe, from Fig. 6.18, that in the proposed circuit in Fig. 6.17 the bias current in the output stage remains constat, with a slight variation due to channel length modulation. This enhances the power consumption dramatically, especially for designs where for large power supply voltages.

Previous chapters have shown the implementation of the technique described in Chapter 3 to achieve a well controlled bias current in the output stage under static conditions. However, it is desirable to implement these amplifiers in a functional system so as to observe improved performance.

As mentioned in the beginning of this document, Class AB amplifiers are commonly used in applications that isolate a low-power signal from a load that might distort it, such as a low-resistive or high-capacitive load.

R-2R Digital-to-Analog Converter

The first system used to observe the functionality of the amplifiers is a 4-bit R-2R Digital-to-Analog Converter [3] with sign control bit for positive and negative reference voltages, shown in Fig. 7.1. This converter presents a resistive load to be driven by the output amplifiers. In this design the conventional opamps set the voltage R_{ref+} and V_{ref-} to the corresponding resistor. This sets the currents through the resistors to $I_{B-} = (V_{dd} - V_{ref-})/R$ and $I_{B+} = (V_{ref+} - V_{ss})/R$. Consequently, this current is copied to the rest of the branches, which sense a binary weighted current. This current is loaded either from Gnd or from the amplifier under test through the switches. The transistors used as switches have a size of $(w/l)_{PMOS} = 26\mu/1.2\mu m$ and $(w/l)_{NMOS} = 9\mu/1.2\mu m$, the resistor has a value
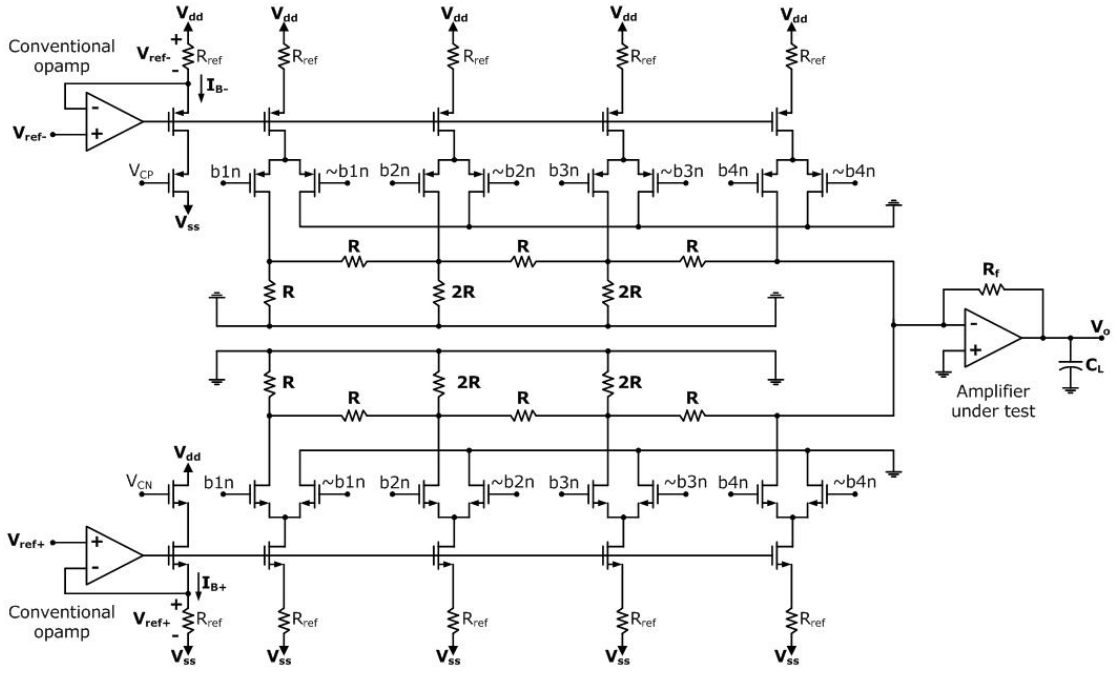
Figure 7.1: R-2R Digital-to-Analog Converter.

of R = 1kΩ, the supply voltage is $V_{dd} - V_{ss} = 5$V, $I_B = 100\mu$A, a capacitive load $C_L = 30$pF and the opamps are conventional two-stage amplifiers.

For this system the transfer function is given by:

$$V_{out} = \frac{-R_o \cdot V_{ref}}{2R} \cdot \left[\frac{b_0}{2^0} + \frac{b_1}{2^1} + ... + \frac{b_n}{2^n} \right] \tag{7.1}$$

Figs. 7.2(a) and (b) show the operation of the common two-stage amplifier in Fig. 4.1 and the Class AB opamp with floating current sources in Fig. 2.31 respectively. Fig. 7.3(a) and (b) show the operation of the 2-stage and 3-stage amplifiers in Figs. 4.3 and 4.11, respectively. Fig. 7.4(a) and (b) show the operation of the amplifier in Fig. 5.13 using the floating batteries in Figs. 5.3 and 5.5, respectively. Fig. 7.5(a) and (b) show the operation of the buffers in Figs. 6.7 and 6.17, respectively.

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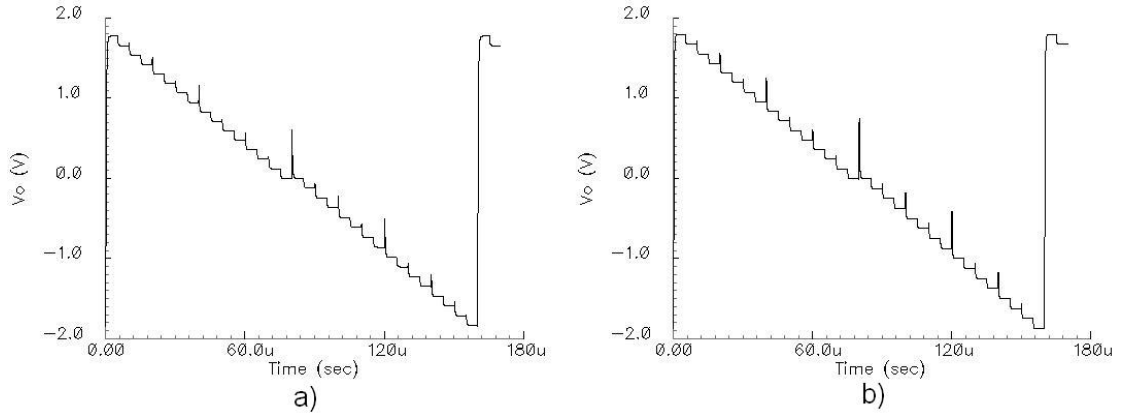
Figure 7.2: R-2R Digital-to-Analog Converter using a) the common 2-stage opamp in Fig. 4.1 and b) the Class AB opamp with floating current sources in Fig. 2.31.
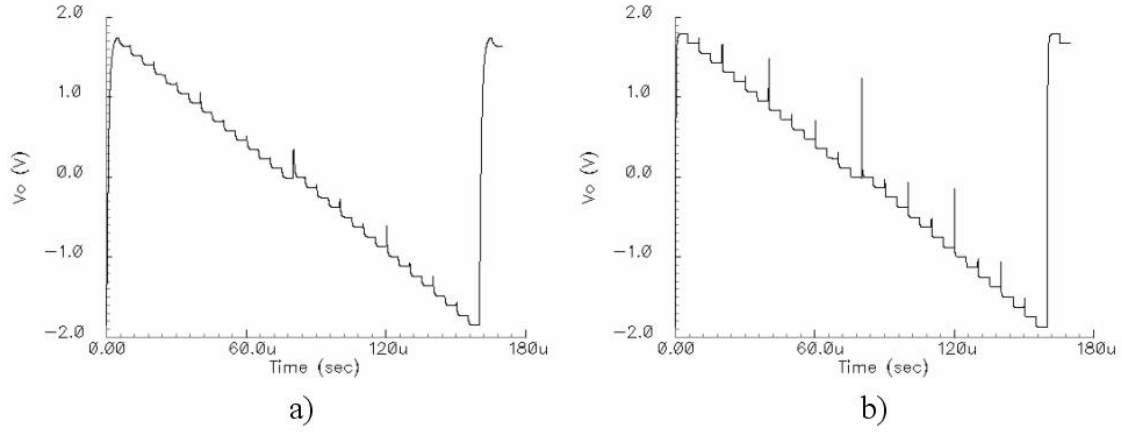
Figure 7.3: R-2R Digital-to-Analog Converter using the opamps a) in Fig. 4.3 and b) in Fig. 4.11.

Observe that all the amplifiers were operational when tested in the Digital-to-Analog Converter. Some of them switch from the previous state to the next faster that others, although it is difficult to visualize this as every step is considerably small. Therefore, the switching time is analyzed as the slew rate. A comparison of the slew rate between the amplifiers is studied later in this chapter.

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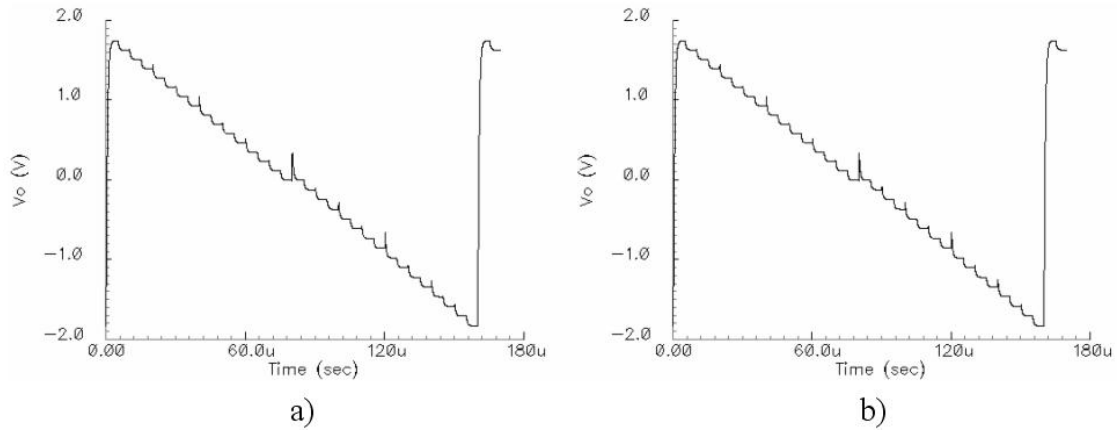
Figure 7.4: R-2R Digital-to-Analog Converter with an opamp using the floating batteries a) in Fig. 5.3. and b) in Fig. 5.5
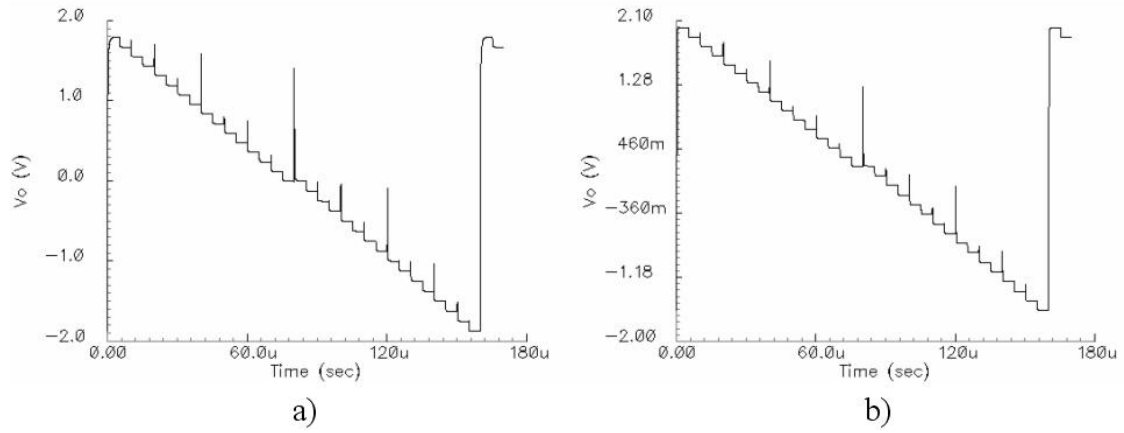
Figure 7.5: R-2R Digital-to-Analog Converter using buffers a) in Fig. 6.7 and b) in Fig. 6.17.

Charge Redistribution Digital-to-Analog Converter

The second system we used to observe the functionality of the amplifiers is a charge-redistribution Digital-to-Analog Converter [3], as shown in Fig. 7.6, which presents a capacitive load to be driven by the output amplifiers. In this design the size of the transistors used as switches are the same as in the previous
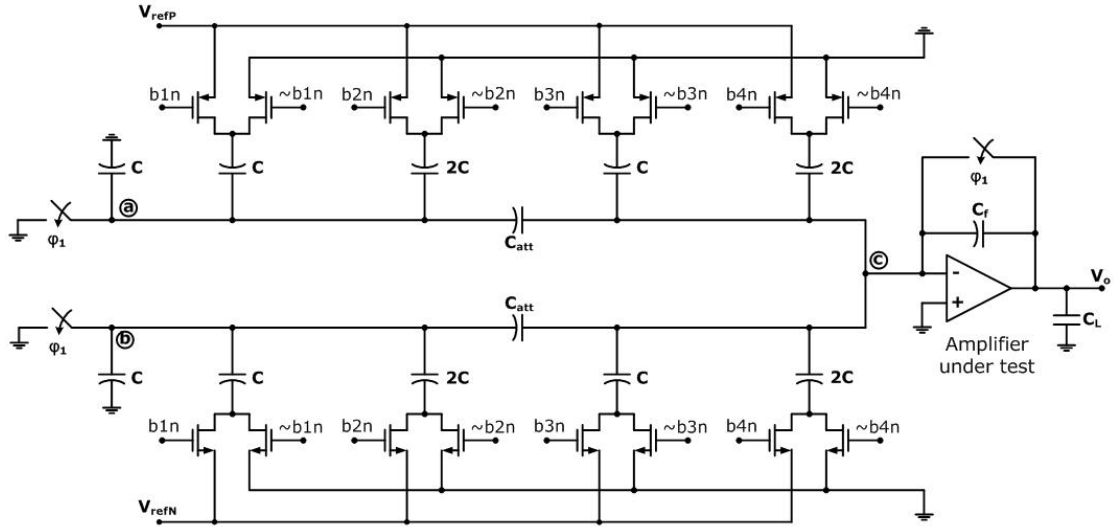
Figure 7.6: Charge redistribution Digital-to-Analog Converter.

case. Also, it has a capacitance C = 1pF, a load capacitance C_L = 30pF and the supply voltage is $V_{dd} - V_{ss}$ = 5V. Observe there are switches from nodes a, b and c, to short them to Gnd before the converter is operated. This is to eliminate any charge trapped as these are floating nodes due to the capacitors.

For this system the transfer function is given by:

$$V_{out} = V_{ref} \left[\frac{b_0}{2^0} + \frac{b_1}{2^1} + ... + \frac{b_n}{2^n} \right] \tag{7.2}$$

Fig. 7.7(a) and (b) show the operation of the common two-stage amplifier in Figs. 4.1 and 2.31 respectively. Figs. 7.8(a) and (b) show the operation of the 2-stage and 3-stage amplifiers in Figs. 4.3 and 4.11, respectively. Fig. 7.9(a) and (b) show the operation of the amplifier in Fig. 5.13 using the floating batteries in Figs. 5.3 and 5.5, respectively. Fig. 7.10(a) and (b) show the operation of the buffers in Figs. 6.7 and 6.17, respectively.
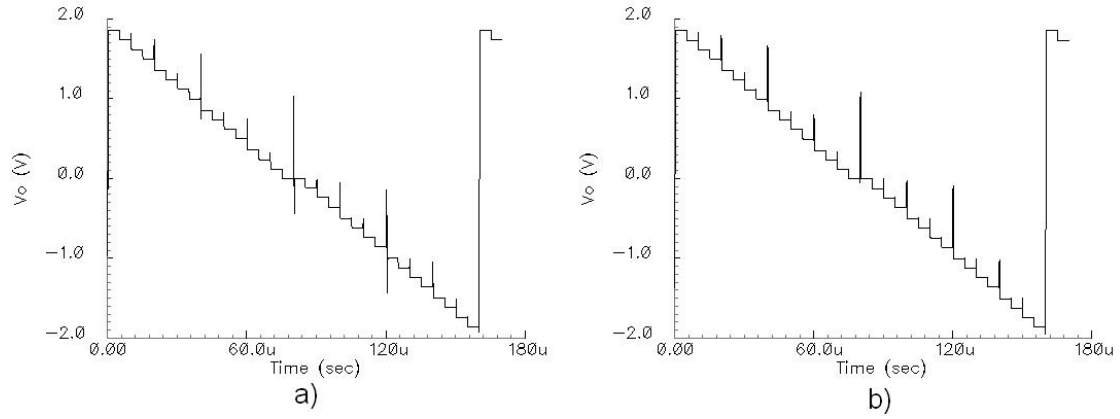
Figure 7.7: Charge redistribution Digital-to-Analog Converter using a) the common 2-stage opamp in Fig. 4.1 and b) the Class AB opamp with floating current sources in Fig. 2.31.
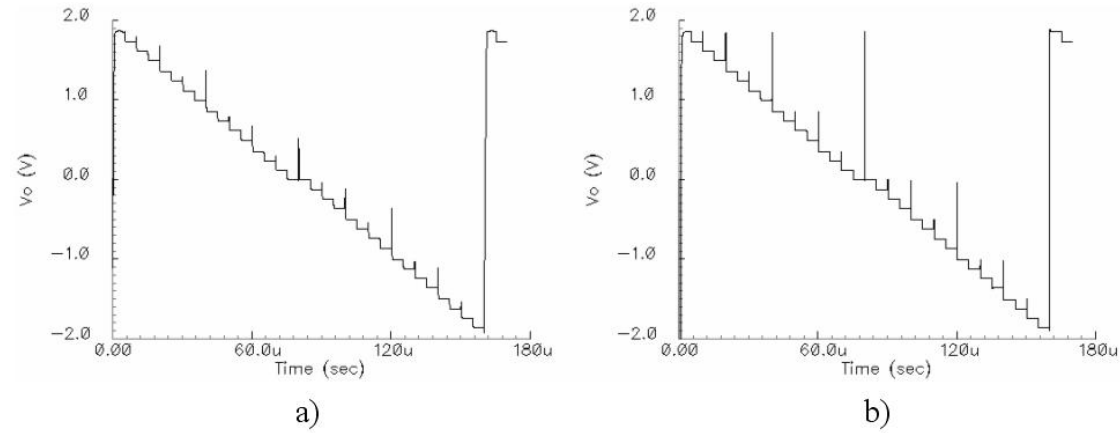
Figure 7.8: Charge redistribution Digital-to-Analog Converter using the opamps a) in Fig. 4.3 and b) in Fig. 4.11.

Again, observe that all the amplifiers were operational when tested in the charge redistribution Digital-to-Analog Converter. Some of them switch from the previous state to the next faster than others, although it is difficult to visualize this as every step is considerably small. Therefore, the switching time is analyzed as the slew rate. A comparison of the slew rate between the amplifiers is studied next.
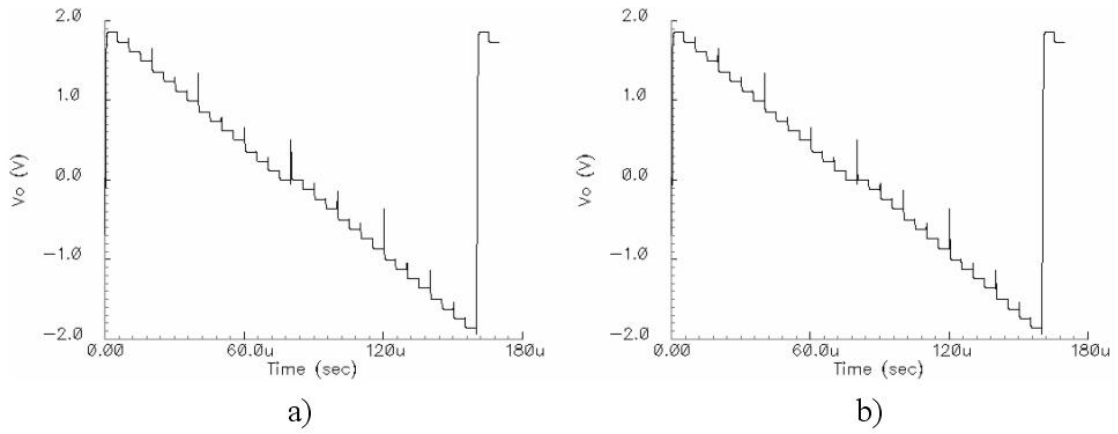
Figure 7.9: Charge redistribution Digital-to-Analog Converter with an opamp using the floating batteries a) in Fig. 5.3. and b) in Fig. 5.5.
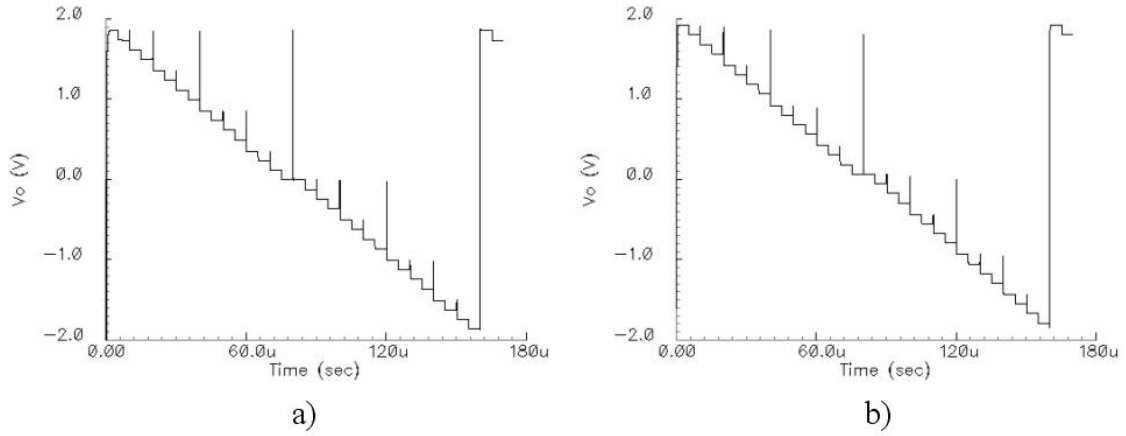
Figure 7.10: Charge redistribution Digital-to-Analog Converter using buffers a) in Fig. 6.7 and b) in Fig. 6.17.

Slew Rate

When an amplifier is used in a system such as a D/A converter, the response time of the amplifier for a given load becomes critical for the overall performance of the entire system. To determine the speed of each amplifier to settle the output to a given voltage, the slew rate and settling time were evaluated. Fig. 7.11 shows

Figure 7.11: Slew rate of amplifier in a) Fig. 4.1, b) Fig. 2.31, c) Fig. 4.3, d) Fig. 4.11, e) Fig. 5.3, f) Fig. 5.5, g) Fig. 6.7 and h) Fig. 6.17 with an input signal of 500MHz. A DC voltage offset was added intentionally.

a comparison of the results obtained for the slew rate of each of the amplifiers when a square wave of $1V_{pp}$ at 500KHz was used. An intentional DC voltage offset was added for visualization purposes. Table 7.1 shows a detailed comparison of the measured values. As mentioned before, a capacitor $C_L = 30pF$ was used as a load. In this case the load capacitance is two times the load used to test the amplifiers separately in previous chapters. This is to test the capability of the amplifiers to provide the desired voltage when driving a larger load. An input signal of 5MHz was used for the LSB bit.

Table 7.1: Comparison of the Slew Rate of the amplifiers.

	Amplifier	SR+ (V/μsec)	SR- (V/μsec)
a)	Common 2-stage opamp	10.21	4.71
b)	Class AB w/floating I's in Fig. 2.31	10.65	8.1
c)	2-stage Class AB opamp in Fig. 4.3	4.01	5.83
d)	3-stage Class AB opamp in Fig. 4.11	23.06	21.7
e)	Opamp using dual battery in Fig. 5.3	4.77	4.73
f)	Opamp using dual battery in Fig. 5.5	4.79	4.73
g)	Class AB output buffer in Fig. 6.7	28.8	23.13
h)	Class AB output buffer in Fig. 6.17	42.12	48.5

Table 7.2: Comparison of the settling time of the amplifiers.

	Amplifier	t_{set} (+) ($n$sec)	t_{set} (-) ($n$sec)
a)	Common 2-stage opamp	170.7	478
b)	Class AB w/floating I's in Fig. 2.31	188.4	193.8
c)	2-stage Class AB opamp in Fig. 4.3	474.4	275
d)	3-stage Class AB opamp in Fig. 4.11	260.9	275
e)	Opamp using dual battery in Fig. 5.3	272	294
f)	Opamp using dual battery in Fig. 5.5	278.4	288
g)	Class AB output buffer in Fig. 6.7	26.6	104
h)	Class AB output buffer in Fig. 6.17	96.2	105

From the results above we see that the fastest amplifiers are the ones with three gain stages, that is, the circuits in Figs. 6.17 and 4.11, shown in Figs. 7.11(a) and (b), respectively. It can be seen that these two amplifiers have a considerable enhancement of the slew rate compared to the rest of the amplifiers. This represents an enhancement over the conventional amplifier from Fig. 4.1 of around 5 for the amplifier in Fig. 6.17 and 2 for the amplifier in Fig. 4.11. The amplifier in Fig. 6.7 is the next fastest circuit with an enhancement of around 3 over the conventional amplifier. The amplifier that uses the batteries in Figs. 5.3 and 5.5 have a lower speed but they have a symmetrical rising and falling slew

rates of around 4.7V/μsec. We expect the same behavior from the amplifier in Fig. 6.7. Fig. 7.11(d) shows the operation of the conventional amplifier from Fig. 4.1, with a slew rate of SR+ = 10.2V/μsec and SR- = 4.7V/μsec. Note from Fig. 7.11 that the raising of the conventional amplifier is even faster than some of the proposed amplifiers, although the falling shows a considerable limitation, whereas the proposed schemes show an improved falling. This can also be verified in Table 7.2, which shows the settling time of the amplifiers. Here one can see that the falling settling time of the conventional amplifier, t_{s-} is very poor.

Headphone speaker

It is also desirable to obtain a very low output impedance from the amplifier when connected in a feedback configuration in order to avoid deviations of the output voltage with respect to the input when driving a very low resistive load.

Therefore, the third method we used to observe the functionality of the amplifiers is driving a headphone speaker, simulated as a resistive load $R_L = 32\Omega$, as shown in Fig. 7.12 [38]. Fig. 7.13 shows the response of each of the amplifiers. A square wave input signal of $1V_{pp}$ at 50KHz was used. An intentional time delay was added for visualization purposes.

In each case the output impedance of the amplifiers is given by the expression:

$$Z_o = \frac{\partial V_o}{\partial I_O} \qquad (7.3)$$

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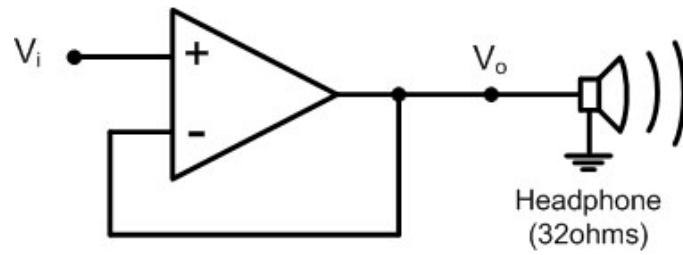
Figure 7.12: Amplifier driving a resistive load.

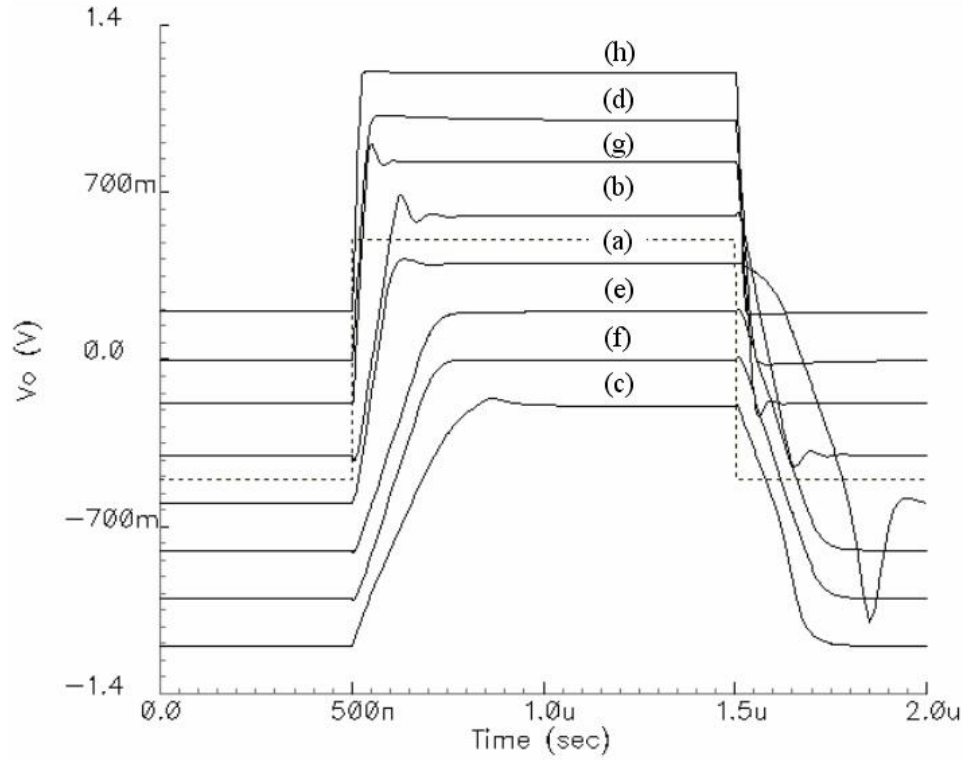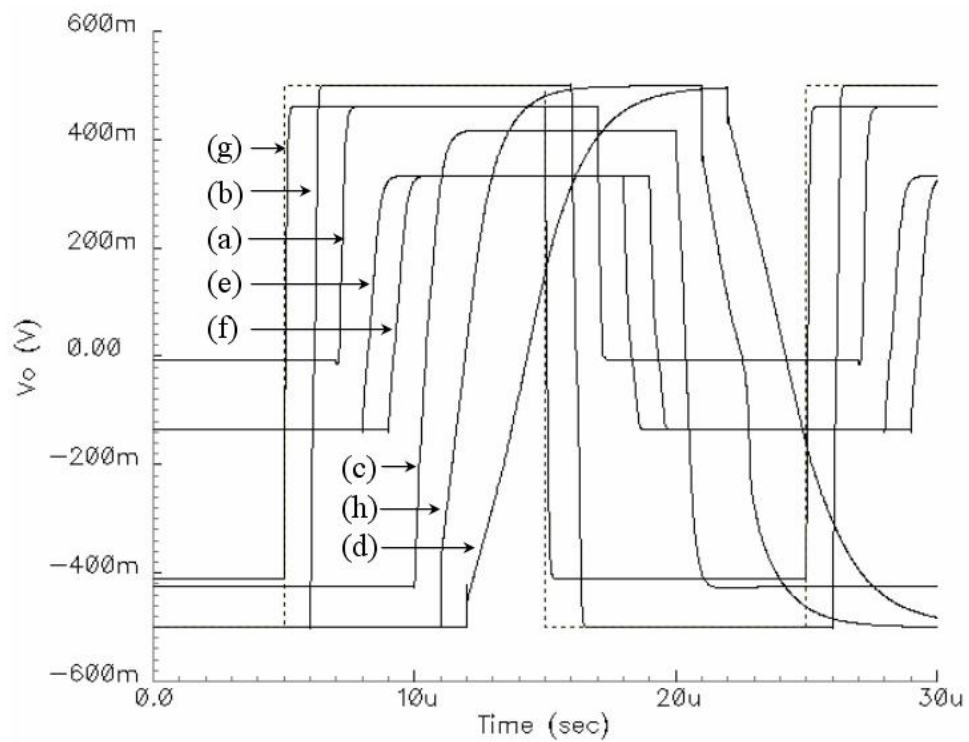Figure 7.13: Response to resistive load of amplifier in a) Fig. 4.1, b) Fig. 2.31, c) Fig. 4.3, d) Fig. 4.11, e) Fig. 5.3, f) Fig. 5.5, g) Fig. 6.7 and h) Fig. 6.17. A time delay was added intentionally.

which is the ratio between the deviation of the output voltage δVo and the current being sourced or sank at the output node. Table 7.1 shows a comparison of the output impedance of the amplifiers.

Table 7.3: Comparison of the output impedance of the amplifiers.

	Amplifier	Z_o (+) (V/A)	Z_o (-) (V/A)
a)	Common 2-stage opamp	2.76	2118.54
b)	Class AB w/floating I's in Fig. 2.31	0.12	0.15
c)	2-stage Class AB opamp in Fig. 4.3	6.31	5.55
d)	3-stage Class AB opamp in Fig. 4.11	0.11	0.12
e)	Opamp using dual battery in Fig. 5.3	15.96	86.43
f)	Opamp using dual battery in Fig. 5.5	16.04	86.34
g)	Class AB output buffer in Fig. 6.7	2.76	6.92
h)	Class AB output buffer in Fig. 6.17	0.064	0.012

From the results above we analyzed by what ratio the output of each amplifier deviates from the ideal value. This property is strongly related with the gain of the amplifier. Observe from Fig. 7.12 that the amplifier is connected as voltage follower, where the output is connected to the inverting input. The capability of the amplifier to maintain the voltage between the two inputs close to each other, when a large current is being delivered at the output node, depends on the open-loop gain of the amplifier. This defines the output impedance of the amplifier. The lower the impedance the amplifier offers at the output node, the more accurate the amplifier follows the ideal value. Observe that Figs. 7.13(f) and (g) are the three-stage amplifiers in Figs. 6.17 and 4.11, respectively, and are capable to follow the ideal value better than any other design for positive and negative values, with a deviation δV of around 0.001V. They are followed by Figs.

7.13(a) and (e), which are the amplifiers in Figs. 6.17 and 4.3, respectively. They have a δV of around 0.06V. Finally, Figs. 7.13(c) and (d) are the plots of an amplifier when the batteries in Figs. 5.3 and 5.5 are used. They have a deviation of $\delta V = 0.1666V$. Note that the plot of the conventional amplifier, shown in Fig. 7.13(b) approaches to ideal voltage more than some of the proposed designs for a positive input. Although, for negative input it reaches a value of 0.0074V, which gives a $\delta V = 0.5926$. In practice, this value is very high, and shows a very poor output impedance for negative values, whereas the proposed schemes show a considerable enhancement. The best case -the amplifier in Fig. 6.17- enhances this value by a factor of 165,000 and the worst case -the amplifiers in Figs. 5.3 and 5.5- enhances this value in a factor 24.5.

Table 7.4 shows a comparison of the parameters used in the design of all the amplifiers such as number of transistors, silicon area, power dissipation, minimum power supply requirements and information from the frequency response analysis.

Mismatched parameters

Again, observe that the implementation of the proposed control circuit explained in Chapter 3 on all the amplifiers described in previous chapters is based on the copy of part of the circuit. Then the conditions of the replicated circuit are transferred to the operational part. Therefore, it is desired to have equal

Table 7.4: Comparison of the parameters of the amplifiers, where a) conventional opamp in Fig. 4.1, b) Class AB opamp using floating current sources in Fig. 2.31, c) 2-stage opamp in Fig. 4.3 and d) 3-stage opamp in Fig. 4.11, e) battery in Fig. 5.3, f) battery in Fig. 5.5, g) Class AB buffer in Fig. 6.7 and h) Class AB buffer in Fig. 6.17.

Amp	# M's	area (μm x μm)	Current (xI_B)	Minimum $V_{dd} - V_{ss}$	A_v (dB)	GB (Hz)	Phase margin ($°$)
a)	10	98x86	4	2.5	70	5	70
b)	34	205x138	12	2.5	104	10	45
c)	38	230x138	15	2.5	110	68	52
d)	88	396x174	20	2.5	69	17	70
e)	34	120x133	$2I_B+5I_R$	1	70	5	70
f)	34	120x133	$2I_B+5I_R$	1	70	5	70
g)	21	220x90	9	2.5	68	5	76
h)	27	280x90	12	2.5	102	45	55

conditions between the replica and the operational circuits. Thus, the parameters between these two parts must be as similar as possible.

Although, it is not possible to have the exact parameters as the fabrication process introduces a certain percentage of mismatch between the devices. For this constrain several techniques are utilized in the process of developing the layout of the circuit, such as common centroid and interdigitation. These techniques minimize the mismatch introduced by the fabrication process, but still it typically introduces an error of 2% between devices. Therefore, it is of interest to determine the effect of this mismatch in the bias current in the output stage. Table 7.5 shows the most sensitive devices in each of the amplifiers discussed in previous chapters and the ratio the bias current is increased by when a mismatch of 2% is introduced to these devices.

Table 7.5: Comparison of the bias current in the output stage when a mismatch of 2% is introduced in the most critical transistor.

	Amplifier	Mismatched Transistor	Ratio I_{outstg}^{Q} increases
a)	Common 2-stage opamp	M7	1.021
b)	Class AB w/floating I's in Fig. 2.31	Mp8,9, Mn8,9	1.007
c)	2-stage Class AB opamp in Fig. 4.3	M5c	3.322
d)	3-stage Class AB opamp in Fig. 4.11	M5c	10.015
e)	Opamp using dual battery in Fig. 5.3	MN+,-	1.328
f)	Opamp using dual battery in Fig. 5.5	MN+,-	1.337
g)	Class AB output buffer in Fig. 6.7	M2b, M3b	1.093
h)	Class AB output buffer in Fig. 6.17	M3a,b	1.036

8 CONCLUSIONS

In this dissertation, the implementation of the biasing technique described in Chapter 3 on various Class AB amplifiers has been presented. This technique consists in making a replica of part of the circuit, and having it operate under the desired bias conditions to obtain the proper state for the output devices in the operational part.

In addition, the application of the amplifiers used to implement this technique in different analog systems has been discussed. These systems include those which represent a low-resistive or high-capacitive load. For this purpose we used an R-2R Digital-to-Analog Converter, a charge redistribution Digital-to-Analog Converter and a headphone speaker.

Simulation and experimental demonstrations are given for the circuits using fabricated prototypes. The enhancements achieved by the proposed circuits yield the following characteristics:

a) An efficient implementation of a two-stage amplifier based on a quiescent-condition control circuit to provide Class AB operation at very high frequencies was presented in Chapter 4. Also, the implementation of a three-stage amplifier using the same control circuit was discussed. It was demonstrated with simulation results that the proposed structures can source and sink large currents at the output stage. The proposed circuits show a considerable improvement compared

to the conventional two-stage Class-A opamp. They enhance the slew rate by a factor 5 and the output impedance in a factor 16,500.

b) A compact and efficient implementation of a battery with dual polarity for the implementation of Class AB output stages based on the combination of positive and negative batteries was described in Chapter 5. It was demonstrated with simulation results that the proposed battery can adopt positive and negative polarities and it can operate with a supply voltage as low as the threshold voltage of one transistor. This implementation enhances the performance of the slew rate of the amplifier in a factor 1.2 and the output impedance in a factor of 25.

c) Two efficient implementations of a Class AB buffer based on a comparison between the current in the output stage against the bias current was presented in Chapter 6. It was demonstrated with simulation results that the proposed technique controls the quiescent current of the devices in the output stage, making them complementary to the biasing current I_B for $|I_o| < I_B$ regardless of the value of the supply voltages. Note that we have not lost the capability of providing a large sourcing or sinking current for driving large capacitive or low resistive loads at the output. It was also proven that for one of the cases the buffer operates with very high open-loop gain and at a very high unity-gain frequency, offering very high positive and negative slew rates compared to the conventional two-stage opamp. They enhance the performance of the slew rate in a factor of 5 compared to the conventional amplifier, and the output impedance in a factor of 165,000.

Future work includes the implementation of the control circuit in other Class AB topologies to verify the capability of the proposed design to be implemented. As well as the design of 3-gain-stage amplifiers with reduced size of compensating capacitor.

APPENDIX

APPENDIX A.

The amplification stage is very important in analog design to enhance weak signals for post processing. In this section we describe some of the amplifying configurations that can be achieved with the transistor, which can be characterized according to the input terminal, output terminal and common terminal (signal ground).

Common Source

Figure A.1 shows the diagram of the Common Source $[1, 2, 3]$. Observe that the Gate is used as the input terminal, the Drain as the output terminal and the Source is connected to V_{ss} which behaves as the common terminal (signal ground).

Figure A.1: Common Source configuration.

Figure A.2: Small signal model of the Common Source.

Figure A.2 shows the small signal model; here the output impedance and the gain are given by the expressions:

$$R_{out} = R_D || r_o \tag{A.1}$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{iR_{out}}{v_{in}} = \frac{-g_m v_{gs}(R_D || r_o)}{v_{gs}} = -g_m(R_D || r_o) \tag{A.2}$$

Intuitively, we can deduct that the gain of the Common Source is given by the impedance in the Drain terminal divided by the impedance in the Source terminal (in many cases this configuration is used connecting this terminal to a signal ground, so the only impedance is the $1/g_m$ of transistor M1).

Common Drain

Figure A.3 shows the diagram of the Common Drain configuration [1,2,3]. Observe that the Gate is used as the input terminal, the Source is the output terminal and the Drain is connected to V_{dd} which behaves as the common terminal (signal ground).
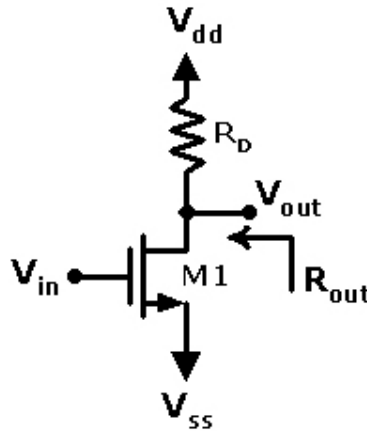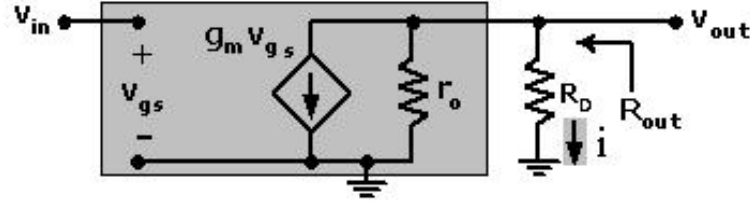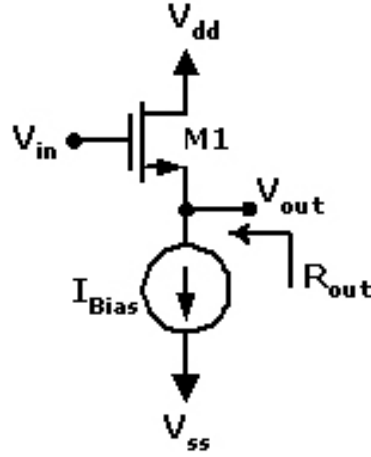
Figure A.3: Common Drain configuration.
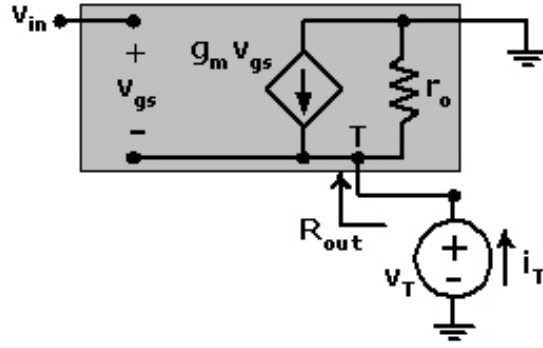
Figure A.4: Small signal model of the Common Drain.

Figure A.4 shows the small signal model; the output impedance is given by the expression:

$$R_{out} = \frac{v_y}{i_y} = \frac{1}{\left(g_m + \frac{1}{r_o}\right)} = \frac{1}{g_m}||r_o \cong \frac{1}{g_m} \tag{A.3}$$

And we know that

$$i_T = -g_m v_{gs} + \left(\frac{v_y}{r_o}\right)$$

$$= +g_m v_y + \left(\frac{v_y}{r_o}\right) \tag{A.4}$$

$$v_o = g_m v_{gs} r_o \tag{A.5}$$

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$$v_i \quad = \quad \frac{v_o}{g_m r_o} + v_o \qquad\qquad (A.6)$$

Therefore, the gain is given by the expression:

$$\begin{aligned} A_v \quad &= \quad \frac{v_o}{v_i} \\ &= \quad \frac{1}{1 + \left(\frac{1}{g_m r_o}\right)} \qquad\qquad (A.7) \end{aligned}$$

Notice that the voltage at the output terminal is approximately the voltage at the input. For this reason, this configuration is also known as the "Voltage Follower" or "Source Follower," and is used to drive weak signals that might be attenuated when being processed.

Cascode Amplifier

Consider the current-voltage equation when a MOSFET operates in saturation. According to the square law, the designer selects the size of the transistor and, by the choice of V_{GS}, manipulates the current (the rest of the parameters are constants given by the technology). Unfortunately, there is another term that is not always considered for practical purposes. This term is described in the expression:

$$I_o = \frac{1}{2}\mu C_{ox} \left(V_{GS} - V_T\right)^2 \left(1 + \lambda \cdot V_{DS}\right) \qquad\qquad (A.8)$$

It shows the effect known as Channel Length Modulation (lambda). This equation describes that the current is not controlled by the length of the transistor, but by
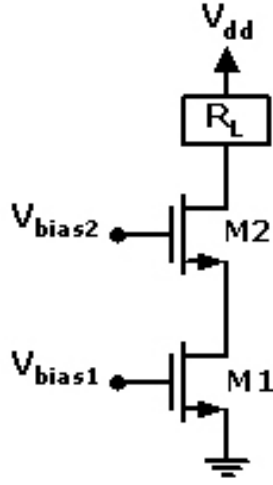
Figure A.5: Cascode amplifier.
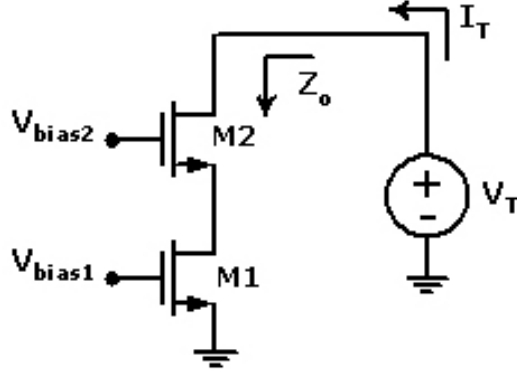
Figure A.6: Cascode amplifier using a testing voltage source for analysis.

the length of the channel formed between the Drain and Source terminals, which at the same time depends on the voltage between these two terminals.

To eliminate the lambda effect, we must consider a scheme that maintains the voltage V_{DS} constant and makes the current I_D depend on the voltage V_{GS} only. Consider the circuit in Figure A.5 where we have two transistors in series; this is known as cascoding [1, 2, 3]. This cell is very useful when using current mirrors and a very accurate copy of the V_{GS}^Q is required.

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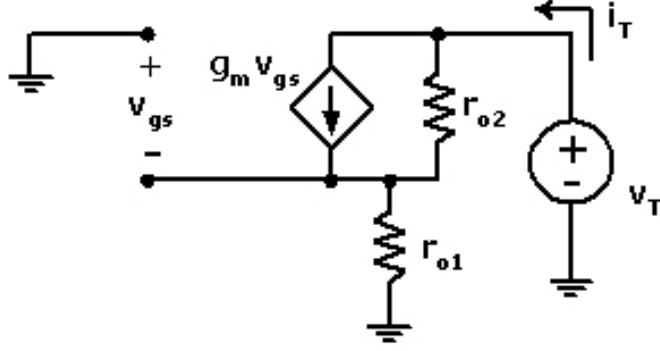
Figure A.7: Small signal model of circuit in Figure A.6.

To analyze the output impedance of the circuit we connect a testing voltage source at the output as shown in Figure A.6 and perform the small signal analysis as shown in Figure A.7.

Observe that the DC voltage sources become a short circuit to ground in small-signal analysis. Also, the voltage $V_{gs1} = 0$. Therefore, the dependent current source of M1 is not shown in the schematic. We know that the gain of a single transistor, in common-source configuration, is given by

$$A_v^N = \frac{v_o}{v_i} = \frac{g_{m2}V_{GS}r_o}{V_{GS}} = g_{m2}r_o \qquad (A.9)$$

From the circuit in Figure A.7 we get the expression

$$I_T = g_{m2}V_{GSM2} + I_{r_{o2}} = -g_{m2}V_x + (V_T - V_x)g_{o2} \qquad (A.10)$$

$$\Rightarrow g_{o2} = \frac{1}{r_{o2}}$$

$$V_x = I_T r_{o1} \Rightarrow I_T = V_x g_{o1} \qquad (A.11)$$

$$V_x g_{o1} = -g_{m2}V_x + (V_T - V_x)g_{o2} \qquad (A.12)$$

$$V_x = V_T \cdot \frac{g_{o2}}{g_{o1} + g_{o2} + g_{m2}} \qquad (A.13)$$

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$$Z_{o3} = (g_{m3} \cdot r_{o3})(g_{m2} \cdot r_{o2}) \cdot r_{o1} + r_{o3} + r_{o2} + r_{o1} \cong (A_{v3})^2 \cdot r_{o1}$$

$$Z_{o2} = (g_{m2} \cdot r_{o2}) \cdot r_{o1} + r_{o2} + r_{o1} \cong A_{v2} \cdot r_{o1}$$

$$Z_{o1} = r_{o1}$$
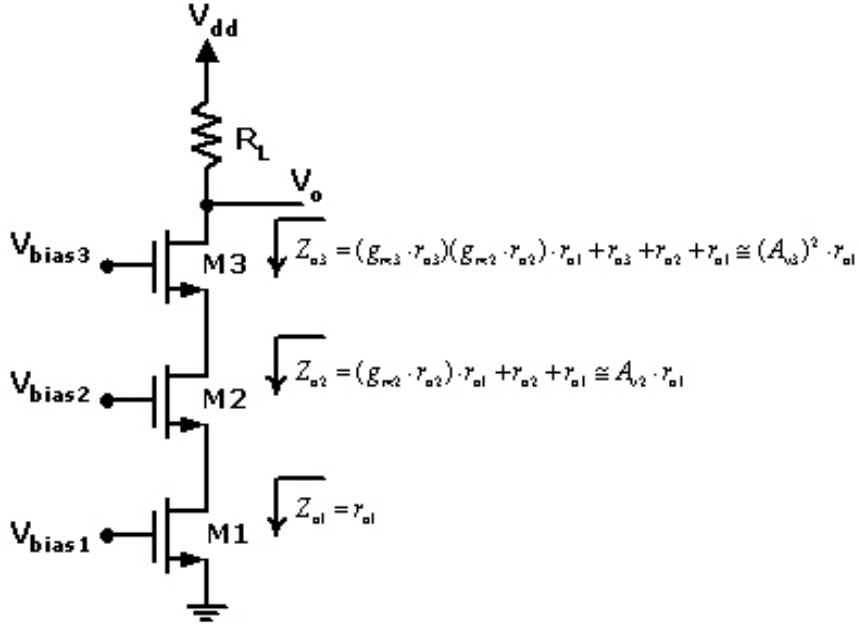
Figure A.8: Cascode amplifier and effect in output impedance when having one, two and three transistors in series.

$$I_T = \frac{g_{o2} \cdot g_{o1}}{g_{o1} + g_{o2} + g_{m2}} \cdot V_T \tag{A.14}$$

$$R_{out} = \frac{V_T}{I_T} = \frac{g_{o1} + g_{o2} + g_{m2}}{g_{o2} \cdot g_{o1}}$$

$$= \frac{1}{g_{o2}} + \frac{1}{g_{o1}} + \frac{g_{m2}}{g_{o2} \cdot g_{o1}}$$

$$= r_{o2} + r_{o1} + g_{m2} \cdot r_{o2} \cdot r_{o2}; \Rightarrow g_{m2} \cdot r_{o2} = A_{vM2} \tag{A.15}$$

$$\cong A_{vM2} \cdot r_{o1} \tag{A.16}$$

This relation describes that the output impedance of M1 is enhanced approximately by the gain of transistor M2. Therefore, if we connect another transistor M3 in series, as shown in Figure A.8, the impedance at the output of that transistor is also enhanced by the gain of M3, as shown in Figure A.9.
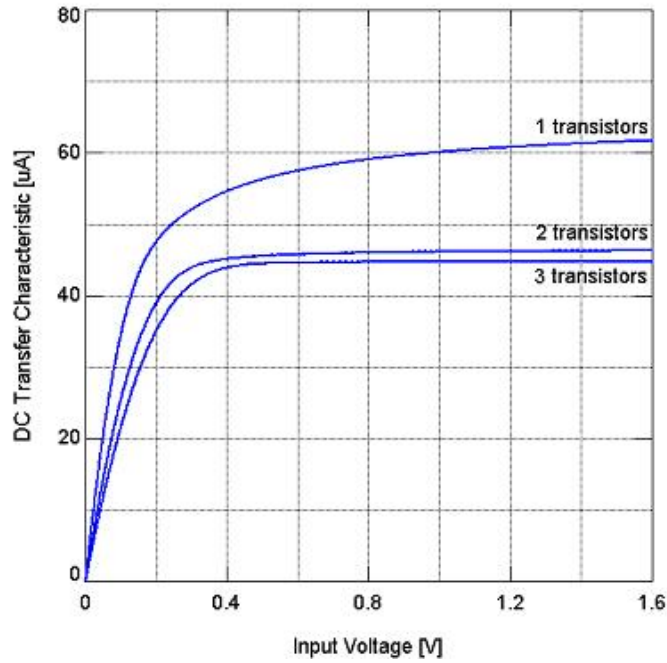
Figure A.9: Behavior of circuit in Figure A.8 with one, two and three transistors in series.

With this design we eliminate the lambda effect. This behavior is described in Figure A.3.5. Notice that we get a more constant behavior of I_D for variations in V_{DS} when using more transistors for cascoding.

Diode Connected Transistors

Figure A.10 shows the Diode-connected NMOS transistor [1,2,3], which is very useful in analog design, especially for current mirrors. Observe that here we have a connection between the Drain and Gate terminals, creating a two-terminal device. The Drain will change its voltage to adjust the V_{GS} according to the requirements of I_D. This is very useful for current mirrors when one is copying a biasing or signal current to another branch.

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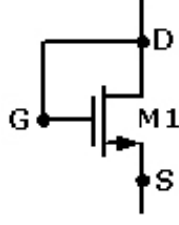
Figure A.10: NMOS transistor as diode connected.
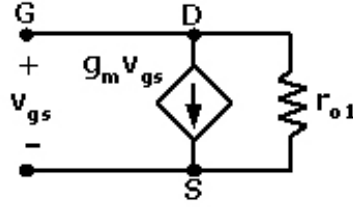
Figure A.11: Small signal model of the diode connected transistor.

Figure A.11 shows the small signal model. Observe that the impedance between Drain and Source is given by the relation

$$Z_{current\ source} = \frac{V_{DS}}{i_{DS}} = \frac{v_{gs}}{g_m v_{gs}} = \frac{1}{g_m} \tag{A.17}$$

$$Z_{DS} = \frac{1}{g_m}||r_{o1} \cong \frac{1}{g_m} \tag{A.18}$$

The impedance of this two-terminal device is $R = 1/g_m$; this is very useful for current mirrors and to implement resistive loads.

Compensation of a Two-Stage Amplifier

The study of amplifiers indicates that two-stage opamps may become unstable if the output voltage swing is maximized. Therefore, frequency compensation of these opamps is required [1, 2].

Figure A.12: Conventional two-stage amplifier.

Consider the circuit shown in Fig. A.12, where $gm1$ and $gm2$ are the transconductance of the amplifiers, $1/g_1$ and $1/g_2$ are the output impedance of the amplifiers, and C_L is the load capacitance. We identify two poles, one at node 1 and anther one at node 2. We know that the bandwidth of a given node depends on the small signal impedance and capacitance seen from that node to signal ground, whether physical ground or either one of the rails. Even if the capacitance at these 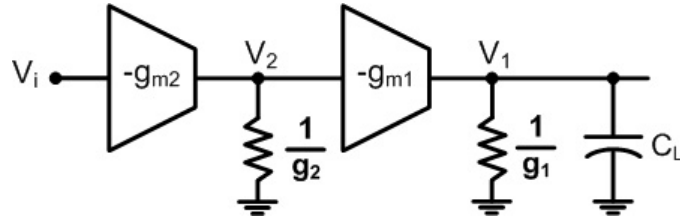two nodes may seem small, the small signal resistance is quite large. This is desired in some cases to achieve high voltage gain. However, this causes low-frequency poles at both of these nodes. Consequently, the circuit exhibits two dominant poles.

Due to high gain, opamps are commonly used with negative feedback to avoid saturation. This causes the signal to have a 180° phase shift as it is back to the circuit. In addition, each pole introduces an extra 90° phase shift. If two poles introduce an extra 180°, it would have a total of 360° shift in the phase. This results in positive feedback, and this causes oscillation and therefore in-stability.

Therefore, it is required to have the effect of only one pole in the signal path before the magnitude goes to zero when the frequency is increased. The

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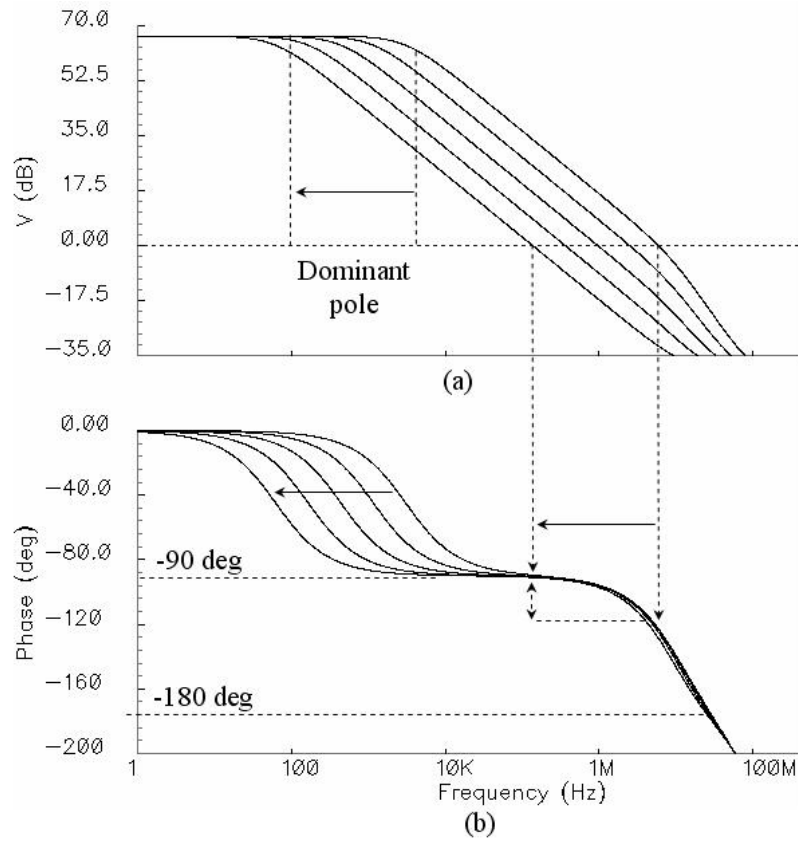
Figure A.13: a)Magnitude and b)phase of the output of a two-stage amplifier as the dominant pole is moved towards the origin.

magnitude and phase plots are shown in Fig. A.13. As described before, as the dominant pole is moved towards the origin, the magnitude decreases to zero before the first non-dominant pole introduces phase shift. With this, we avoid the feedback signal to reach 180° of phase shift, thus preventing oscillation.

Observe that as we move the dominant pole towards the origin, the magnitude of the gain drops before the first non-dominant pole contributes significant phase shift. To move the dominant pole towards the origin, sometimes a large
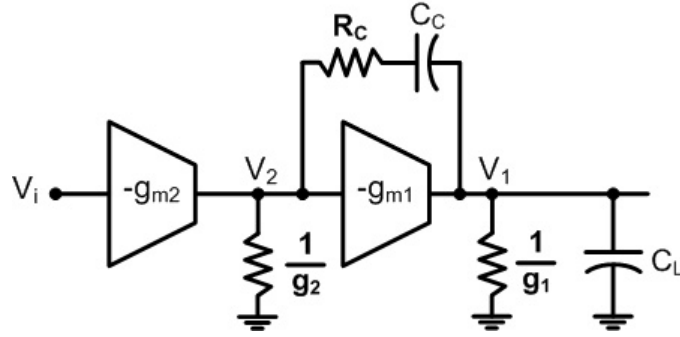
Figure A.14: Two-stage amplifier with Miller compensation network.
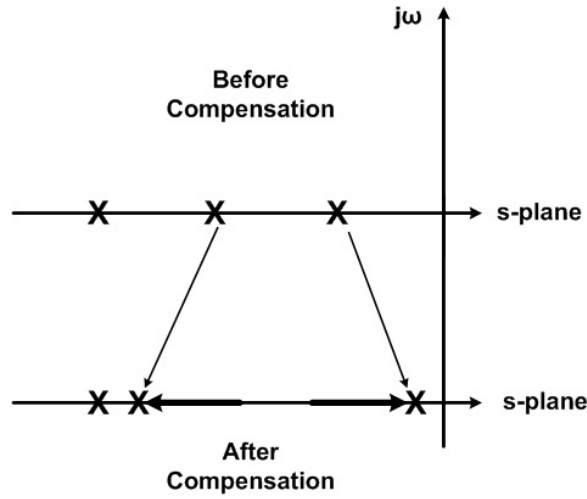
Figure A.15: Pole-splitting effect of the two-stage amplifier.

capacitance is required. An efficient way to achieve this is by compensating the

opamp using Miller's Theorem, as shown in Fig. A.14

Miller's Theorem effectively places a large capacitance at node 2, of the

value $C_C(1 - A_{v_1})$, moving the corresponding pole to $g_2/[C_C(1 - A_{v_1})]$. This effect

is known as pole-splitting, and is shown in Fig. A.15.

This pole-zero effect and phase can also be seen in the magnitude-phase

plot, as shown in Fig. A.16.
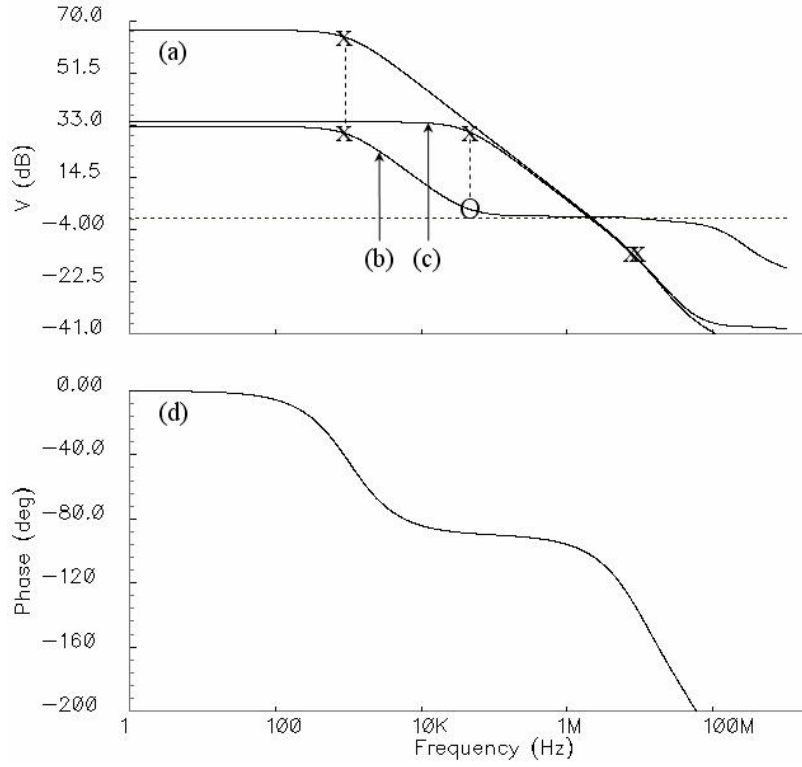
Figure A.16: Pole-zero effect of the two-stage amplifier seen in the magnitude-phase plot, showing a)A_v^{tot}, b)A_{v_1}, c)A_{v_2} and d)phase.

The small signal analysis is as follows: the amplification provided by g_{m1} is given by the expression:

$$A_{v_1} = \frac{V_1}{V_2} = -g_{m1}Z_1 \tag{A.19}$$

The parallel combination of the impedances found at node 1 and the Miller compensation network composed by C_C and R_C results in an impedance equivalent to:

$$Z_1 = \frac{1}{sC_L} \ || \ \frac{1}{g_1} \ || \ \left[\frac{1}{sC_C} + R_C\right] \cdot \left[\frac{1}{1 - \frac{1}{A_{v_1}}}\right] \tag{A.20}$$

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Therefore we obtain:

$$A_{v_1} = \frac{-g_{m1}\left(1 + sC_C R_C\right) + sC_C}{\left(1 + sC_C R_C\right)\left(sC_L + g_1\right) + sC_C} \tag{A.21}$$

Now, the gain provided by g_{m2} is given by:

$$A_{v_2} = \frac{V_2}{V_i} = -g_{m2} Z_2 \tag{A.22}$$

The parallel combination of the impedances found at node 2 and the Miller compensation network composed by C_C and R_C results in an impedance equivalent to:

$$Z_2 = \frac{1}{g_2} \; \| \; \left[\frac{1}{sC_C} + R_C\right] \cdot \left[\frac{1}{1 - A_{v_1}}\right] \tag{A.23}$$

Therefore, we obtain:

$$A_{v_2} = \frac{-g_{m2}\left(1 + sC_C R_C\right)}{g_2\left(1 + sC_C R_C\right) + sC_C\left(1 - A_{v_1}\right)} \tag{A.24}$$

Thus, the overall gain is given by

$$\begin{aligned} A_v &= A_{v_1} \cdot A_{v_2} \\ &= \left(\frac{g_{m1}}{g_1}\right) \cdot \left(\frac{g_{m2}}{g_2}\right). \end{aligned} \tag{A.25}$$

From this analysis, we observe that this amplifier has poles at nodes 1 and 2 given by:

$$\omega_{p1} \approx \frac{g_1}{C_L} = \frac{1}{r_{o1} C_L} \tag{A.26}$$

$$\omega_{p2} \approx \frac{g_2}{A_{v_2} \cdot C_C} = \frac{1}{r_{o2}\left(A_{v_2} \cdot C_C\right)} \tag{A.27}$$

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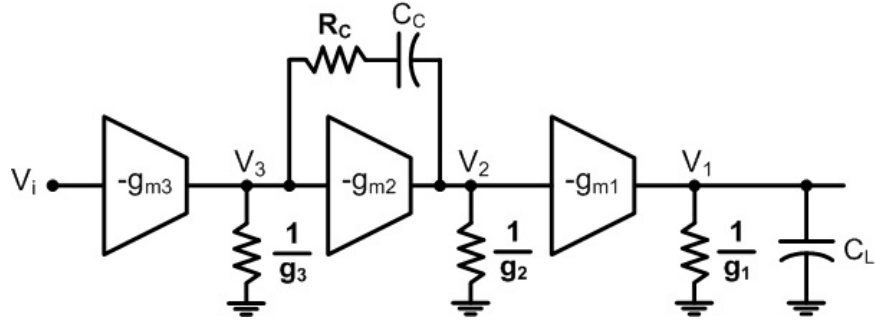
Figure A.17: Three-stage amplifier with Miller compensation network.

Also, a zero

$$\omega_z \quad \approx \quad \frac{1}{C_C \left(\frac{1}{g_{m1}} - R_C \right)} \tag{A.28}$$

Compensation of a Three-Stage Amplifier

In the same manner as we analyzed the two-stage amplifier, we require a compensated system when the amplifier consists of three gain stages, such as the one shown in Fig. A.17.

It was demonstrated in [39], that a three-stage amplifier can be effectively compensated if a compensating network is included in the second stage. The pole-splitting effect is described in Fig. A.18. As a note, the zero generated by R_C is utilized to cancel the pole generated in the consecutive gain stage ω_{p2}, as described in the following small signal analysis.

Again, the pole-zero effect can also be seen in the magnitude-phase plot, shown in Fig. A.19.

Figure A.18: Pole-splitting effect of the three-stage amplifier.

Figure A.19: Pole-zero effect of the three-stage amplifier seen in the magnitude-phase plot, showing a)A_v, b)A_{v_1}, c)A_{v_2}, d)A_{v_3} and e)phase.

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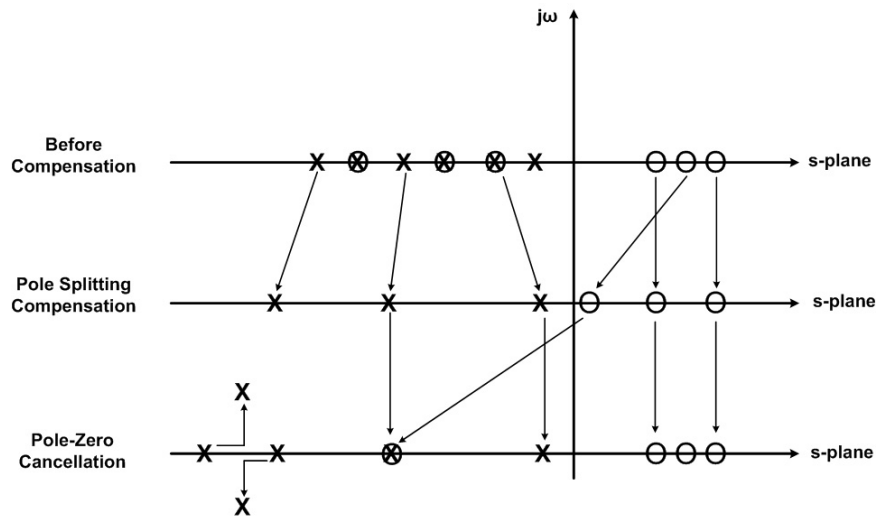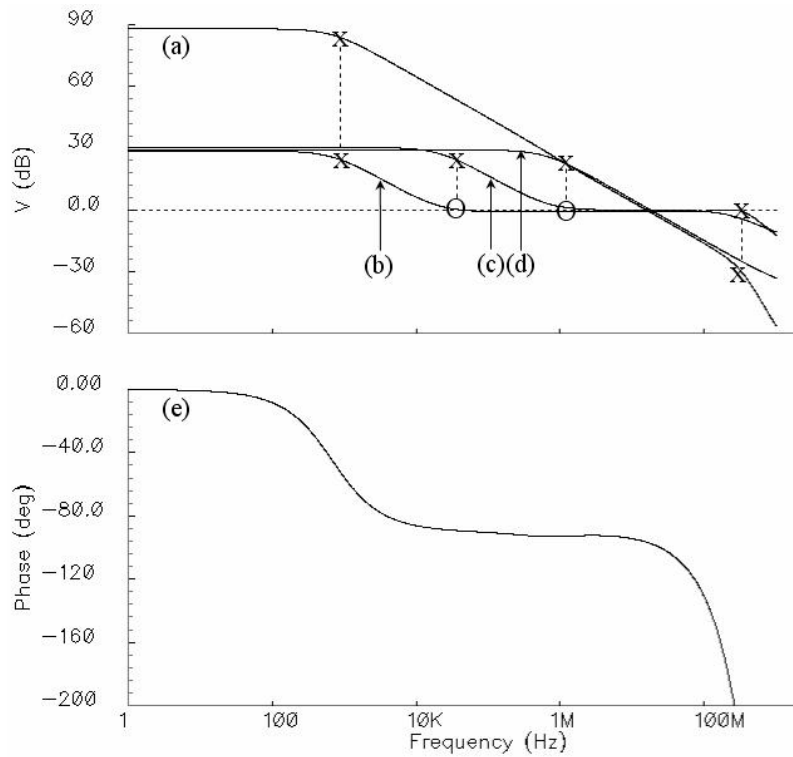
Following the same analysis as in the case of the two-stage amplifier, the gain from g_{m1} is given by:

$$A_{v_1} = \frac{V_1}{V_2} = -g_{m1}Z_1 \tag{A.29}$$

The parallel combination of the impedances at node 1 gives an equivalent impedance given by

$$Z_1 = \frac{1}{sC_L} \ || \ \frac{1}{g_1} \tag{A.30}$$

Therefore, we obtain:

$$A_{v_1} = \frac{-g_{m1}}{g_1 + sC_L} \tag{A.31}$$

The amplification provided by g_{m2} is given by the expression:

$$A_{v_2} = \frac{V_2}{V_3} = -g_{m2}Z_2 \tag{A.32}$$

The parallel combination of the impedances found at node 2, and the Miller compensation network composed by C_C and R_C results in an impedance equivalent to:

$$Z_2 = \frac{1}{g_2} \ || \ \left[\frac{1}{sC_C} + R_C\right] \cdot \left[\frac{1}{1 - \frac{1}{A_{v_2}}}\right] \tag{A.33}$$

Therefore, we obtain:

$$A_{v_2} = \frac{-g_{m2}\left(1 + sC_C R_C\right) + sC_C}{\left(1 + sC_C R_C\right)g_2 + sC_C} \tag{A.34}$$

Now, the gain provided by g_{m3} is given by:

$$A_{v_3} = \frac{V_3}{V_i} = -g_{m3}Z_3 \tag{A.35}$$

The parallel combination of the impedances found at node 3 and the Miller compensation network composed by C_C and R_C results in an impedance equivalent to:

$$Z_2 = \frac{1}{g_3} \,||\, \left[\frac{1}{sC_C} + R_C\right] \cdot \left[\frac{1}{1 - A_{v_2}}\right] \tag{A.36}$$

Therefore, we obtain:

$$
\begin{aligned}
A_{v_3} &= \frac{-g_{m3}\left(1 + sC_C R_C\right)}{g_3\left(1 + sC_C R_C\right) + sC_C\left(1 - A_{v_2}\right)} \\
&= \frac{-g_{m3}\left(\left(1 + sC_C R_C\right)g_1 + sC_C\right)}{g_3\left(\left(1 + sC_C R_C\right)g_1 + sC_C\right) + sC_C\left(g_1 - g_{m1}\right)}
\end{aligned}
\tag{A.37}
$$

Thus, the overall gain is given by

$$
\begin{aligned}
A_v &= A_{v_1} \cdot A_{v_2} \cdot A_{v_3} \\
&= \left(\frac{g_{m1}}{g_1}\right) \cdot \left(\frac{g_{m2}}{g_2}\right) \cdot \left(\frac{g_{m3}}{g_3}\right).
\end{aligned}
\tag{A.38}
$$

From this analysis, we observe that this amplifier has poles at

Dominant pole

$$\omega_{p1} \approx -\frac{g_3 g_2}{g_{m2} C_C} \tag{A.39}$$

First non-dominant pole

$$\omega_{p2} \approx -\frac{g_{m2} g_1}{g_{m2} C_L} \tag{A.40}$$

Second non-dominant pole

$$\omega_{p3} \approx -\frac{g_{m2}}{C_{L_2} + C_{L_3}} \tag{A.41}$$

Also, a zero

$$\omega_z \approx -\frac{g_{m2}}{C_C \left(R_C g_{m2} - 1\right)} \tag{A.42}$$

And the value of R_C needed to cancel the first non-dominant pole ω_{p2} is

$$R_C \approx \frac{1}{g_{m2}} \left(\frac{g_{m2} C_L}{g_1 C_C} + 1\right) \tag{A.43}$$

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