AND9093/D

Using MOSFETs in Load Switch Applications

ON Semiconductor®

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APPLICATION NOTE

Introduction

In today's market, power management is more important than ever. Portable systems strive to extend battery life while meeting an ever increasing demand for higher performance. Load switches provide a simple and inexpensive method for the system to make the appropriate power management decisions based on which peripherals or sub-circuits are currently in use. Load switches are found in notebooks, cell phones, hand held gaming systems and many other portable devices.

The load switch is controlled by the system, and connects or disconnects a voltage rail to a specific load. By turning unused circuitry off, the system as a whole can run more efficiently. The load switch provides a simple means to power a load when it is in demand and allows the system to maximize performance.

Load Switch Basics

A load switch is comprised of two main elements: the pass transistor and the on/off control block, as shown in Figure 1.

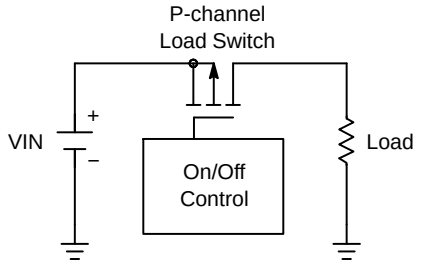

Figure 1. Example Load Switch Circuit

The pass transistor is most commonly a MOSFET (either N-channel or P-channel) that passes the voltage supply to a specified load when the transistor is on.

N-channel and P-channel Considerations

The selection of a P-channel or N-channel load switch depends on the specific needs of the application. The N-channel MOSFET has several advantages over the P-channel MOSFET. For example, the N-channel majority carriers (electrons) have a higher mobility than the P-channel majority carriers (holes). Because of this, the N-channel transistor has lower $R_{DS(on)}$ and gate capacitance for the same die area. Thus, for high current applications the N-channel transistor is preferred.

When using an N-channel MOSFET in a load switch circuit, the drain is connected directly to the input voltage rail and the source is connected to the load. The output voltage is defined as the voltage across the load, and therefore:

$$V_S = V_{OUT} \quad \text{(eq. 1)}$$

In order for the N-channel MOSFET to turn on, the gate-to-source voltage must be greater than the threshold voltage of the device. This means that:

$$V_G \geq V_{OUT} + V_{th} \quad \text{(eq. 2)}$$

In order to meet Equation 2, a second voltage rail is needed to control the gate. Therefore, the input voltage rail can be considered independently of the pass transistor. Because of this, the N-channel load switch can be used for very low input voltage rails or for higher voltage rails, as long as the gate-to-source voltage V_{GS} remains higher than the threshold voltage of the device. The designer must ensure that the device maximum ratings and the safe operating area of the MOSFET are not violated.

When using a P-channel MOSFET in a load switch circuit (as in Figure 1, the source is directly connected to the input voltage rail and the drain is connected to the load. In order for the P-channel load switch to turn on, the source-to-gate voltage must be greater than the threshold voltage. Therefore:

$$V_{IN} \geq V_G + V_{th} \quad \text{(eq. 3)}$$

At minimum, the input voltage rail must be greater than the threshold voltage of the selected pass transistor (assuming the gate voltage is 0 V when the load switch is turned on).

The P-channel MOSFET has a distinct advantage over the N-channel MOSFET, and that is in the simplicity of the on/off control block. The N-channel load switch requires an additional voltage rail for the gate; the P-channel load switch does not. As with the N-channel MOSFET, the designer must ensure that the device maximum ratings and the safe operating area of the P-channel MOSFET are not violated.

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Load Switch Control Circuit Considerations

There are multiple ways to implement the on/off control block in a load switch circuit. This section will cover one control circuit example for the N-channel and one for the P-channel load switch.

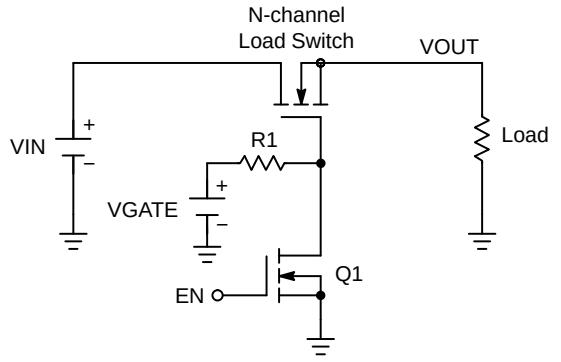

Figure 2. N-channel Example Control Circuit

Figure 2 shows an example load switch control circuit for an N-channel pass transistor. A logic signal from the system power management control circuitry turns the load switch on and off via a small-signal NMOS transistor, Q1. When EN is LOW, Q1 is off and the pass transistor gate is pulled up to V_{GATE} to keep it turned on. When EN is HIGH, Q1 turns on, the pass transistor gate is pulled to ground, and the load switch turns off. Resistor R1 is selected so that milliamps of current or less flow through R1 when Q1 is on. A standard range is 1 kΩ – 10 kΩ.

An additional voltage source, V_{GATE}, is needed to keep the gate-to-source forward biased. As expressed in Equation 2, the gate voltage must be larger than the sum of the output voltage and the threshold voltage. This may be undesirable for systems that do not have an extra voltage rail available.

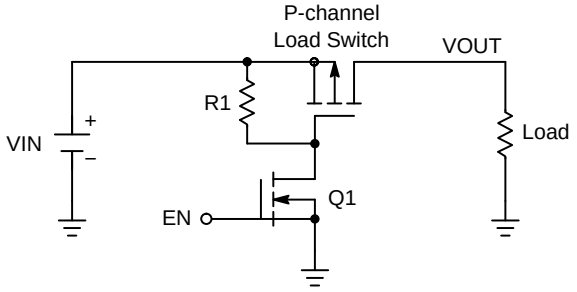

Figure 3. P-channel Example Control Circuit

Figure 3 shows an example load switch control circuit for a P-channel pass transistor. As with the N-channel example, a logic signal from the system power management control circuitry turns the load switch on and off via a small-signal NMOS transistor, Q1. When EN is LOW, Q1 is off and the gate is pulled up to V_{IN}. When EN is HIGH, Q1 turns on, the pass transistor gate is pulled to ground, and the load switch turns on. As long as the input voltage rail is higher than the threshold voltage of the PMOS transistor, it will turn on when EN is HIGH without the need of an additional voltage source. As with the N-channel control circuit, resistor R1 is selected so that milliamps of current or less flow through R1 when Q1 is on. A standard range is 1 kΩ – 10 kΩ.

For both control circuit implementations, the small-signal NMOS transistor, Q1, can be integrated into the same package as the pass transistor.

Efficiency Considerations

Efficiency is critical to the success of the overall power management of the system. In a load switch circuit, the load current flows directly through the pass transistor when it is turned on. Therefore, the main power loss is the conduction loss.

$$P_{LOSS} = I_{LOAD}^{\ 2} \cdot R_{DS(on)} \qquad \text{(eq. 4)}$$

The $R_{DS(ON)}$ of the pass transistor causes a voltage drop between the input voltage and the output voltage, as shown in Equation 5. For applications requiring high load currents or low voltage rails, this voltage drop becomes critical. The voltage drop will increase as the load current increases, and the voltage drop at maximum load must be taken into consideration when selecting the pass transistor.

$$V_{OUT} = V_{IN} - I_{LOAD} \cdot R_{DS(on)} \qquad \text{(eq. 5)}$$

As discussed in previous sections, the N-channel MOSFET has an $R_{DS(on)}$ advantage over the P-channel MOSFET for a given die size. The $R_{DS(on)}$ of an N-channel device can be two times lower than the $R_{DS(on)}$ of a P-channel device of similar die area. This difference is most prominent at higher currents, but the N-channel $R_{DS(on)}$ advantage becomes less prominent at lower currents. For applications such as cell phones and other portable low power devices, higher efficiency can be attained using a P-channel pass transistor, with the advantage of a simpler control circuit.

To illustrate this, let's assume that a 30 mΩ N-channel transistor and a 50 mΩ P-channel transistor have similar die size. The efficiency impact of the two devices will be examined for a high current application and a low current application.

For the first example, consider an application that requires a maximum load current of 10 A. Using Equations 4 and 5, the power loss at the maximum load is calculated to be 3 W for the N-channel transistor, and the voltage drop across the transistor is 300 mV. The power loss at the maximum load is 5 W for the P-channel transistor, and the voltage drop across the transistor is 500 mV.

Now consider an application in which the maximum current is 2 A. The power loss at maximum load is 120 mW for the N-channel device and 200 mW for the p-channel device. The voltage drop for the N-channel transistor is 60 mV and is 100 mV for the P-channel transistor.

As a final example, consider an application with an 850 mA maximum load current. The 30 mΩ N-channel transistor's power loss is 21.7 mW compared to the 36.1 mW power loss of the 50 mΩ P-channel transistor of similar die size. For low current applications, the N-channel

$R_{DS(ON)}$ advantage becomes negligible. P-channel pass transistors can be designed to have $R_{DS(on)}$ as low as 8 mΩ. Low $R_{DS(on)}$ is critical for maximizing the efficiency of the load switch circuit and minimizing the voltage drop across the pass transistor. The specific conditions of the load switch application must be considered to make the final decision to use a PMOS or NMOS pass transistor.

Gate-to-Source Voltage Considerations

The applied gate-to-source voltage of the pass transistor directly affects the efficiency of the circuit because $R_{DS(on)}$ is inversely proportional to the applied gate-to-source voltage. Figure 4 shows an example $R_{DS(on)}$ curve over a V_{GS} range.

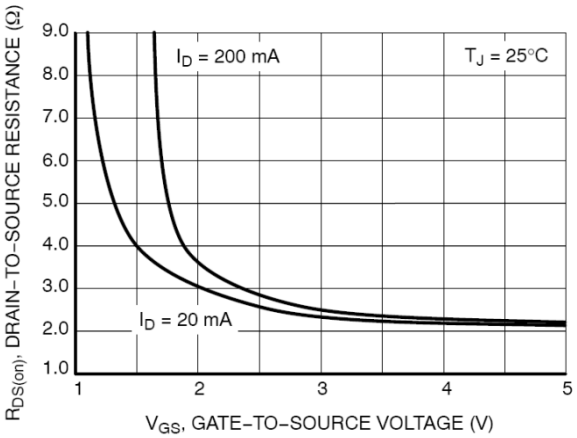

Figure 4. Example $R_{DS(on)}$ vs. V_{GS} Curve

The available V_{GS} of the circuit must be considered when selecting the pass transistor. Operating too close to the knee of the $R_{DS(on)}$ curve can lead to higher conduction losses. Any small change in the gate-to-source voltage could result in a large change in the $R_{DS(on)}$.

Turn-on Considerations

Proper turn-on of the load switch pass transistor is critical for maximizing circuit performance and maintaining safe operation of the individual components. Optimal turn-on speed depends on the needs of the specific application and the device parameters of the selected load switch. If the turn-on speed is too fast, a transient current spike occurs on the input voltage supply, known as inrush current.

Inrush Current

Inrush current occurs when the load switch is first turned on and is connected to a capacitive load, as shown in Figure 5. The capacitive load could be a battery, a DC:DC circuit, or other sub-circuit. The turn-on speed of the pass transistor directly influences the amount of inrush current seen on the input of the load switch.

Inrush current causes a dip in the input supply voltage that can adversely impact the functionality of the entire system. Likewise, inrush current spikes can potentially damage the load switch circuit components or reduce the lifetime of the components.

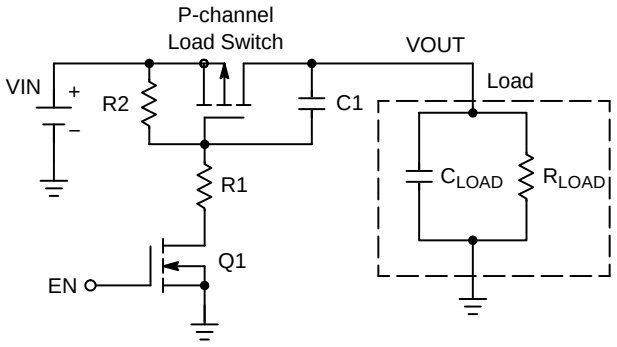

Figure 5. Load Switch with Capacitive Load

When the load switch is first turned on, an inrush current event occurs on the input as the C_{LOAD} is charged. This can be seen in Equation 6:

$$I_{inrush} = C_{LOAD} \cdot \frac{dV}{dt} \quad \text{(eq. 6)}$$

The faster the device switches on, the higher the inrush current will be. This potentially harmful inrush current can be reduced by controlling the load switch turn-on characteristics.

Figure 6 shows the simplified MOSFET turn-on transfer curves. There are four main regions for device turn-on, and each will be briefly addressed.

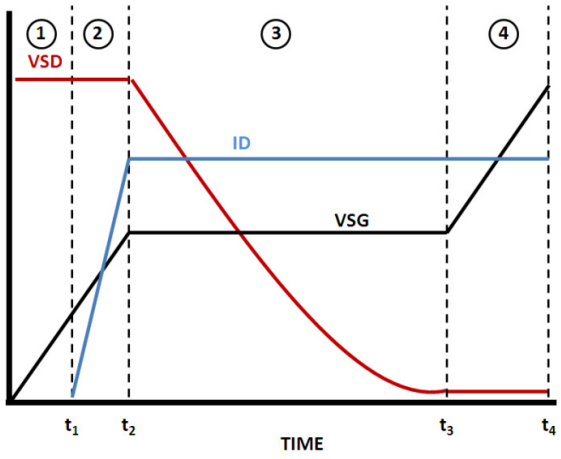

Figure 6. MOSFET Turn-on Waveforms

During Region 1, V_{SG} increases until it reaches V_{TH}. Because the device is off, V_{SD} remains at V_{DD}. During Region 2, V_{SG} rises above the V_{TH} and the device begins to turn on. Additionally, I_D increases to the final load current and C_{GS} charges.

In Region 3, V_{SG} remains constant as V_{SD} decreases to its saturation level, and C_{GD} charges. During Region 4, both C_{GS} and C_{GD} are fully charged, the device is fully on, and V_{SG} rises to its final drive voltage, V_{DR}. The plateau voltage, V_{PL},is defined as:

$$V_{PL} = V_{th} + \frac{I_{LOAD}}{g_{fs}} \quad \text{(eq. 7)}$$

In order to control the turn-on speed of the load switch, an external resistor R1 and external capacitor C1 are added to the load switch circuit as shown in Figure 7.

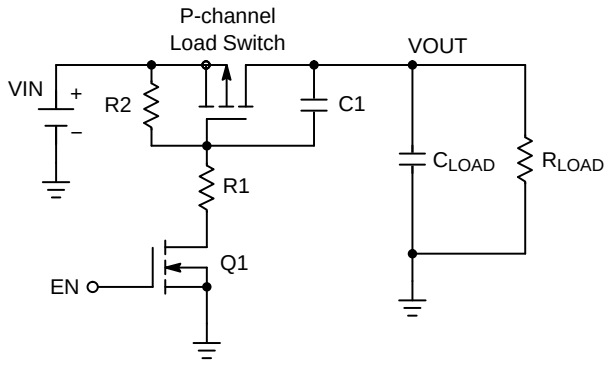

Figure 7. Inrush Current Limiting Circuit

The selection of R1, R2 and C1 is very important to the performance of the load switch circuit. C1 must be much larger than the C_{GD} of the load switch device so this capacitance will dominate over C_{GD}. By placing C1 between the drain and source of the pass transistor, Region 3 of the V_{SD} curve becomes linear and the MOSFET slew-rate, dV_{SD}/dt, can be controlled.

R1 and R2 form a voltage divider that determines the voltage seen at the gate of the pass transistor. R1 and R2 can be calculated by using Equation 8 when the small-signal N-channel device is on.

$$\frac{R_1}{R_1 + R_2} = 1 - \frac{V_{SG,MAX}}{V_{IN}} \qquad \text{(eq. 8)}$$

In order to ensure that V_{SG} does not exceed the maximum rating of the device, $V_{SG,MAX}$ is used. $V_{SG,MAX}$ can be found in the device datasheet (see Figure 8). R2 is the pull-up resistor described in previous sections, and is recommended to be between 1 kΩ and 10 kΩ.

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Value	Units
Drain-to-Source Voltage	V_{DSS}	−20	V
Gate-to-Source Voltage	V_{GS}	±8.0	V

Figure 8. Maximum VGS Spec Example from Datasheet

R1 and C1 determine the turn-on speed of the pass transistor. C1 can be calculated by using Equation 9, where I_{INRUSH} is the desired maximum inrush current for the load switch circuit.

$$C_1 = \left(\frac{V_{IN} + VPL}{R_1} + \frac{V_{PL}}{R_2}\right) \cdot \frac{C_{LOAD}}{I_{INRUSH}} \qquad \text{(eq. 9)}$$

Plugging Equation 7 into Equation 9, C_1 becomes:

$$C_1 = \left[\frac{V_{IN} + V_{th} - \left(\frac{I_{LOAD}}{g_{fs}}\right)}{R_1} + \frac{V_{th} - \left(\frac{I_{LOAD}}{g_{fs}}\right)}{R_2}\right] \cdot \frac{C_{LOAD}}{I_{INRUSH}} \qquad \text{(eq. 10)}$$

For many designs, the equivalent C_{LOAD} may be an unknown. If this is the case, C_{LOAD} can be estimated from the measured inrush current waveform of the circuit without the addition of R1 and C1. Figure 9 shows an example inrush current waveform for a load switch circuit similar to Figure 5.

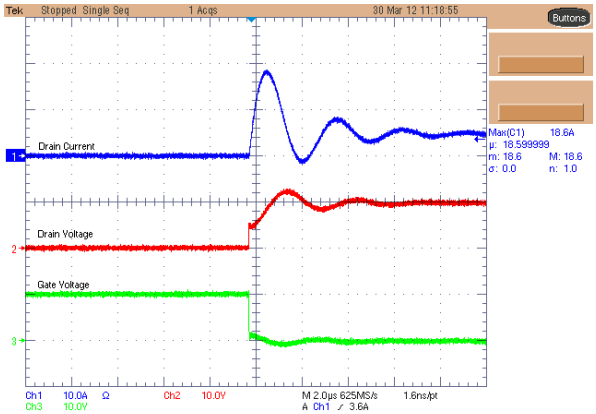

Figure 9. Example Inrush Current Without R1 or C1

The load capacitance, C_{LOAD}, can be estimated using the following equation:

$$C_{LOAD} = \frac{1}{2} \cdot \Delta t \cdot \Delta I \qquad \text{(eq. 11)}$$

For the example current waveform shown in Figure 9, C_{LOAD} is estimated as:

$$C_{LOAD} = \frac{1}{2} \cdot 1.6\ \mu s \cdot 18\ A = 1.28\ \mu F$$

Inrush Current Example

Consider the P-channel load switch circuit shown in Figure 7 with the following parameters:

Table 1. LOAD SWITCH CIRCUIT EXAMPLE

Circuit Parameters	PMOS Parameters
V_{IN} = 10 V	$V_{SD,MAX}$ = 20 V
$I_{LOAD,MAX}$ = 5 A	$V_{SG,MAX}$ = 8 V
$I_{IN,MAX}$ = 8 A	V_{TH} = −0.67 V
C_{LOAD} = 1 μF	g_{fs} = 5.9 S

First, R1 and R2 must be selected. For this example, a 1 kΩ resistor was selected for R2. R1 was calculated by rearranging Equation 8 and solving for R1:

$$R_1 = R_R \cdot \frac{V_{IN} - V_{SGMAX}}{V_{SGMAX}} = \frac{R_2}{4} = 250\ \Omega$$

Next, C1 is calculated using Equation 10 and the parameters in Table 1.

$$C_1 = \left(\frac{10 - 0.67 - \left(\frac{5}{5.9}\right)}{250} + \frac{-0.67 - \left(\frac{5}{5.9}\right)}{1000} \right) \cdot \frac{1\ \mu F}{3}$$

$$C_1 = 10.8\ nF$$

Therefore, for the example circuit, the inrush current will be limited to 3 A by selecting a 1 kΩ pull-up resistor (R1), a 250 Ω resistor for R2 and a 10 nF capacitor for C1.

Turn-on Speed

Turn-on speed plays an important role in the behavior of the load switch. As mentioned, a fast device turn-on creates an inrush current. A softer turn-on reduces this current spike. However, caution must be taken when slowing down the MOSFET turn-on.

Figure 10 shows a standard load switch datasheet transfer curve. Drain current versus gate-to-source voltage is plotted at three different temperatures.

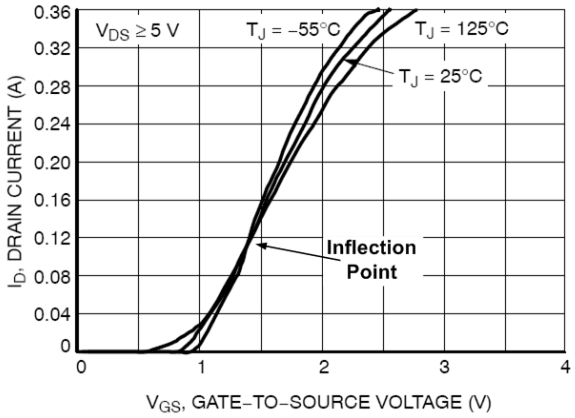

Figure 10. Example Transfer Curve for a Load Switch

All three temperature curves will intersect at a specific V_{GS}. This point is known as the inflection point. For a V_{GS} above the inflection point, $R_{DS(on)}$ increases as temperature increases. Thus, as the device heats up, cells that are carrying higher current will become more resistive and current will be shared with cells carrying lower current. This MOSFET property creates a uniform current sharing across all the cells. Below the inflection point, the MOSFET behaves more like a bipolar transistor. As the device heats up, a cell with higher current than the surrounding cells will continue to take more current. If the device remains within this transition region for too long, thermal runaway can occur.

The load switch should be operated with a V_{GS} above the inflection point to ensure proper device function. The threshold voltage for the example device shown in Figure 10 is around 0.8 V. The inflection point occurs around 1.75 V. For the example device, it is recommended to operate at a V_{GS} of 1.8 V or higher.

Safe Operating Area

The Safe Operating Area (SOA) defines the safe operating conditions of the load switch. Operation outside of this region can degrade the performance, reliability and lifetime of the device, and can potentially damage other components within the system.

The load switch must have a continuous current rating greater than the maximum load current of the application. Likewise, the MOSFET must not be operated outside of the maximum V_{DS} and V_{GS} specifications. The device datasheet specifies the absolute maximum ratings and also contains a figure showing the Safe Operating Area (SOA). The designer must evaluate whether the device will operate within its specified SOA for the application.

Figure 11 shows an example MOSFET SOA for an N-channel device. The outer boundaries of the safe operating area are determined by: the $R_{DS(on)}$ at maximum junction temperature, the maximum drain current I_{DM}, and the rated breakdown voltage V_{DSS} of the device. I_{DM} is limited by the package, source wires, gate wires and die characteristics.

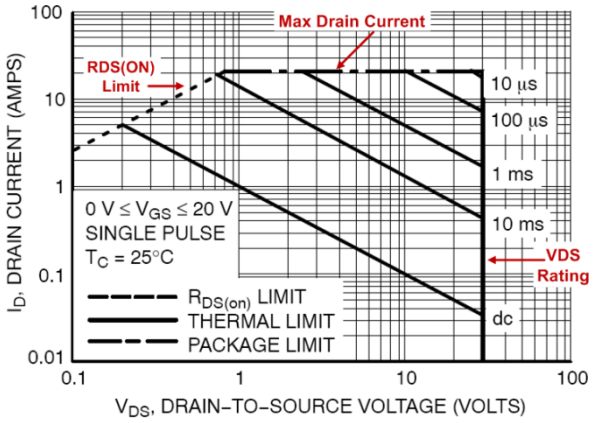

Figure 11. Example MOSFET SOA

The basic power and current equations used to generate the SOA curve are:

$$V_{DS} = \frac{P_D}{I_D} \quad \text{or} \quad I_D = \frac{P_D}{V_{DS}} \qquad \text{(eq. 12)}$$

$$I_D = \sqrt{\frac{R_D}{R_{DS(on)}, MAX@TJMAX}} \qquad \text{(eq. 13)}$$

First, the outer boundaries of the SOA are drawn: the maximum I_D and V_{DS} lines. Next, the $R_{DS(on)}$ boundary is drawn by using Equations 12 and 13 to determine the end points, and the slope of the $R_{DS(on)}$ boundary line is:

$$\frac{R_D}{R_{DS(on)}, MAX@TJMAX}$$

The DC line is determined by the maximum continuous power the device can dissipate. The continuous power dissipation is specified in the device datasheet. The DC line intersects the outer SOA boundaries in two places: at the $R_{DS(on)}$ limit and at the V_{DS} limit. Additional lines are plotted for a single pulse of 10 ms, 1 ms, 100 μs and 10 μs duration. The safe operation region is located within the

outer I_{DMAX} and V_{DSMAX} limits, and underneath the $R_{DS(on)}$, DC and single pulse lines.

The example MOSFET device from Figure 11 has the following datasheet specifications:

Table 2. EXAMPLE MOSFET DATASHEET SPECS

Datasheet Parameter	Datasheet Value
BV_{DSS}	30 V
$P_{D,CONTINUOUS}$	1 W
$I_{D,MAX}$	45 A
$R_{DS(ON)@TJMAX}$	33.5 mΩ

The $R_{DS(on)}$ line for the Figure 11 example MOSFET can be drawn using equations 12, 13 and the values presented in Table 2. The first end-point is located at a V_{DS} of 0.1 V, and the second end point is located at the I_D limit of 45 A.

Similarly, the DC line can be drawn using Equations 12 and 13 to calculate the end points. The first DC line end-point is at a V_{DS} of 30 V. Using Equation 12 and the P_D value presented in Table 2, the current at 30 V_{DS} is calculated to be 0.03 A. The second end-point is where the DC line intersects the $R_{DS(on)}$ boundary. Therefore, the current can be calculated using Equation 13 and then plugging the calculated drain current into Equation 12 to determine the corresponding voltage. For this example MOSFET, the DC line intersects the $R_{DS(ON)}$ boundary at 0.18 V and 5.5 A. The calculated V_{DS} and I_D values can be verified with Figure 11.

The single-pulse lines are calculated using the same methodology and equations as for the DC line, but using the power dissipation for a single pulse of: 10 ms, 1 ms, 100 μs and 10 μs.

ON Semiconductor Load Switches

ON Semiconductor has a large portfolio of P-channel and N-channel load switches in a wide variety of packages. ON Semiconductor load switches are offered in the following configurations: single, dual, and complementary. Table 3 lists just a few of the vast number of load switches that are currently available from ON Semiconductor. For a complete product list please visit www.onsemi.com.

Table 3. ON SEMICONDUCTOR LOAD SWITCHES

Package	Dimension (mm)	Part Number	Configuration	Pol	VDS (V)	VGS (V)	ID (A)	MAX $R_{DS(on)}$ (Ω)			
								V_{GS} 4.5 V	V_{GS} 2.5 V	V_{GS} 1.8 V	V_{GS} 1.5 V
XLLGA−3	0.6 x 0.6 x 0.4	NTNS3A91PZ**	Single	P	−20	±8	0.214	1.6	2.4	3.3	4.5
		NTNS3190NZ**	Single	N	−20	±8	0.229	1.4	1.9	2.7	4.3
SOT−883	1.0 x 0.6 x 0.4	NTNS3A65PZ**	Single	P	−20	±8	0.235	1.6	2.4	3.3	4.5
		NTNS3164NZ**	Single	N	−20	±8	0.245	1.5	2.0	4.0	6.8
SOT−963	1.0 x 1.0 x 0.5	NTUD3170NZ	Dual	N	20	±8	0.22	1.5	2.0	3.0	4.5
		NTUD3169CZ	Complimentary	N	−20	±8	0.22	1.5	2.0	3.0	4.5
				P	20	±8	0.25	5.0	6.0	7.0	10.0
SOT−723	1.2 x 1.2 x 0.5	NTK3139P**	Single	P	−20	±6	0.78	0.48	0.67	0.95	2.2
		NTK3134N**	Single	N	20	±6	0.89	0.35	0.45	0.65	1.2
UDFN	2.0 x 2.0 x 0.55	NTLUS3A18PZ**	Single	P	−20	±8	8.2	0.018	0.028	0.050	0.090
		NTLUS3A39PZ**	Single	P	20	±8	5.2	0.039	0.050	0.081	0.147
WDFN	3.3 x 3.3 x 0.8	NTTFS3A08PZ**	Single	P	20	±8	14	0.0067	0.0090	––	––

** New Products in Development. Samples Available Upon Request.

REFERENCES

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[3] Q. Deng. “A Primer on High-Side FET Load Switches. EE Times, May 2007.

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