

Reality-Driven Physical Synthesis

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Layout Secrets

"They" Don't Want You To Know About

Sad but true: ad-hoc EDA beats algorithms
Why Optimal is not Optimal at all
The disturbing truth about Place and Route
Shocking! 100% error in Static Timing Analysis

Simple solutions to complex problems!

AS SEEN AT ISPD

#1 NEW YORK TIMES BESTSELLER
Kevin Trudeau
THE WEIRDEST LOSERS
"They" Don't Want You to Know About
• THE REVEALING TRUTH
• GETS RID OF
FIND OUT!

CURES THEY DON'T WANT YOU TO KNOW ABOUT
ON FOR MORE
SES!

MAGMA

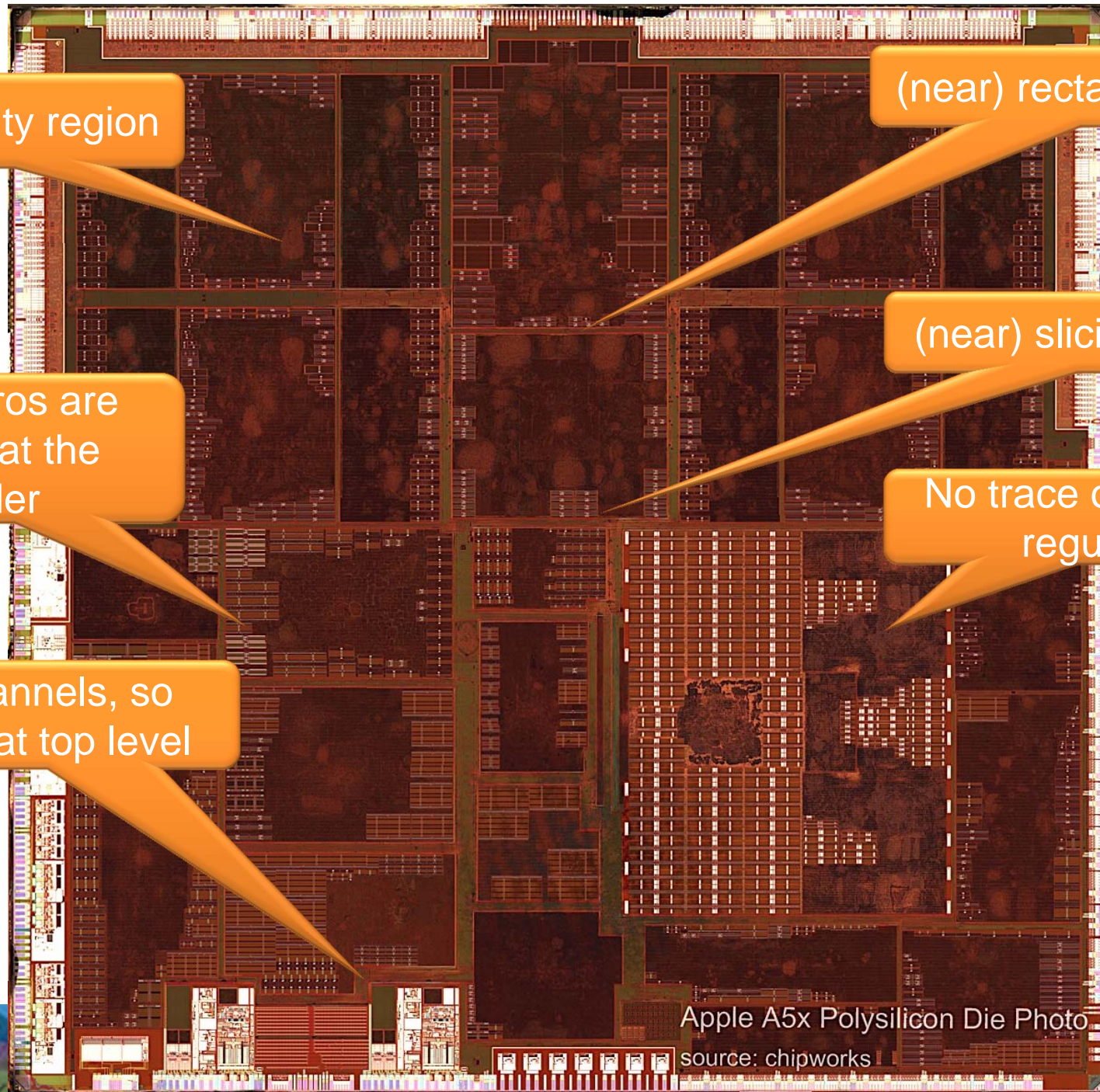
Physical Design of Apple processors

- Common technology:
 - 45nm Samsung
- A4: 2010
 - iPhone 4 & iPad 1
 - 7.3mm x 7.3mm
- A5: 2011
 - iPhone 4s & iPad 2
 - 10.0mm x 12.5mm
- A5x: 2012
 - iPad 3
 - 12.9mm x 12.7mm
= 3x as big as the A4

“The perceived usefulness of any new product is an underlying technology’s logarithmic function”
(Theo Claassen, 2003)



A closer look at the Apple's physical design style



Apple A5x Polysilicon Die Photo

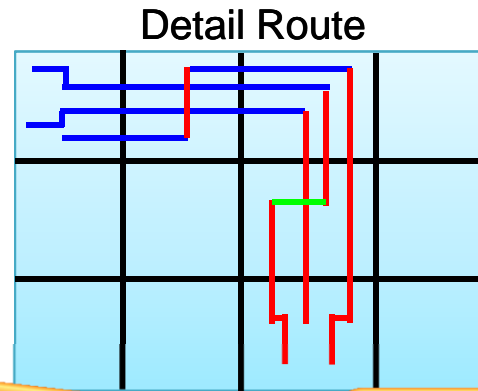
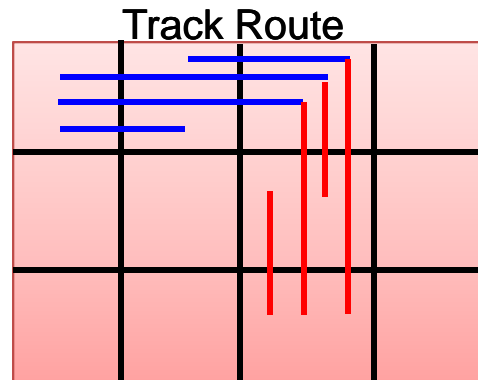
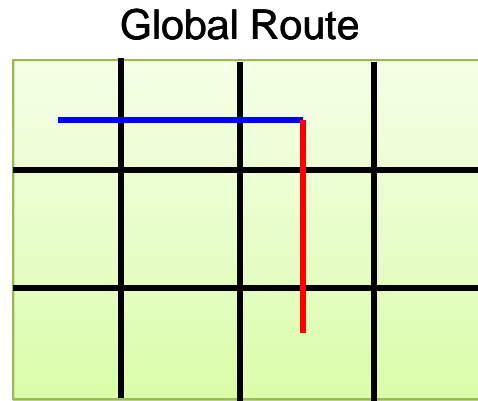
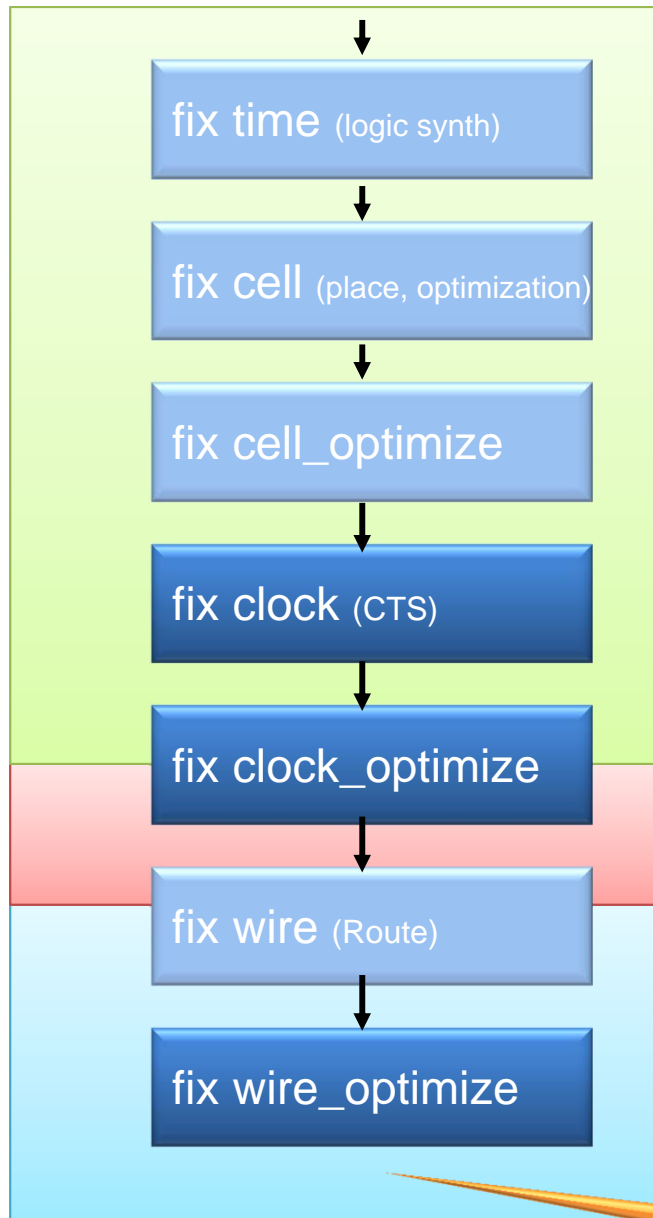
source: chipworks

PD: *Many* Objectives Simultaneously

- **Correct** & manufacturable mask pattern
 - Congestion control
 - Big chip = good
- Meets **timing** & electrical requirements
 - Battle parasitics: timing, voltage drop
 - Big gates = good, compact chip = good & a little better
- **Low power**
 - Leakage control, multi voltage, sleep, etc
 - Small gates = good, complex floorplan = necessary evil
- **Low part cost**
 - Compact chip, dense wires = good
- **Low design effort**
 - Robust design, short tool run times, re-use
 - Simple = good, pushbutton = good

Intricate trade-off

Magma Flow: guided by 'best available' data



- Global route:
 - Layer assignment
 - Congestion
 - Resource contention
 - Detours
- Track route:
 - Refines global route
- Detail route
 - Copies track route
 - Fixes opens
 - Ripup & Reroute

The only thing that matters is the quality at the end!

Layout Design at different levels of abstraction

The image displays the Magma Design Automation (MAGMA) interface, illustrating layout design at different levels of abstraction. The main window shows the Verilog code for a divider unit, with a schematic view on the left and a layout view on the right. The layout view shows a detailed routing of the divider unit, with a yellow box highlighting a specific area. The right panel shows the 'Worst Case Analysis' window, which provides a summary of the analysis results, including a table of exceptions.

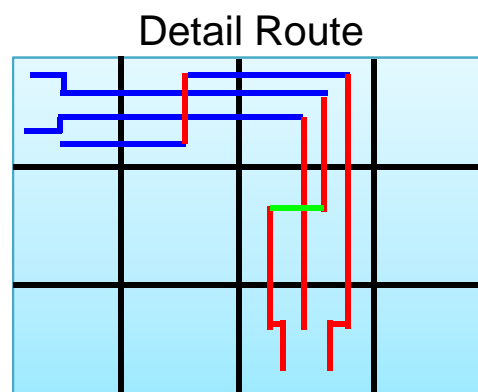
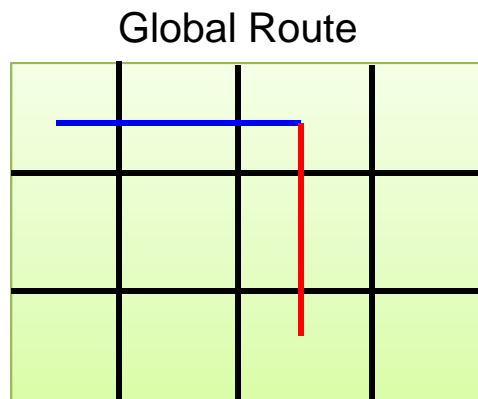
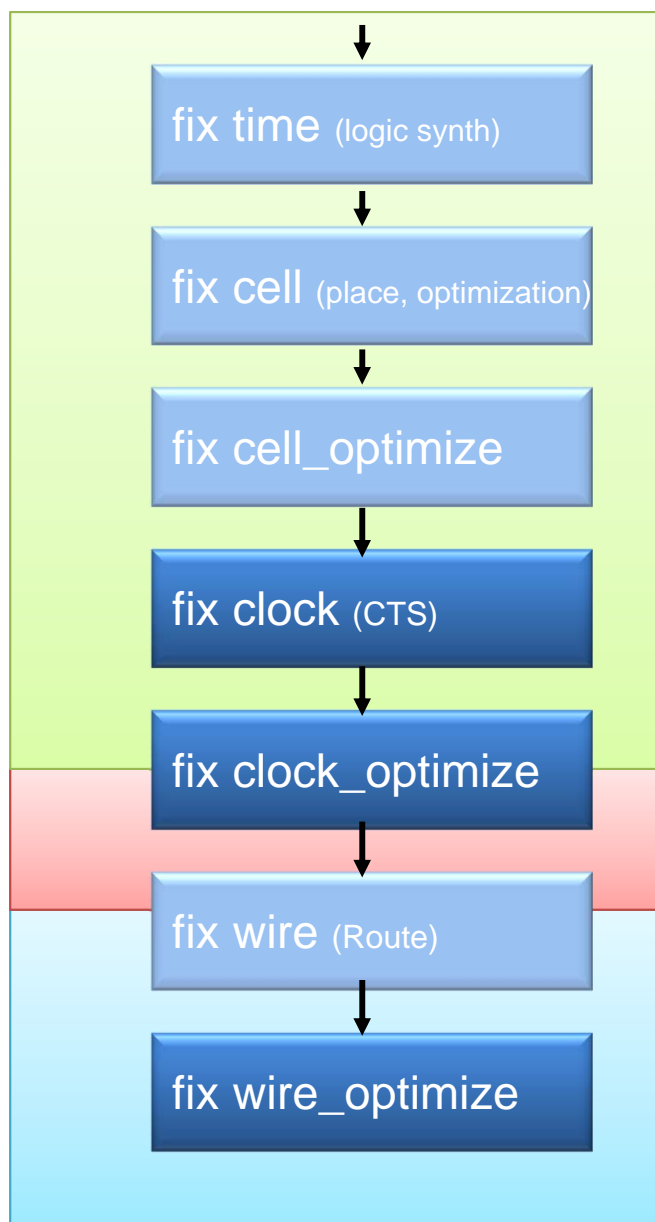
Verilog Code (serial_divide_uu.v):

```
170. divide_count <= 0;
171. // dividend placed initially so that remainder bits are zero...
172. grand_dividend <= dividend_i << R_PP;
173. // divisor placed initially for a 1 bit overlap with dividend...
174. // But adjust it back by S_PP, to account for bits that are known
175. // to be leading zeros in the quotient.
176. grand_divisor <= divisor_i << (N_PP+R_PP-S_PP-1);
177. end
178. else if (divide_count == M_PP+R_PP-S_PP-1)
179. begin
180. if (~done_o) quotient <= quotient_node; // final shift...
181. if (~done_o) quotient_reg <= quotient_node; // final shift (held output)
182. done_o <= 1; // Indicate done, just sit
183. end
184. else // Division in progress
185. begin
186. // If the subtraction yields a positive result, then store that result
```

Worst Case Analysis Table:

line	AT	entity name
89	891	oai21d1
89	892	aoi21d1
89	947	aoi21d1
89	949	aoi21d1
89	1017	aoi21d1

What is the timing accuracy?



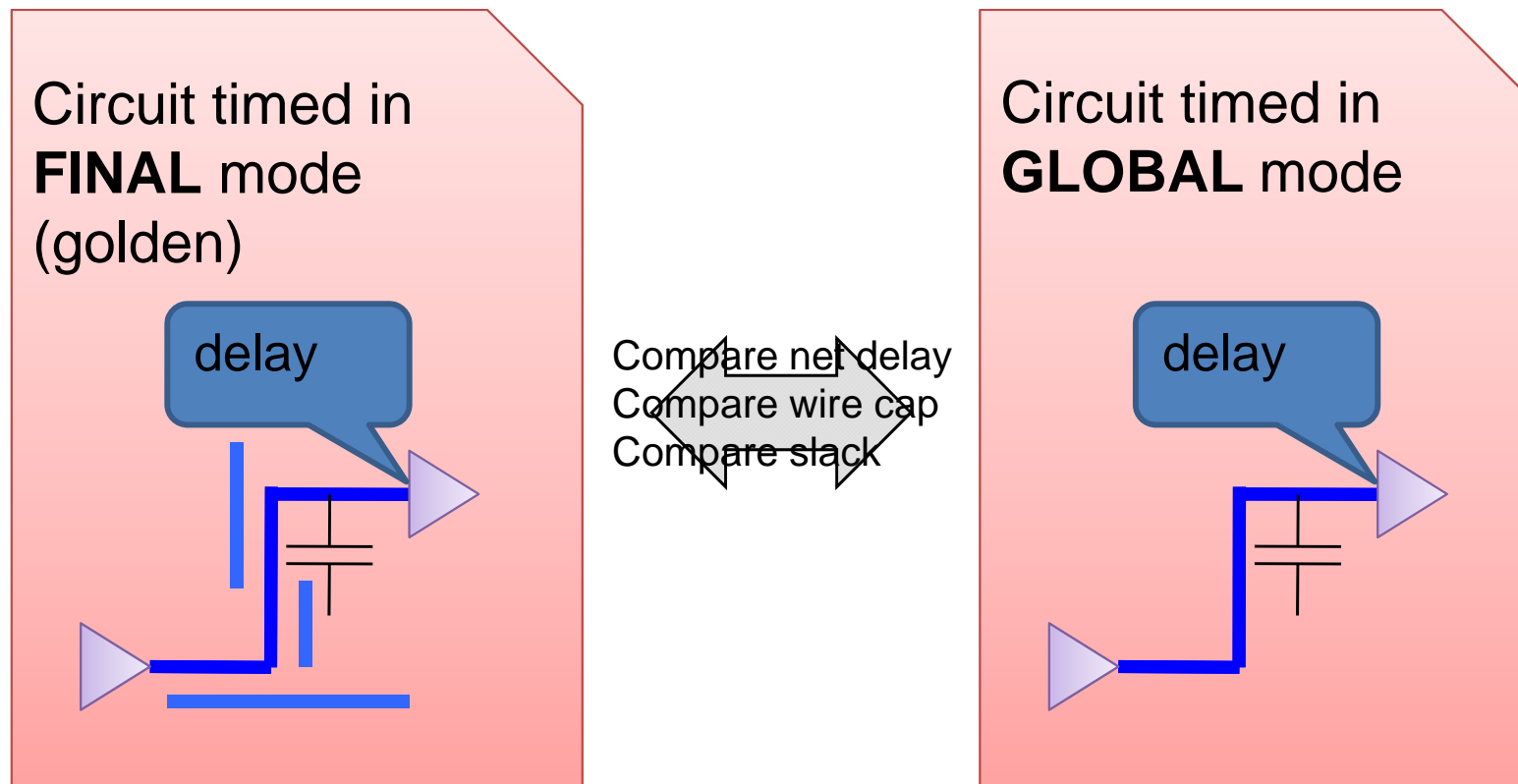
Extract glr segments
Delay calculator
Timer

GR-DR
Timing correlation?

Extract detailed wires
Delay calculator
Timer

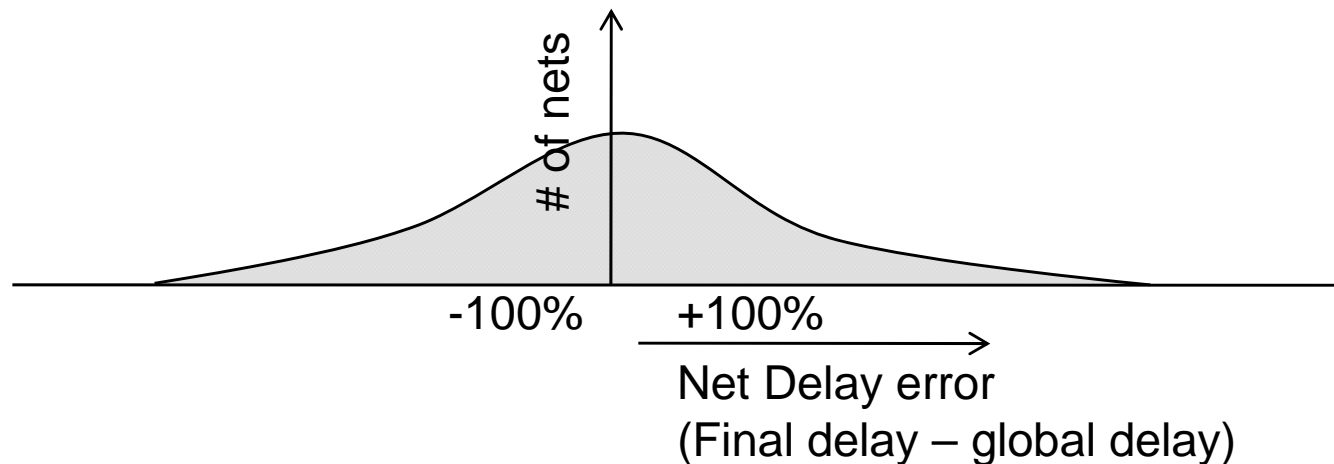
Measuring correlation error: Experimental set-up

- Take routed design:
 - Segments – time in **global** mode, CCT
 - Wires – time in **final** mode, Xtalk on = golden
- Only compare 2-pin nets, > 40um length



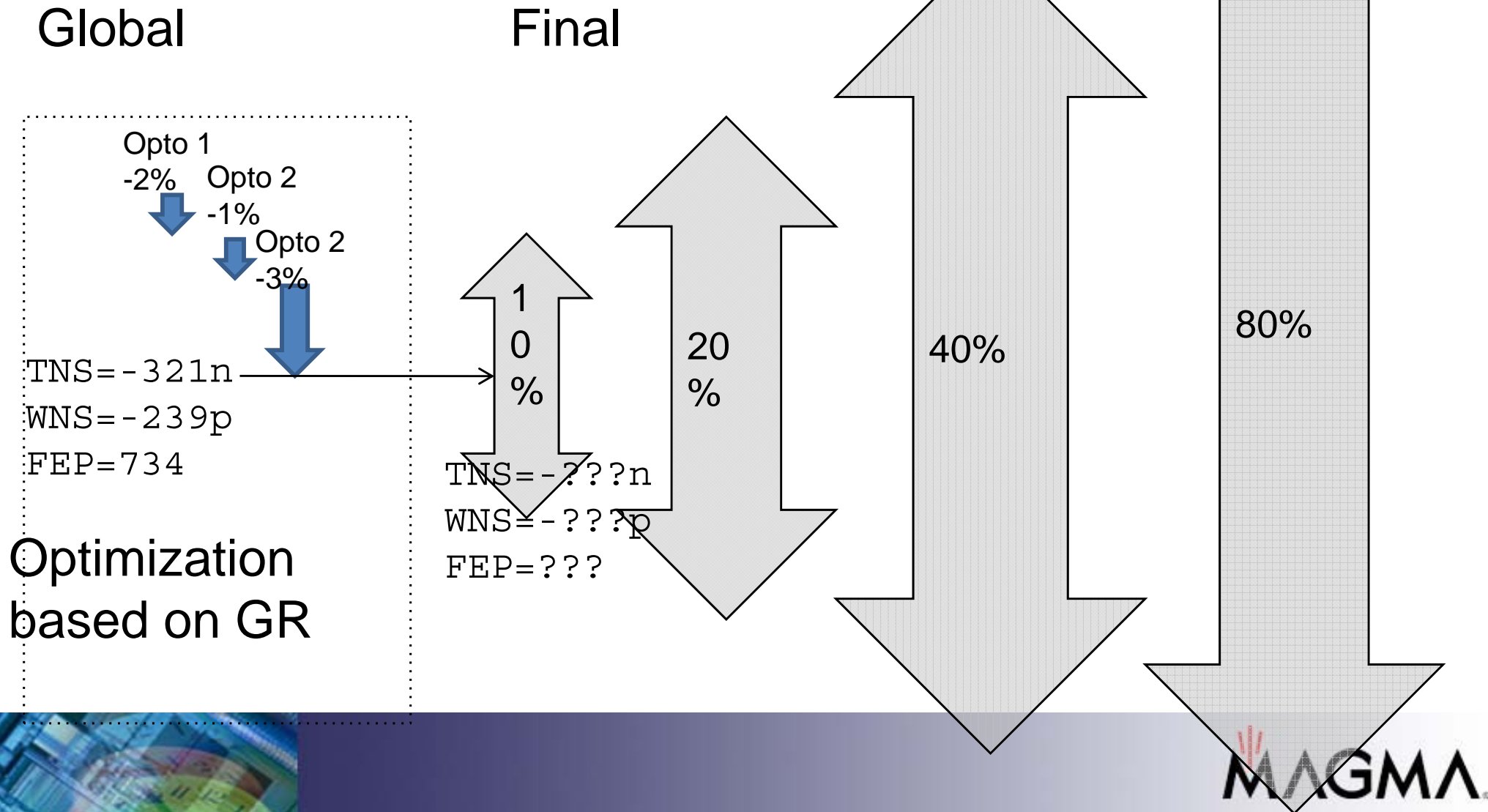
Observations on Global vs Final delay correlation

- Over 7 real designs, net delay miscorrelates badly between global and final:
 - Average = roughly OK
 - 88% standard deviation
 - So 33% of the net delays are off by more than 88%
 - 97% of nets are worse than $\pm 5\%$ accurate




Garbage in – Garbage out ?

- Modeling inaccuracies, causes earlier opto to work on the wrong parts
- Crosstalk noise could seriously randomize results.



What can we do?

- Attempt to increase accuracy of early timing:
 - Add xtalk estimate during Global Route Extraction
 - Perform track routing as well
- And/or:
- Live with the problem:
 - Spend less effort on early optimization...
 - Carefully examine statistics of optimization effectiveness
 - Have a good way to patch up xtalk at the end



“But!? But!?
I need to optimize
for *something!!*”

Building a Layout Design Flow

Observation 1:

Need gradual refinement flow using many algorithms

Observation 2:

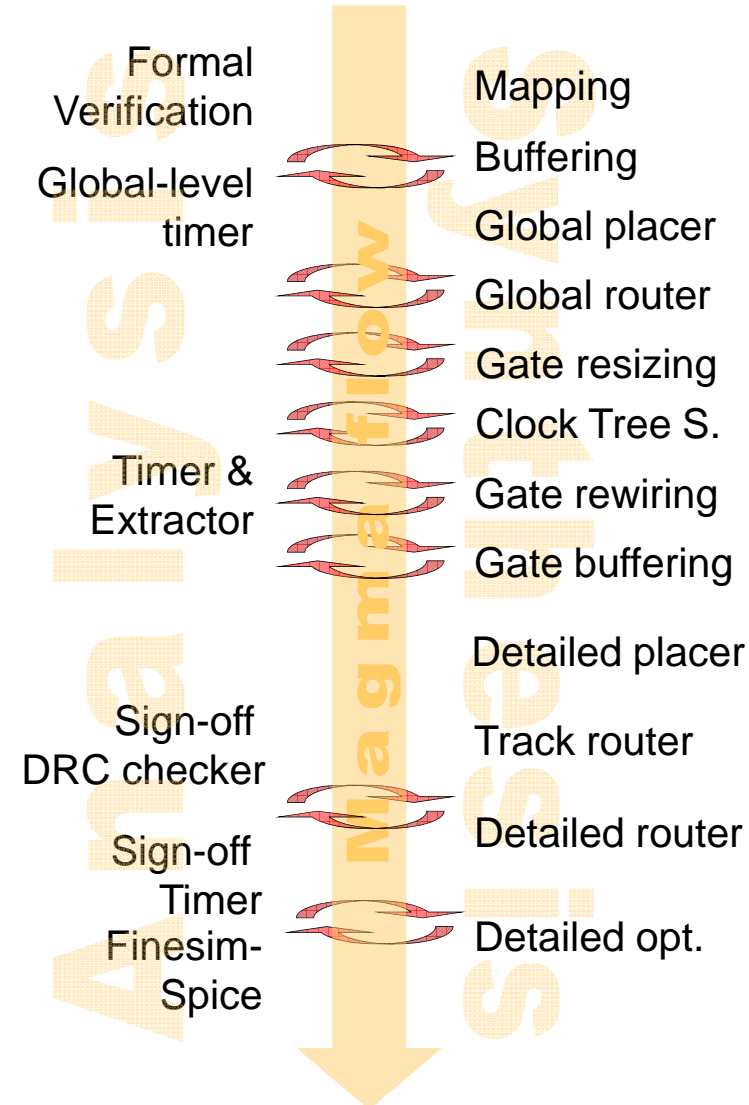
Synthesis algorithms need highly simplified models of reality

Observation 3:

Synthesis algorithms cannot deliver good multi-objective trade-offs

Observation 4:

Optimizing a single objective often makes other objectives worse.



Optimal is not Optimal!

The ABC of a solid EDA Design Flow

A: **Avoid**

Use pessimism to make problem unlikely, 'Correct by Construction'

More avoidance =
worse results...

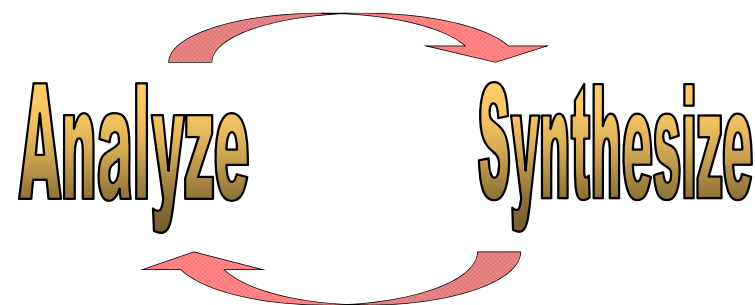
B: **Build**

Synthesize using an algorithm

Synthesis is from Mars...

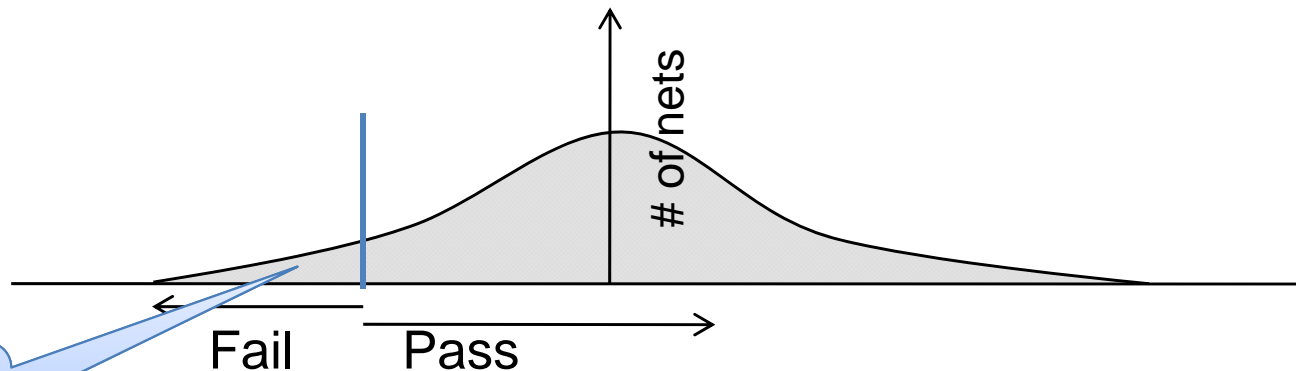
C: **Correct**

Fix each failure by incremental modifications (ECOs).



Goal: Living on the edge

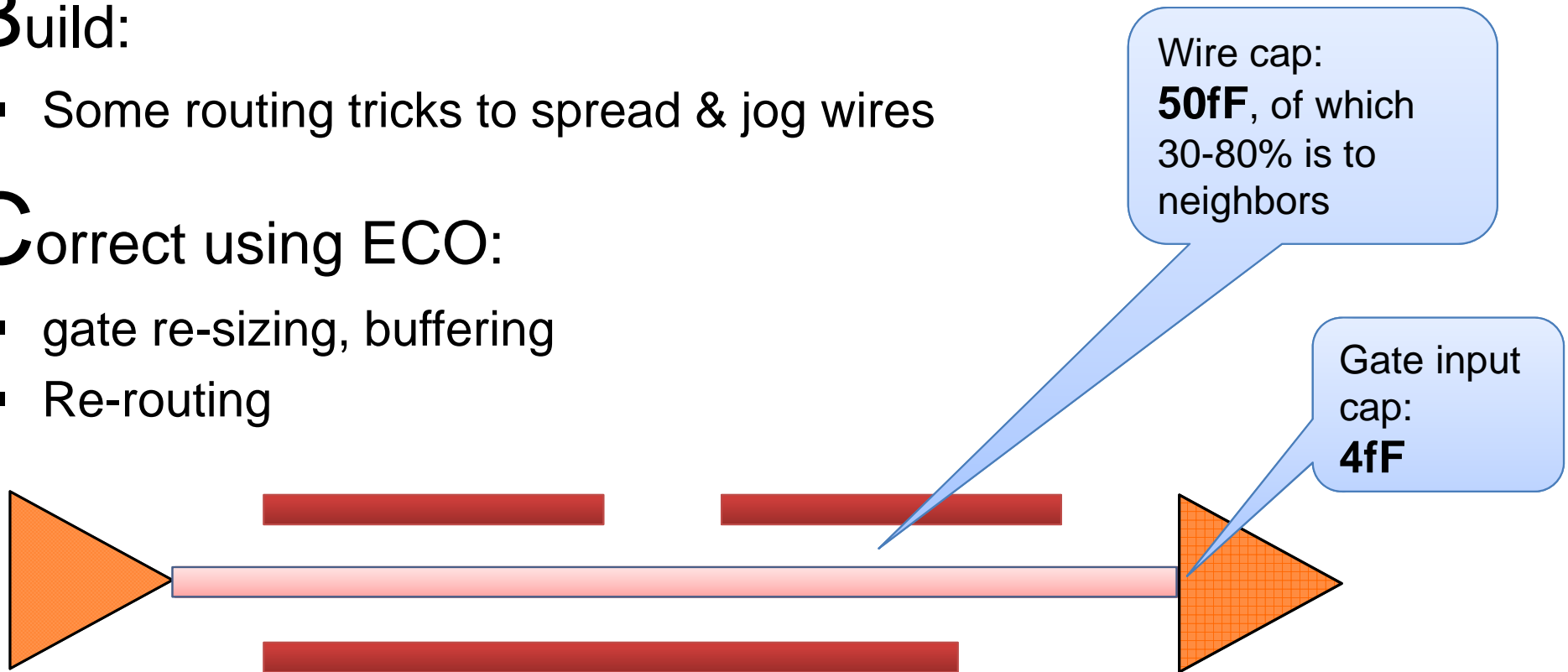
- **A**void as little as possible
- ... Such that the remaining failures can be **C**orrected incrementally
- And accept the reality that **B**uild algorithms offer little control



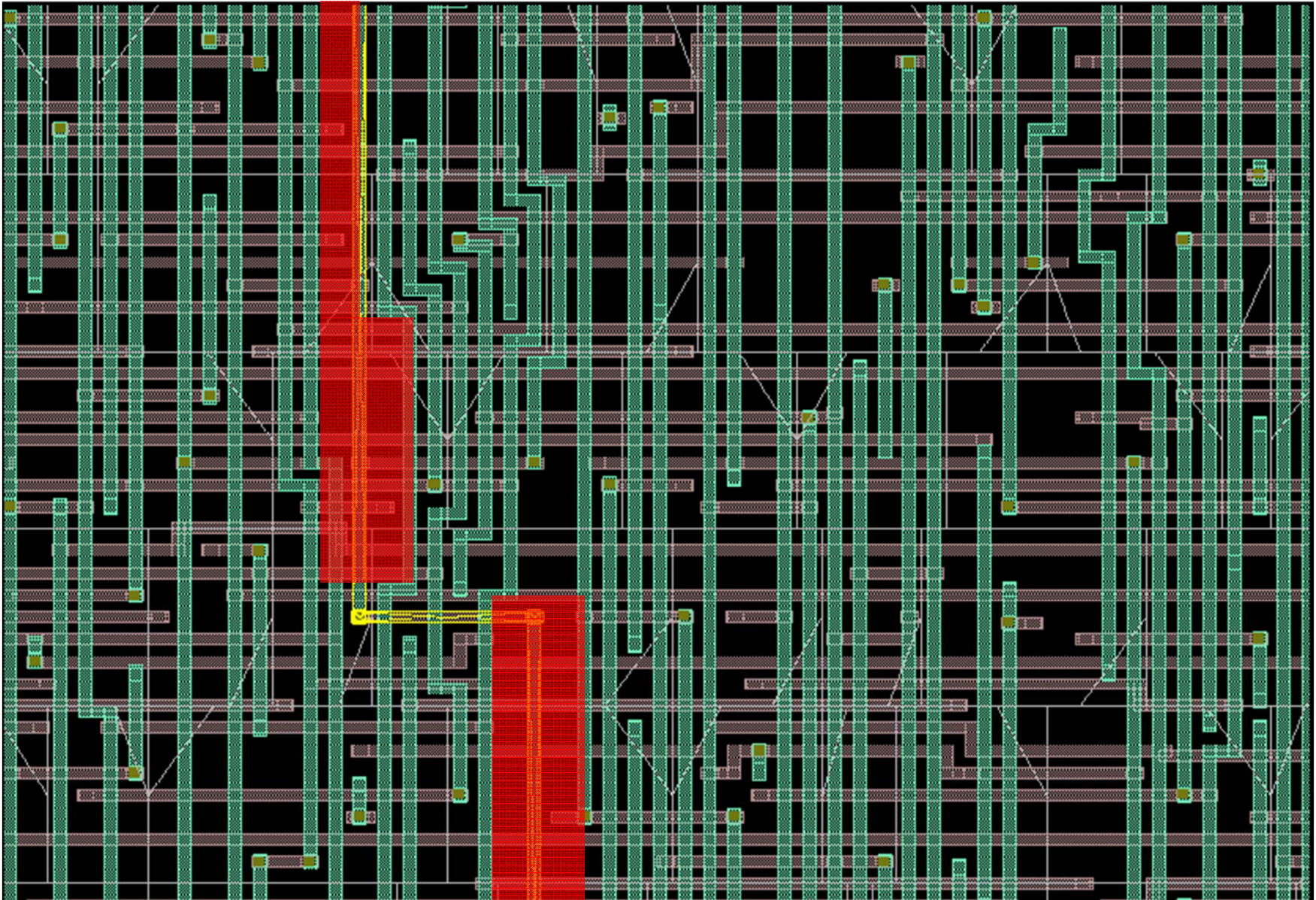
Needs
correction

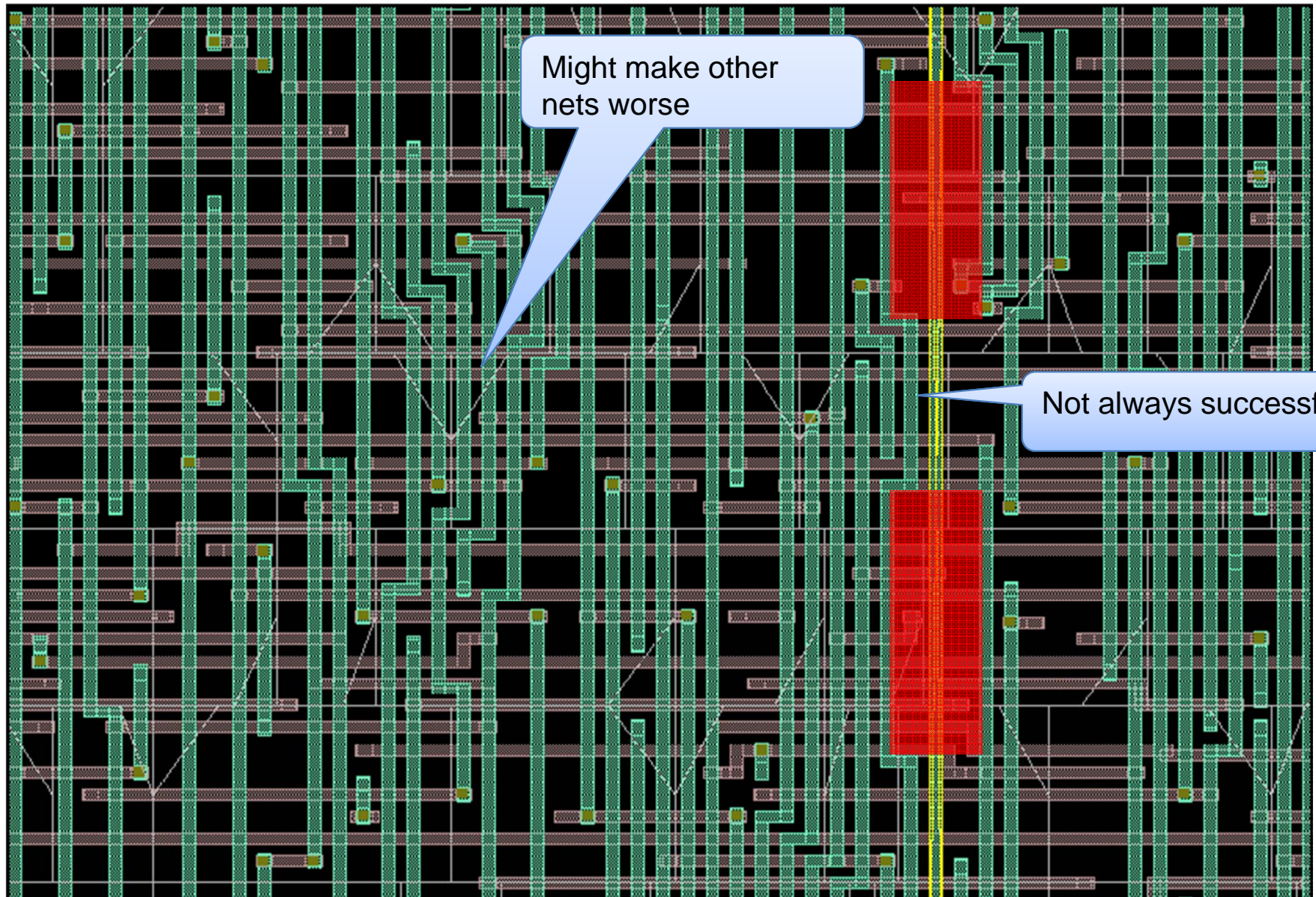
ABC in action: Combating crosstalk delay

- **A**void: using pessimism:
 - Size up all drivers: Costs cell area and power
 - Force double spacing NDR on many nets: Costs congestion = area
- **B**uild:
 - Some routing tricks to spread & jog wires
- **C**orrect using ECO:
 - gate re-sizing, buffering
 - Re-routing

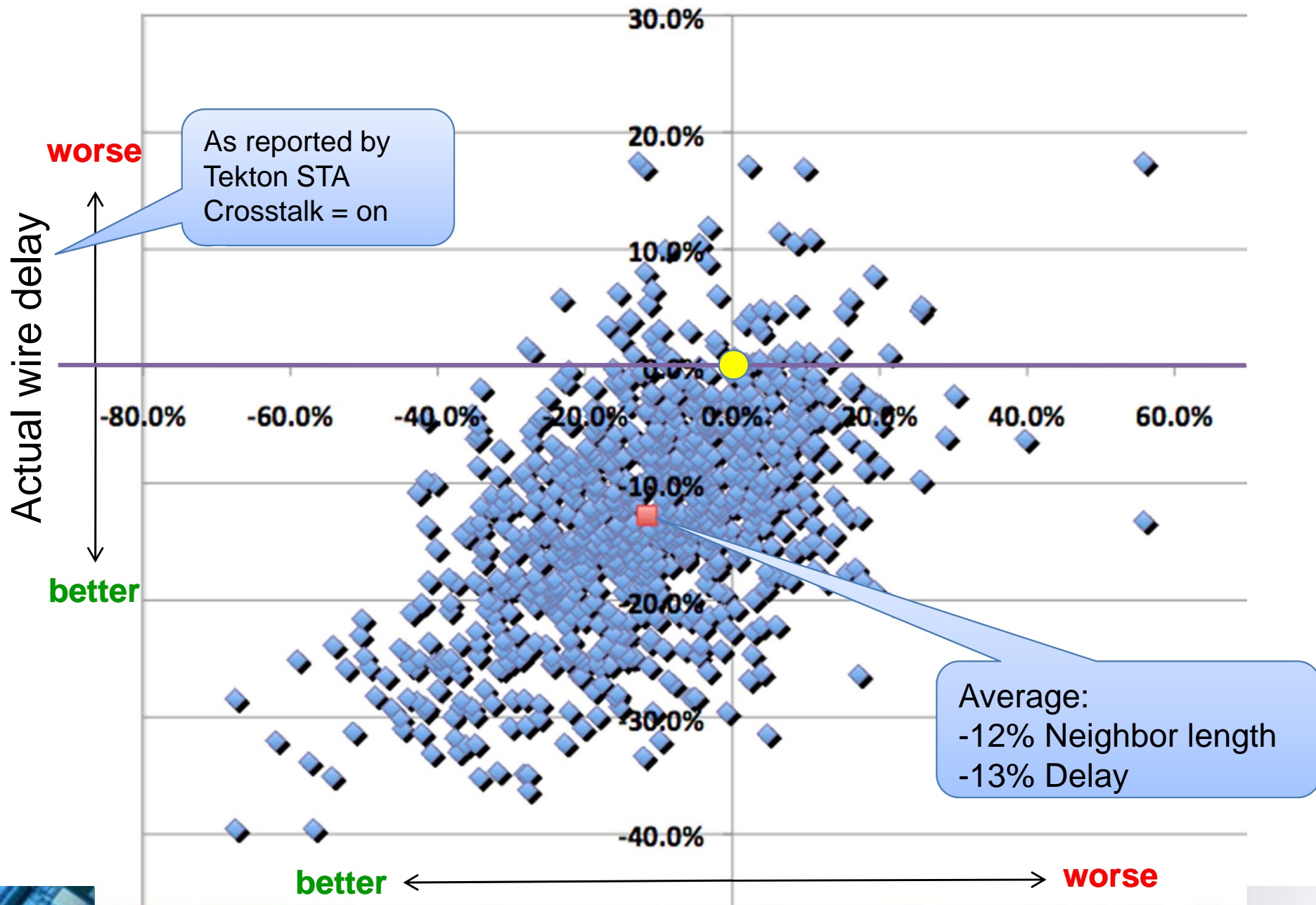


'C' routing improvement: pushing neighbors away





Effect of this layout push on timing

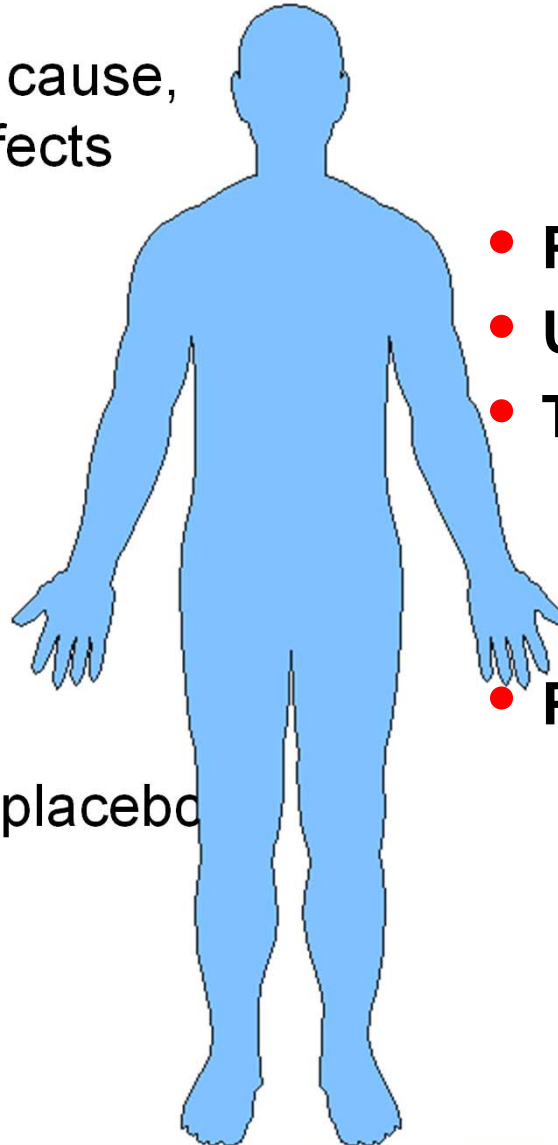


Medical tools

vs.

EDA tools

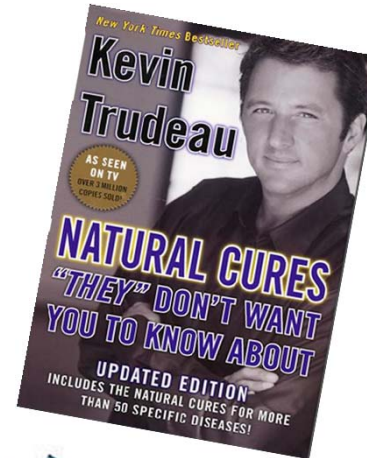
- New drug
 - Biological model of cause, actions and side-effects
- Develop it
- Test tube test
- Test on animals
 - Efficacy,
 - side effects
- Clinical trials
 - Large double-blind placebo controlled tests
- FDA-approval
- Deployment



- New Method/Algorithm
 - Based on electrical/physical plausibility
- Program it (C++/TCL)
- Unit test
- Test on small testcases
 - Debug program
 - Get a results table
- Publish at ISPD
 - Go for it!



Lack of Evidence = Quackery



EDA
is not exempt:

- Datapath placement
- Thermal-driven placement
- DFM-driven design
- Plug 'n play tool interoperability
- Hybrid GPU/CPU EDA tools.
- Gridless routing
- X-Architecture

Skeptical wisdom for Electronic Design

- “Humans are amazingly good at self-deception”
 - This looks soooo good, therefore this *must* work
- “If it has no side effects, it probably has no effects either”
 - Example: improving temperature gradients will cost timing you!
Are you really willing to pay based on the evidence?
- “Do not confuse association with causation”
 - “I took this airborne pill, and I did not get sick”
 - “I used this DFM optimizer, and the chip yields!
- “The plural of ‘anecdote’ is ‘anecdotes’, *not* ‘data’”
 - Result could be a random effect, or another side effect
 - No substitute for unbiased placebo-controlled tests
 - Only large data sets are statistically relevant



Summary: observations from practice

- Layout is a multi-objective optimization problem
 - DRC, Manufacturability, timing, power, cost, design effort
- Timing is poorly predictable early in the flow
- The only thing that counts is the result at the end
 - Intermediate data is a poor indicator
 - Need hard evidence that trade off is worthwhile
- Beware of XX-driven synthesis/place/route
 - Is the gain worth the side effects?
- Optimal is irrelevant, while greedy is pretty good
- Simple A-B-C flows are proven in practice

