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Colibri VFxx

Datasheet

Revision History

Date	Doc. Rev.	Colibri VFxx Version	Changes
08-Aug-2013	Rev. 0.9	V1.0	Initial Release: Preliminary version
24-Oct-2013	Rev. 1.0	V1.0	Official release: Minor changes
07-Jan-2014	Rev. 1.1	V1.1	Changes regarding new HW version 1.1, remove Security features from VF61 variant
05-Mar-2014	Rev. 1.2	V1.1	Update flash size of VF61
14-Mar-2014	Rev. 1.3	V1.1	Add information about compatibility of CAN interface with other Colibri modules
03-Jul-2014	Rev. 1.4	V1.1	Correction of operating temperature range of IT-Version Corrections in Table 5-27 Clarifications in the section 7 “Bootstrap Option” Minor changes
17-Nov-2014	Rev. 1.5	V1.1	Correction in section 10.2 “Recommended Operation Conditions” Correction of VF61 block diagram Section 10.7 renamed and updated Clarifications in section 5.12 “PWM” Minor changes
15-April-2015	Rev. 1.6	V1.1	Section 1.3.3 Interfaces: updated number of available GPIOs
25-Sep-2015	Rev. 1.7	V1.2	Update module version Section 5.22: change SAI clock output from EXT_AUDIO_MCLK to CKO1 Section 5.22: correction “FIF” to “FIFO”
16-Feb-2016	Rev. 1.8	V1.2	Replace Figure 7, minor changes
13-Feb-2017	Rev. 1.9	V1.2	Updated web-links (Section 1.2, 1.4 and 10.5.1) Changed heading to “Colibri Carrier Board Schematics” (Section 1.4.6) Updated remarks in the Table 5-4 (Section 5.2.1)
06-April-2017	Rev. 2.0	V1.2	Added voltage level for the I/Os in the table.
25-May-2018	Rev. 2.1	V1.2	Added typical current values (Section 10.3)
18 Apr-2019	Rev. 2.2	V1.2	Added remark to flash endurance (Section 1.3.2) Added remark to suspend (Section 8) Added GPIO pins for VF50 (Section 3.2, 4.4) Updated web-links (Section 10.5.1) Minor changes
10-May-2019	Rev. 2.3	V1.2	Removed faulty statement abut USB recovery mode (Section 5.4) Added note about baud rate limitations (Section 5.9) Changed min VCC_BATT to 2.4V (Section 10.2) Minor changes
29-May-2019	Rev. 2.4	V1.2	Added remark about back feeding for USB (Section 5.4)

1 Introduction

1.1 Hardware

The Colibri VF50 and VF61 are both SODIMM sized computer modules based on the Freescale Vybrid embedded System-on-Chip (SoC). The Vybrid SoC features a Cortex-A5 processor supporting a clock frequency of up to 500MHz. The Colibri VF61 additionally features a second Cortex-M4 processor core which can be clocked at up 167MHz maximum. This unique heterogeneous dual core system allows for running a second hard real time operating system on the M4 core for time and security critical tasks.

The module tarets a wide range of applications, including: Digital Signage, Medical Devices, Navigation, Industrial Automation, HMIs, Avionics, Entertainment System, POS, Data Acquisition, Thin Clients, Robotics, Gaming and many more.

It offers a wide range of interfaces from simple GPIOs, industry standard I2C and SPI buses through to high speed USB 2.0 interfaces. Both Colibri VFxx modules feature a Fast Ethernet PHY with IEEE1588 time stamping on the module. Additional, a second PHY can be integrated on the customer carrier board by using the RMII interface.

Existing customers will benefit from an extremely easy migration path from the current Colibri PXAxxx or Colibri T20/30 module range to the Colibri VFxx – all Colibri modules are electrically pin compatible. New customers will also appreciate the ability to select the Colibri module most suitable for their application to achieve the optimum price/performance balance without the need to support different carrier board designs.

1.2 Software

Initially, the Colibri VFxx modules are provided with an embedded Linux Image. Additionally a Windows Embedded Compact Image available. More information can be found here: http://developer.toradex.com/software/windows-embedded-compact/vf50-vf61-wec-software

For the additional Cortex-M4 processor of the Colibri VF61, Toradex provides the free and open source real-time operating system eCos. Additional information and download links can be found here: http://developer.toradex.com/knowledge-base/ecos-rtos-on-the-cortex-m4-of-a-colibri-vf61

Toradex also works with third-party partners should you require another Operating System.

1.3 Main Features Colibri VFxx

1.3.1 CPU

	Colibri VF50	Colibri VF61
Freescale Vybrid Controller	MVF50NN151CMK40	MVF61NN151CMK50
CPU Cores	1	2
ARM Cortex-A5 with TrustZone	✓	✓
ARM Cortex-M4	-	✓
Instruction Cache	32KB	32KB (A5) 16KB (M4)
L1 Cache	32KB	32KB (A5) 16KB (M4)
L2 Cache	-	512KB (A5)
NEON	✓	✓
VFPv4 floating point unit	✓	✓
Maximum CPU frequency	400MHz	500MHz (A5) 167 MHz (M4)
Secure High Assurance Boot	-	-
AES, DES/3DES, SHA-1, SHA-224, SHA-256	-	-
Tamper Detection	-	-
Run-time Integrity Checker and Security Controller	-	-
Random Number Generator (NIST SP 800-90)	-	-
Secure JTAG Controller (with electrical fuses)	-	-
Secure real-time clock	-	-
Universal Unique ID	-	-

1.3.2 Memory

	Colibri VF50	Colibri VF61
DDR3 RAM (16 bit mode, no ECC)*	128MB	256MB
DDR3 RAM (8 bit mode, ECC enabled)*	64MB	128MB
On-chip SRAM	1.5MB (512KB with ECC)	1.0MB (512KB with ECC)
NAND Flash (8Bit)	128MB	512MB

*The DDR3 RAM can be software configured to be used either in 16bit mode without ECC or in 8bit mode with ECC. Flash write endurance is limited. Extensive writing to the memory can wear out the memory cell. Software wear levelling makes sure the cells are getting worn out evenly. More information can be found here http://developer.toradex.com/knowledge-base/flash-memory and here https://en.wikipedia.org/wiki/Flash_memory#Write_endurance.

1.3.3 Interfaces

	Colibri VF50	Colibri VF61
LCD RGB 24bpp (1024x768 maximum resolution)	✓	✓
Resistive Touch Screen 4 Wire	✓	✓
Resistive Touch Screen 5 Wire	-	-
Audio I/O	-	✓
ADC 12bit	4+12*	4+8*
DAC 12bit	2*	-
Camera Interface (10bit)	✓	✓
I2C	1+3*	1+3*
SPI	1+3*	1+3*
UART	3+2*	3+2*
SD/SDIO/MMC (4bit)	1+1*	1+1*
GPIO	Up to 103	Up to 99
USB 2.0 High Speed OTG (host/device)	✓	✓
USB 2.0 High Speed Host	✓	✓
10/100 Mbit/s Ethernet with auto MDI/MDI-X and IEEE1588	✓	✓
RMII interface for 2nd Ethernet PHY on Baseboard with L2 Switch	✓*	✓*
PWM	4+13*	4+13*
S/PDIF In	✓*	✓*
S/PDIF Out	✓*	✓*
Enhanced Serial Audio Interface (I2S, AC97 compatible)	✓*	✓*
CAN	2*	2*
Reference Clock Output	1+1*	1+1*
QuadSPI	2*	2*
Analogue Video ADC inputs (PAL/NTSC)	-	4*
Anti-Tamper Protection Signals	-	-

*These interfaces are available on pins that are not compatible within the Colibri family. There are restrictions to using different interfaces simultaneously, please check the available alternative functions of the Vybrid pins.

1.3.4 Supported Operating Systems

	Colibri VF50	Colibri VF61
Embedded Linux	✓	✓
Windows CE6.0	✓	✓
Android (contact Toradex)	✓	✓
eCos RTOS (M4 Processor)	-	✓
Freescale MQX RTOS (M4 Processor)	-	✓

1.4 Reference Documents

1.4.1 Freescale Vybrid Controller

You will find more details about the Vybrid chip in the Datasheet and Technical Reference Manual provided by NXP:
http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/vfxxx-controller:VYBRID

1.4.2 Ethernet Physical Layer Transceiver

Colibri VFxx uses the Microchip KSZ8041NL Ethernet PHY:
http://www.microchip.com/wwwproducts/en/KSZ8041

1.4.3 Audio Codec and Touch Screen Controller (only on Colibri VF61)

Colibri VF61 uses the Cirrus Logic WM9715L Audio Controller:
https://www.cirrus.com/products/wm9715/

1.4.4 Toradex Migration Guide

This document provides additional information about pin usage and describes the functional compatibility with the rest of the Colibri family. Please study this document in detail prior to starting your carrier board design.
http://docs.toradex.com/100188-colibri-migration-and-design-guide.pdf
http://developer.toradex.com/carrier-board-design

1.4.5 Toradex Developer Center

There is additional information in the Toradex Developer Center, which is regularly updated with the latest product support information.
Please note that the Developer Center is common for all Toradex products. You should always check to ensure if information is valid or relevant for the Colibri VFxx.
http://www.developer.toradex.com

1.4.6 Colibri Carrier Board Schematics

We provide the complete schematics and the Altium project file which includes library symbols and IPC-7351 compliant footprints for the Colibri Evaluation Board and other Carrier Boards free of charge. This is a great help when designing your own Carrier Board.
http://developer.toradex.com/carrier-board-design/reference-designs

2 Architecture Overview

2.1 Block Diagram Colibri VF61

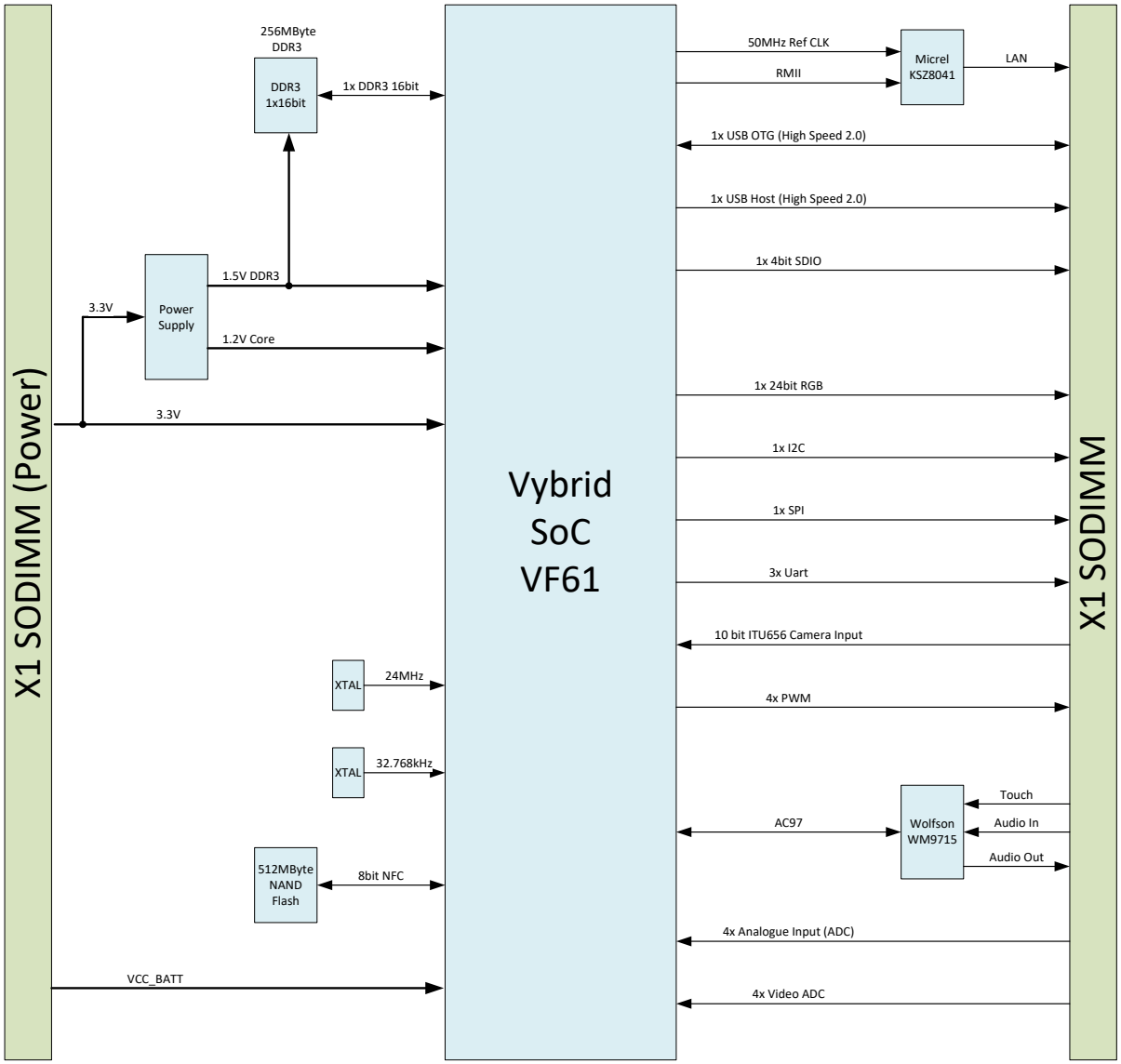

Figure 1 Colibri VF61 Block Diagram

2.2 Block Diagram Colibri VF50

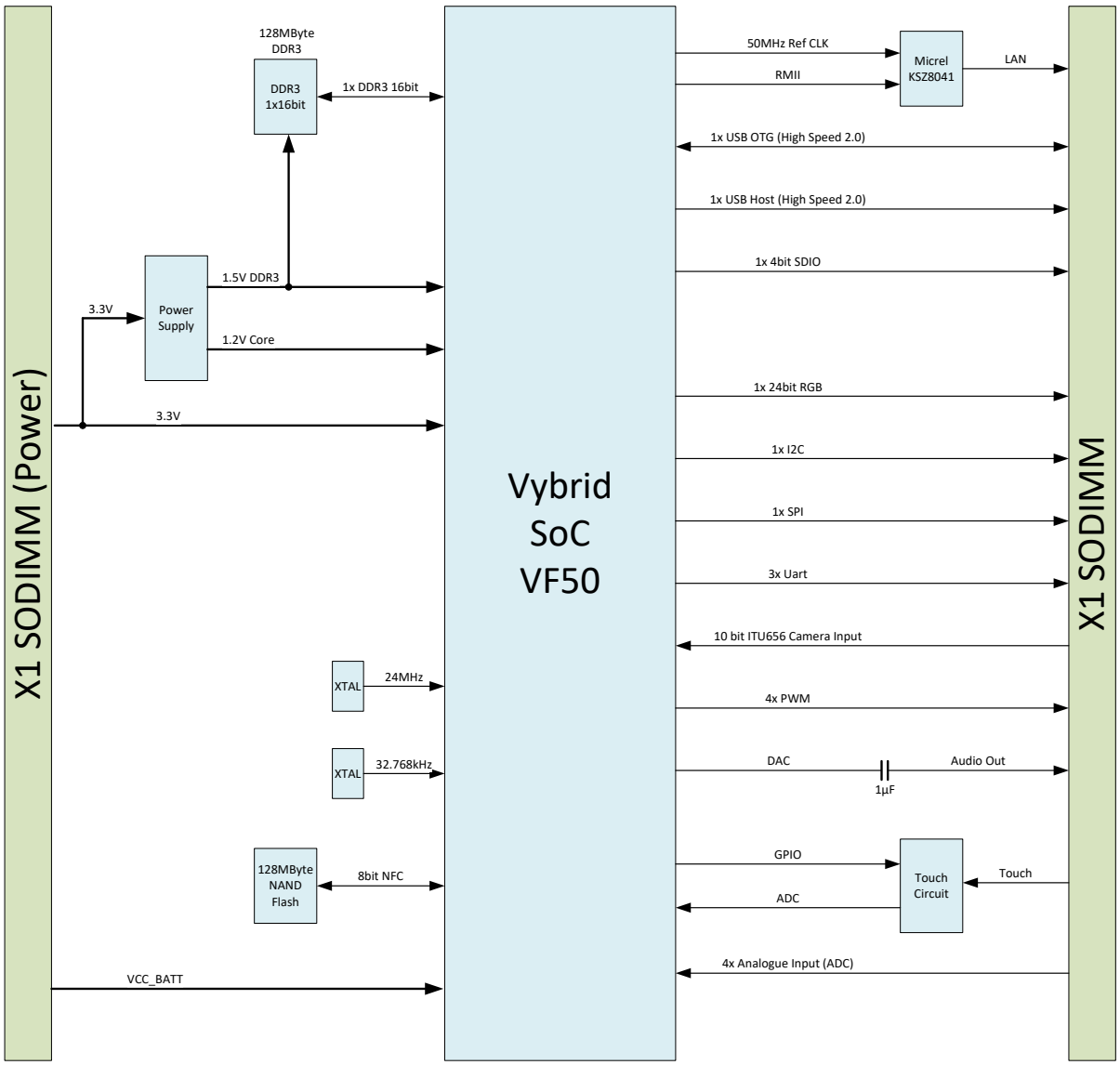

Figure 2 Colibri VF50 Block Diagram

3 Colibri VFxx SODIMM Connector

3.1 Physical Location

Colibri VFxx modules are equipped with a 200 Pin SODIMM edge connector (X1). Some of the edge connector fingers are missing because they are not connected to any signal on the module. In order to be compatible with the pin numbering of the Colibri family, these pin numbers are maintained. The figure below shows these pin positions and numbers.

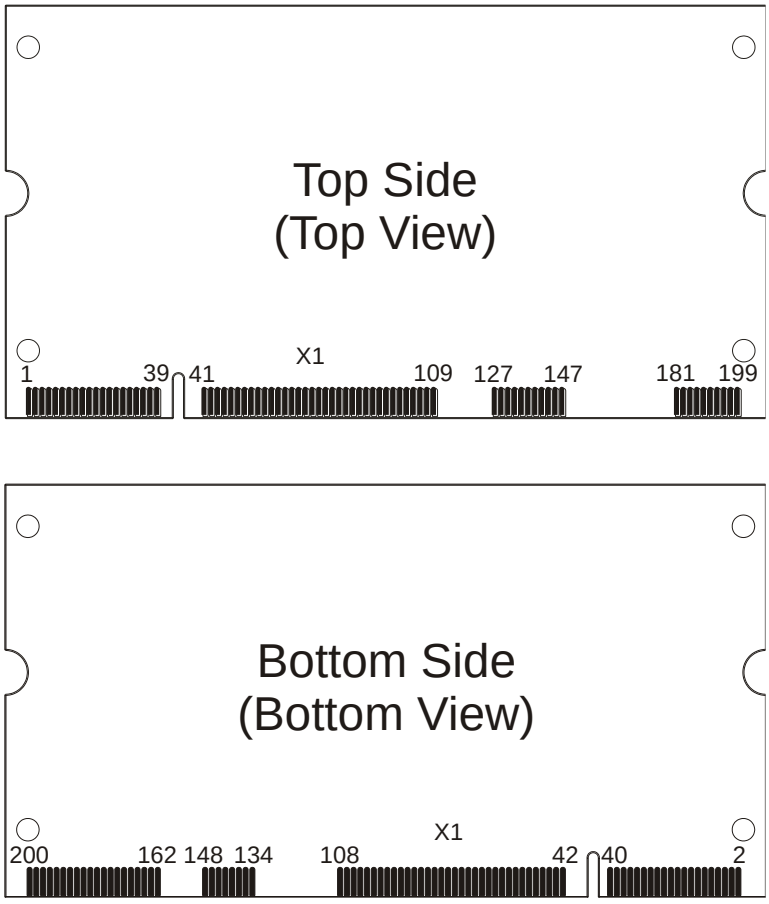

Figure 3 Location and pin numbering of SODIMM edge connector

3.2 Pin Assignment

The table below details the SODIMM 200 way connector pin functionality.

It should be noted that some of the pins are multiplexed; there is more than one Vybrid pin connected to one SODIMM or FFC pin. For example, PTB9 and PTC6 are both assigned to SODIMM pin 67. Care should be taken to ensure that multiplexed pins are tri-stated when they are not being used (e.g., if Vybrid pin A and pin B are tied to SODIMM pin 1, then if you are driving Vybrid pin A, then pin B should be tri-stated). Additional information can be found in chapter 4.1: Function Multiplexing.
Some of the SODIMM pins are not connected to anything on the module. The finger pads of these pins are not present on the modules.

- X1 Pin: Pin number on the SODIMM connector (X1).
- Compatible function: The default function which is compatible with all Colibri modules. IMPORTANT: There are some limitations. You can find more information about pin compatibility in the "**Colibri Migration Guide**".
- VFxx CPU Pin: The name of the pin of the Vybrid chip. This is also the name of the GPIO function which is available on this pin
- Non VFxx CPU Pins: Peripheral functions which are not directly provided by the Vybrid chip.
- Note: Additional information. Some pins are noted as "only GPIO". These pins can provide only the GPIO functionality, not the Colibri compatible function. Some of the Colibri compatible functions might be emulated by programmably manipulating the GPIO.

Table 3-1 X1 Connector

X1 Pin	Compatible Function	VFxx CPU Pin	Non VFxx CPU Pins	Note
1	Audio Analogue Microphone Input		MIC_IN	Colibri VF61 only, not available on Colibri VF50
3	Audio Analogue Microphone GND		MIC_GND	Colibri VF61 only, not available on Colibri VF50
5	Audio Analogue Line-In Left		LINEIN_L	Colibri VF61 only, not available on Colibri VF50
7	Audio Analogue Line-In Right		LINEIN_R	Colibri VF61 only, not available on Colibri VF50
9	Audio_Analogue GND		VSS_AUDIO	Colibri VF61 only, not available on Colibri VF50
11	Audio_Analogue GND		VSS_AUDIO	Colibri VF61 only, not available on Colibri VF50
13	Audio Analogue Headphone GND		HEADPHONE_GND	Colibri VF61 only, Colibri VF50: VSS_AUDIO
15	Audio Analogue Headphone Left		HEADPHONE_L	Colibri VF61 only, Colibri VF50: DACO0
17	Audio Analogue Headphone Right		HEADPHONE_R	Colibri VF61 only, Colibri VF50: DACO1
19	UART_C RXD	PTB5		
21	UART_C TXD	PTB4		
23	UART_A DTR	PTA20		only GPIO
25	UART_A CTS, Keypad_In<0>	PTB13		
27	UART_A RTS	PTB12		
29	UART_A DSR	PTA31		only GPIO
31	UART_A DCD	PTA21		only GPIO
33	UART_A RXD	PTB11		
35	UART_A TXD	PTB10		
37	UART_A RI, Keypad_In<4>	PTA30		only GPIO
39	GND		GND	
41	GND		GND	
43	WAKEUP Source<0>, SDCard CardDetect	PTB20		
45	GPIO	PTB19		only GPIO
47	SDCard CLK	PTA24		
49	SDCard DAT<1>	PTA27		
51	SDCard DAT<2>	PTA28		

X1 Pin	Compatible Function	VFxx CPU Pin	Non VFxx CPU Pins	Note
53	SDCard DAT<3>	PTA29		
55	GPIO	PTB17		only GPIO
57	LCD RGB Data<16>	PTE11		
59	PWM<A>, Camera Input Data<7>	PTB0 PTC7		Multiplexed (Two Vybrid Pins)
61	LCD RGB Data<17>	PTE12		
63	GPIO	PTB16		only GPIO
65	Camera Input Data<9>, Keypad_Out<3>	PTB18		
67	PWM<D>, Camera Input Data<6>	PTB9 PTC6		Multiplexed (Two Vybrid Pins)
69	GPIO	PTD30		only GPIO
71	Camera Input Data<0>, LCD Back-Light GPIO	PTC0		
73	GPIO	PTB21		only GPIO
75	GPIO	PTD12		only GPIO
77	GPIO	PTB22		only GPIO
79	Camera Input Data<4>	PTC4		
81	Camera Input VSYNC	PTB7		
83	GND		GND	
85	Camera Input Data<8>, Keypad_Out<4>	PTC8		
87	nReset Out	RESETB/RESET_OUT		Not GPIO capable
89	GPIO	JTDI		GPIO Pin PTA9
91	Recovery Mode		Recovery glue logic	Pull to GND for entering the Serial loader
93	GPIO	PTB28		only GPIO
95	GPIO	PTC30		only GPIO
97	Camera Input Data<5>	PTC5		
99	GPIO	PTD29		only GPIO
101	Camera Input Data<2>	PTC2		
103	Camera Input Data<3>	PTC3		
105	GPIO	PTB26		only GPIO
107	GPIO	PTD27		only GPIO
109	GND		GND	
111			no connection	
113			no connection	
115			no connection	
117			no connection	
119			no connection	
121			no connection	
123			no connection	
125			no connection	
127	GPIO	PTD26		only GPIO
129	USB Host Power Enable	PTD4		only GPIO

X1 Pin	Compatible Function	VFxx CPU Pin	Non VFxx CPU Pins	Note
131	Usb Host Over-Current Detect	PTE3		only GPIO
133	GPIO	PTD9		only GPIO
135	GPIO	PTD10		only GPIO
137	USB Client Cable Detect	PTC29 USB0_VBUS_DETECT		Multiplexed (Two Vybrid Pins)
139	USB Host DP	USB1_DP		
141	USB Host DM	USB1_DM		
143	USB Client DP	USB0_DP		
145	USB Client DM	USB0_DM		
147	GND		GND	
149			no connection	
151			no connection	
153			no connection	
155			no connection	
157			no connection	
159			no connection	
161			no connection	
163			no connection	
165			no connection	
167			no connection	
169			no connection	
171			no connection	
173			no connection	
175			no connection	
177			no connection	
179			no connection	
181	GND		GND	
183	Ethernet Link/Activity Status		LINK_AKT	
185	Ethernet Speed Status		SPEED100	
187	Ethernet TXO-		TXO-	
189	Ethernet TXO+		TXO+	
191	Ethernet GND		AGND_LAN	
193	Ethernet RXI-		RXI-	
195	Ethernet RXI+		RXI+	
197	GND		GND	
199	GND		GND	
2	Analogue Input<3>	ADC1SE9		
4	Analogue Input<2>	ADC0SE9		
6	Analogue Input <1>	ADC1SE8		
8	Analogue Input <0>	ADC0SE8		
10	Audio_Analogue VDD		AVDD_AUDIO	
12	Audio_Analogue VDD		AVDD_AUDIO	

X1 Pin	Compatible Function	VFxx CPU Pin	Non VFxx CPU Pins	Note
14	Resistive Touch PX	PTA19	TSPX	CPU Pin only available on VF50
16	Resistive Touch MX	PTA18	TSMX	CPU Pin only available on VF50
18	Resistive Touch PY	PTA16	TSPY	CPU Pin only available on VF50
20	Resistive Touch MY	PTB2	TSMY	CPU Pin only available on VF50
22		PTC31		
24	Battery Fault Detect	PTB3		
26	nReset In	RESETB/RESET_OUT		Not GPIO capable
28	PWM<B>	PTB8		
30	PWM<C>	PTB1		
32	UART_B CTS	PTD3		
34	UART_B RTS	PTD2		
36	UART_B RXD	PTD1		
38	UART_B TXD	PTD0		
40	VCC_BATT		VCC_BATT	
42	3V3		3V3	
44	LCD RGB DE	PTE4		
46	LCD RGB Data<7>	PTE16		
48	LCD RGB Data<9>	PTE18		
50	LCD RGB Data<11>	PTE20		
52	LCD RGB Data<12>	PTE7		
54	LCD RGB Data<13>	PTE8		
56	LCD RGB PCLK	PTE2		
58	LCD RGB Data<3>	PTE26		
60	LCD RGB Data<2>	PTE25		
62	LCD RGB Data<8>	PTE17		
64	LCD RGB Data<15>	PTE10		
66	LCD RGB Data<14>	PTE9		
68	LCD RGB HSYNC	PTE0		Do not pull up these signals during power up (strapping) see information in section 7
70	LCD RGB Data<1>	PTE24		
72	LCD RGB Data<5>	PTE28		
74	LCD RGB Data<10>	PTE19		
76	LCD RGB Data<0>	PTE23		
78	LCD RGB Data<4>	PTE27		
80	LCD RGB Data<6>	PTE15		
82	LCD RGB VSYNC	PTE1		Do not pull up these signals during power up (strapping) see information in section 7
84	3V3		3V3	
86	SPI CS	PTD5		
88	SPI CLK	PTD8		

X1 Pin	Compatible Function	VFxx CPU Pin	Non VFxx CPU Pins	Note
90	SPI RXD	PTD6		
92	SPI TXD	PTD7		
94	Camera Input HSYNC	PTB6		
96	Camera Input PCLK	PTA7		
98	Camera Input Data<1>	PTC1		
100	Keypad_Out<1>	PTD13		only GPIO
102	GPIO	PTA12		only GPIO
104	GPIO	PTD28		only GPIO
106	GPIO	PTD31		only GPIO
108	3V3		3V3	
110			no connection	
112			no connection	
114			no connection	
116			no connection	
118			no connection	
120			no connection	
122			no connection	
124			no connection	
126			no connection	
128			no connection	
130			no connection	
132			no connection	
134	GPIO	PTA17		only GPIO
136	GPIO	PTE21		LCD RGB Data<18>, compatible with Colibri Txx
138	GPIO	PTE22		LCD RGB Data<19>, compatible with Colibri Txx
140	GPIO	PTE13		LCD RGB Data<20>, compatible with Colibri Txx
142	GPIO	PTE14		LCD RGB Data<21>, compatible with Colibri Txx
144	GPIO	PTE5		LCD RGB Data<22>, compatible with Colibri Txx
146	GPIO	PTE6		LCD RGB Data<23>, compatible with Colibri Txx
148	3V3		3V3	
150			no connection	
152			no connection	
154			no connection	
156			no connection	
158			no connection	
160			no connection	
162		VADCSE0		Analog Video Input (Colibri VF61 only)
164		VADCSE1		Analog Video Input (Colibri VF61 only)

X1 Pin	Compatible Function	VFxx CPU Pin	Non VFxx CPU Pins	Note
166		VADCSE2		Analog Video Input (Colibri VF61 only)
168		VADCSE3		Analog Video Input (Colibri VF61 only)
170		EXT_TAMPER0		Security Feature (not supported)
172		EXT_TAMPER1		Security Feature (not supported)
174		EXT_TAMPER2/EXT_WM0_TAMPER_IN		Security Feature (not supported)
176		EXT_TAMPER3/EXT_WM0_TAMPER_OUT		Security Feature (not supported)
178		EXT_TAMPER4/EXT_WM1_TAMPER_IN		Security Feature (not supported)
180		EXT_TAMPER5/EXT_WM1_TAMPER_OUT		Security Feature (not supported)
182	3V3		3V3	
184	GPIO	PTD25		only GPIO
186	GPIO	PTD24		only GPIO
188	GPIO	PTD11		only GPIO
190	SDCard CMD	PTA25		
192	SDCard DAT<0>	PTA26		
194	I2C SDA	PTB15		
196	I2C SCL	PTB14		
198	3V3		3V3	
200	3V3		3V3	

4 I/O Pins

4.1 Function Multiplexing

The Freescale Vybrid SoC I/O pins can be configured in any of up to eight alternate functions. Most of the pins can also be used as "normal" GPIOs (General Purpose I/O, sometimes also referred to as Digital I/O). For example the Vybrid signal pin on the SODIMM finger pin 19 has the primary function SCI1_RX (Colibri standard function UART_C_RXD), but can also provide the following alternative functions: PTB5 (GPIO), FTM0_CH5 (PWM output), ADC1_SE4 (ADC input), LCD39 (LCD output), VIU_DE (Camera input), VIU_DATA23 (Camera Input) or QSPI1_A_DQS (QSPI interface).

The default setting for this pin is the primary function SCI1_RX. It is strongly recommended to, whenever possible, use a pin for a function which is compatible with all Colibri modules. This guarantees the best compatibility with the standard software and with the other modules in the Colibri family.

Some of the alternative functions are available on more than one pin. For example the SCI1_CTS function is available at the SODIMM pins 81, 97 and 105. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behaviour.

In some cases, the available alternative functions of certain pins on the Vybrid SoC are constrained; to allow maximum flexibility, some of these pins are paired and share the same SODIMM pin. As previously mentioned, ensure that the unused pin in the pair is tri-stated to avoid undesired behaviour and/or hardware damage.

The following X1 connector pins are connected to more than one Vybrid pin:

Table 4-1 Colibri Multiplexed Pins

X1 Pin #	Vybrid Pin 1	Vybrid Pin 2	Remarks
59	PTB0	PTC7	PWM and Camera input are both Colibri standard functions
67	PTB9	PTC6	PWM and Camera input are both Colibri standard functions
137	PTC29	USB0_VBUS_DETECT	USB0_VBUS_DETECT is not GPIO capable

The RESETB/RESET_OUT pin of the Vybrid SoC is the reset input to the processor as well as a reset output from the SoC. Since the other computer modules in the Colibri family feature separate reset input (SODIMM Pin 26 nRESET_EXT) and output (SODIMM Pin 87 nRESET_OUT) pins, the RESETB/RESET_OUT signal is routed to both SODIMM pins with the circuit shown in Figure 4.

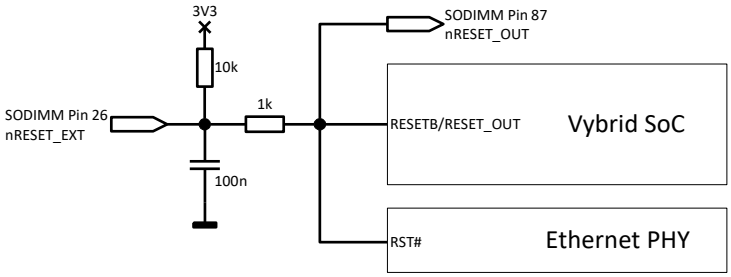

Figure 4 Reset Circuit

4.2 Pin Control

The alternative function of each pin can be changed independently. Every pin has a Software MUX Pad Control Register in which the following settings can be set (some settings might be not available on certain pins). The Register is called IOMUXC_x where x is the name of the Vybrid pin. More information about the available register settings can be found in the Vybrid Reference Manual.

Table 4-2 Software Mux Pad Control Registor

Bit	Field	Description	Remarks
31-23	Reserved		
22-20	MUX_MODE	000 Select mux mode: ALT0 mux port (GPIO) 001 Select mux mode: ALT1 mux port 010 Select mux mode: ALT2 mux port 011 Select mux mode: ALT3 mux port 100 Select mux mode: ALT4 mux port 101 Select mux mode: ALT5 mux port 110 Select mux mode: ALT6 mux port 111 Select mux mode: ALT7 mux port:	Check chapter 4.1 for the available alternative function of the pin
19-14	Reserved		
13-12	SPEED	00 Low (50 MHz) 01 Medium (100 MHz) 10 Medium (100 MHz) 11 High (200 MHz)	
11	SRE	0 Slow Slew Rate 1 Fast Slew Rate	Use slow slew rate if possible for reducing EMC problems
10	ODE	0 Output is CMOS 1 Output is open drain	
9	HYS	0 CMOS input 1 Schmitt trigger input	
8-6	DSE	000 output driver disabled 001 150 Ohm (240 Ohm if pad is DDR) 010 75 Ohm (120 Ohm if pad is DDR) 011 50 Ohm (80 Ohm if pad is DDR) 100 37 Ohm (60 Ohm if pad is DDR) 101 30 Ohm (48 Ohm if pad is DDR) 110 25 Ohm 111 20 Ohm (34 Ohm if pad is DDR)	If possible decrease the drive strength by increasing the resistance in order to reduce EMC problems
5-4	PUS	00 100 kOhm Pull Down 01 47 kOhm Pull Up 10 100 kOhm Pull Up 11 22 kOhm Pull Up	
3	PKE	0 Pull/Keeper Disabled 1 Pull/Keeper Enabled	Enable keeper or pull up/down function
2	PUE	0 Keeper enable 1 Pull enable	Selection between keeper and pull up/down function
1	OBE	0 Output buffer disabled 1 Output buffer enabled	Set to 0 if pin is used as input (default value)
0	IBE	0 Input buffer disabled 1 Input buffer enabled	

4.3 Pin Reset Status

After a reset, all GPIO compatible Vybrid pins that are available at the SODIMM connector are configured to have the output buffer disabled (OBE = 0) and the internal pull up/down resistors disabled (PKE = 0). This means all the pins are initially in high-Z state. As soon as the bootloader is running, it is possible to reconfigure the pins and their states.

4.4 List Functions

Below is a list of all the Vybrid pins which are available on the SODIMM connector X1. It shows what alternative functions are available for each pin. The GPIO functionality is located always as the ALT0 function. The default functions for compatibility with other Colibri modules types are highlighted.

Function Short Forms

SCI:	Serial Communications Interface (Universal Asynchronous Receiver/Transmitter)
VUI:	Video Interface Unit (Camera Interface)
SPDIF:	S/PDIF (Sony-Philips Digital Interface I/O)
SDIO:	Secure Card I/O (SD, MMC, CE-ATA, eMMC)
SDHC:	Secure Digital Memory Card High Capacity (SD, MMC, CE-ATA, eMMC)
SPI:	Serial Peripheral Interface Bus
QSPI:	Quad Serial Peripheral Interface Bus
FB:	FlexBus, external bus (only partial usable)
DCU:	Display Control Unit, parallel display interface
LCD:	Segmented LCD (only partial usable)
SAI:	Serial Audio Interface (I2S and AC97)
ESAI:	Enhanced Serial Audio Interface (I2S and AC97)
FTM:	FlexTimer, general purpose timer, can be used as PWM output
CAN:	Controller Area Network
I2C:	Inter Integrated Circuit
RMII:	Reduced Media Independent Interface (interface between Ethernet MAC and PHY)
NF:	NAND Flash, Interface for the internal NAND Flash
ADC:	Analogue to Digital Converter
DACO:	Digital to Analogue Converter Output
VADCSE:	Video ADC, composite video input
TAMPER:	Tamper detection signal

X1 Pin	GPIO Pad	GPIO Port	ALT0 (GPIO)	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
19	PAD_27	PORT0[27]	PTB5	FTM0_CH5	SCI1_RX	ADC1_SE4	LCD39	VIU_DE	VIU_DATA23	QSPI1_A_DQS
21	PAD_26	PORT0[26]	PTB4	FTM0_CH4	SCI1_TX	ADC0_SE4	LCD38	VIU_FID	VIU_DATA22	QSPI1_A_DATA0
23	PAD_10	PORT0[10]	PTA20	TRACED4			LCD33		SCI3_TX	DCU1_HSYNC/ DCU1_TCON1
25	PAD_35	PORT1[3]	PTB13	SCI0_CTS		SPI0_PCS4	DCU0_TCON7	FB_AD0	TRACECTL	
27	PAD_34	PORT1[2]	PTB12	SCI0_RTS		SPI0_PCS5	DCU0_TCON6	FB_AD1	NMI	ENET0_1588_TMR1
29	PAD_21	PORT0[21]	PTA31	TRACED15	SAI3_TX_SYNC	ENET1_1588_TMR3	SCI4_CTS	I2C3_SDA		SCI3_RX
31	PAD_11	PORT0[11]	PTA21/ MII0_RXCLK	TRACED5				SAI2_RX_BCLK	SCI3_RX	DCU1_VSYNC/ DCU1_TCON2
33	PAD_33	PORT1[1]	PTB11	SCI0_RX			DCU0_TCON5	SNVS_ALARM_OUT_B	CKO2	ENET0_1588_TMR0
35	PAD_32	PORT1[0]	PTB10	SCI0_TX			DCU0_TCON4	VIU_DE	CKO1	ENET_TS_CLKIN
37	PAD_20	PORT0[20]	PTA30	TRACED14	SAI3_RX_SYNC	ENET1_1588_TMR2	SCI4_RTS	I2C3_SCL		SCI3_TX
43	PAD_42	PORT1[10]	PTB20	SPI0_SIN			LCD42		VIU_DATA11	CCM_OBS2
45	PAD_41	PORT1[9]	PTB19	SPI0_PCS0					VIU_DATA10	CCM_OBS1
47	PAD_14	PORT0[14]	PTA24	TRACED8	USB1_VBUS_EN			SDHC1_CLK	DCU1_TCON4	
49	PAD_17	PORT0[17]	PTA27	TRACED11	SAI3_RX_BCLK			SDHC1_DAT1	DCU1_TCON7	
51	PAD_18	PORT0[18]	PTA28	TRACED12	SAI3_RX_DATA	ENET1_1588_TMR0	SCI4_TX	SDHC1_DAT2	DCU1_TCON8	
53	PAD_19	PORT0[19]	PTA29	TRACED13	SAI3_TX_DATA	ENET1_1588_TMR1	SCI4_RX	SDHC1_DAT3	DCU1_TCON9	
55	PAD_39	PORT1[7]	PTB17	CAN1_TX	I2C1_SDA		DCU0_TCON11			
57	PAD_116	PORT3[20]	PTE11	DCU0_R6		RCON4	LCD11			
59	PAD_22	PORT0[22]	PTB0	FTM0_CH0	ADC0_SE2	TRACECTL	LCD34	SAI2_RX_BCLK	VIU_DATA18	QSPI1_A_CS0
	PAD_52	PORT1[20]	PTC7	RMII0_TXD0/ MII0_TXD[0]		SPI1_SOUT	ESAI_SDO4/ ESAI_SDI1		VIU_DATA7	DCU0_B0
61	PAD_117	PORT3[21]	PTE12	DCU0_R7	SPI1_PCS3	RCON5	LCD12			LPT_ALT0
63	PAD_38	PORT1[6]	PTB16	CAN1_RX	I2C1_SCL		DCU0_TCON10			
65	PAD_40	PORT1[8]	PTB18	SPI0_PCS1	EXT_AUDIO_MCLK		CKO1		VIU_DATA9	CCM_OBS0
67	PAD_31	PORT0[31]	PTB9	FTM1_CH1		FTM1_QD_PHB				DCU1_R7
	PAD_51	PORT1[19]	PTC6	RMII0_TXD1/ MII0_TXD[1]		SPI1_SIN	ESAI_SDO5/ESAI_SDI0	SDHC0_WP	VIU_DATA6	DCU0_G1
69	PAD_64	PORT2[0]	PTD30	FB_AD30	NF_IO14		FTM3_CH1	SPI2_PCS0		

X1 Pin	GPIO Pad	GPIO Port	ALT0 (GPIO)	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
71	PAD_45	PORT1[13]	PTC0	RMII0_MDC/ MII0_MDC	FTM1_CH0	SPI0_PCS3	ESAI_SCKT	SDHC0_CLK	VIU_DATA0	RCON18
73	PAD_43	PORT1[11]	PTB21	SPI0_SOUT			LCD43		VIU_DATA12	DCU1_PCLK
75	PAD_91	PORT2[27]	PTD12	QSPI0_B_DATA0	SPI3_SOUT		FB_AD3			
77	PAD_44	PORT1[12]	PTB22	SPI0_SCK			VLCD	VIU_FID		
79	PAD_49	PORT1[17]	PTC4	RMII0_RXD0/ MII0_RXD[0]	SCI1_RTS	SPI1_PCS1	ESAI_SDO2/ ESAI_SDI3	SDHC0_DAT2	VIU_DATA4	DCU0_R1
81	PAD_29	PORT0[29]	PTB7	FTM0_CH7	SCI1_CTS	QSPI0_B_CS1	LCD41		VIU_VSYNC	SCI2_RX
85	PAD_53	PORT1[21]	PTC8	RMII0_TXEN/ MII0_TXEN		SPI1_SCK			VIU_DATA8	DCU0_B1
87				RESETB/RESET_OUT						
89	PAD_2	PORT0[2]	PTA9	JTDI	RMII_CLKOUT	RMII_CLKIN/ MII0_TXCLK	DCU0_R1		WDOG_b	
93	PAD_98	PORT3[2]	PTB28	SAI0_TX_SYNC		RCON23	FB_RW_b			DCU1_B6
95	PAD_103	PORT3[7]	PTC30	SAI1_RX_SYNC	SPI1_PCS2	RCON28	FB_MUXED_BE0_b	FB_TSIZ0	ADC0_SE5	DCU1_B5
97	PAD_50	PORT1[18]	PTC5	RMII0_RXER/ MII0_RXER	SCI1_CTS	SPI1_PCS0	ESAI_SDO3/ ESAI_SDI2	SDHC0_DAT3	VIU_DATA5	DCU0_G0
99	PAD_65	PORT2[1]	PTD29	FB_AD29	NF_IO13		FTM3_CH2	SPI2_SIN		
101	PAD_47	PORT1[15]	PTC2	RMII0_CRS_DV	SCI1_TX		ESAI_SDO0	SDHC0_DAT0	VIU_DATA2	RCON20
103	PAD_48	PORT1[16]	PTC3	RMII0_RXD1/ MII0_RXD[1]	SCI1_RX		ESAI_SDO1	SDHC0_DAT1	VIU_DATA3	DCU0_R0
105	PAD_96	PORT3[0]	PTB26	SAI0_TX_DATA	SCI1_CTS	RCON21	FB_CS0_b	NF_CE1_b		DCU1_G6
107	PAD_67	PORT2[3]	PTD27	FB_AD27	NF_IO11	I2C2_SDA	FTM3_CH4	SPI2_SCK		
127	PAD_68	PORT2[4]	PTD26	FB_AD26	NF_IO10		FTM3_CH5	SDHC1_WP		
129	PAD_83	PORT2[19]	PTD4	QSPI0_A_DATA1		SPI1_PCS1	FB_AD11	SPDIF_SRCLK		
131	PAD_108	PORT3[12]	PTE3	DCU0_TAG/ DCU0_TCON0			LCD3			
133	PAD_88	PORT2[24]	PTD9	QSPI0_B_DATA3	SPI3_PCS1		FB_AD6		SAI1_TX_SYNC	DCU1_B0
135	PAD_89	PORT2[25]	PTD10	QSPI0_B_DATA2	SPI3_PCS0		FB_AD5			DCU1_B1
137	PAD_102	PORT3[6]	PTC29	SAI1_TX_DATA	SPI0_PCS2	RCON27	FB_BE1_b	FB_MUXED_TSIZ1		DCU1_B4
				USB0_VBUS_DETECT						
139				USB1_DP						

X1 Pin	GPIO Pad	GPIO Port	ALT0 (GPIO)	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
141				USB1_DM						
143				USB0_DP						
145				USB0_DM						
2				ADC1_SE9						
4				ADC0_SE9						
6				ADC1_SE8						
8				ADC0_SE8						
14	PAD_9	PORT0[9]	PTA19	TRACED3	ADC0_SE1	FTM1_QD_PHB	LCD32	SAI2_TX_SYNC	VIU_DATA17	QSPILA_SCK
16	PAD_8	PORT0[8]	PTA18	TRACED2	ADEC0_SE0	FTM1_QD_PHA	LCD31	SAI2_TX_DATA	VIU_DATA16	I2C1_SDA
18	PAD_6	PORT0[6]	PTA16	TRACED0	USB0_VBUS_EN	ADC1_SE0	LCD29	SAI2_TX_BCLK	VIU_DATA14	I2C0_SDA
20	PAD_24	PORT0[24]	PTB2	FTMO_CH2	ADC1_SE2	RCON31	LCD36	SAI2_RX_SYNC	VIU_DATA20	QSPI1_A_DATA2
22	PAD_104	PORT3[8]	PTC31	SAI1_TX_SYNC		RCON29			ADC1_SE5	DCU1_B6
24	PAD_25	PORT0[25]	PTB3	FTM0_CH3	ADC1_SE3	EXTRIG	LCD37		VIU_DATA21	QSPI1_A_DATA1
26				RESETB/ RESET_OUT						
28	PAD_30	PORT0[30]	PTB8	FTM1_CH0		FTM1_QD_PHA		VIU_DE		DCU1_R6
30	PAD_23	PORT0[23]	PTB1	FTM0_CH1	ADC0_SE3	RCON30	LCD35	SAI2_RX_DATA	VIU_DATA19	QSPI1_A_DATA3
32	PAD_82	PORT2[18]	PTD3	QSPI0_A_DATA2	SCI2_CTS	SPI1_PCS2	FB_AD12	SPDIF_PLOCK		
34	PAD_81	PORT2[17]	PTD2	QSPI0_A_DATA3	SCI2_RTS	SPI1_PCS3	FB_AD13	SPDIF_OUT1		
36	PAD_80	PORT2[16]	PTD1	QSPI0_A_CS0	SCI2_RX		FB_AD14	SPDIF_IN1		
38	PAD_79	PORT2[15]	PTD0	QSPI0_A_SCK	SCI2_TX		FB_AD15	SPDIF_EXTCLK		
44	PAD_109	PORT3[13]	PTE4	DCU0_DE/ DCU0_TCON3			LCD4			
46	PAD_121	PORT3[25]	PTE16	DCU0_G3		RCON7	LCD16			
48	PAD_123	PORT3[27]	PTE18	DCU0_G5		RCON9	LCD18			
50	PAD_125	PORT3[29]	PTE20	DCU0_G7		RCON11	LCD20	I2C0_SDA		EWM_in
52	PAD_112	PORT3[16]	PTE7	DCU0_R2		RCON0	LCD7			
54	PAD_113	PORT3[17]	PTE8	DCU0_R3		RCON1	LCD8			
56	PAD_107	PORT3[11]	PTE2	DCU0_PCLK			LCD2			
58	PAD_131	PORT4[3]	PTE26	DCU0_B5		RCON15	LCD26			

X1 Pin	GPIO Pad	GPIO Port	ALT0 (GPIO)	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
60	PAD_130	PORT4[2]	PTE25	DCU0_B4		RCON14	LCD25			
62	PAD_122	PORT3[26]	PTE17	DCU0_G4		RCON8	LCD17			
64	PAD_115	PORT3[19]	PTE10	DCU0_R5		RCON3	LCD10			
66	PAD_114	PORT3[18]	PTE9	DCU0_R4		RCON2	LCD9			
68	PAD_105	PORT3[9]	PTE0	DCU0_HSYNC/ DCU0_TCON1	BOOTMOD1		LCD0			
70	PAD_129	PORT4[1]	PTE24	DCU0_B3		RCON13	LCD24			
72	PAD_133	PORT4[5]	PTE28	DCU0_B7		RCON17	LCD28	I2C1_SDA		EWM_out
74	PAD_124	PORT3[28]	PTE19	DCU0_G6		RCON10	LCD19	I2C0_SCL		
76	PAD_128	PORT4[0]	PTE23	DCU0_B2		RCON12	LCD23			
78	PAD_132	PORT4[4]	PTE27	DCU0_B6		RCON16	LCD27	I2C1_SCL		
80	PAD_120	PORT3[24]	PTE15	DCU0_G2		RCON6	LCD15			
82	PAD_106	PORT3[10]	PTE1	DCU0_VSYNC/ DCU0_TCON2	BOOTMOD0		LCD1			
86	PAD_84	PORT2[20]	PTD5	QSPI0_A_DATA0		SPI1_PCS0	FB_AD10			
88	PAD_87	PORT2[23]	PTD8	QSPI0_B_CS0	FB_CLKOUT	SPI1_SCK	FB_AD7			
90	PAD_85	PORT2[21]	PTD6	QSPI0_A_DQS		SPI1_SIN	FB_AD9			
92	PAD_86	PORT2[22]	PTD7	QSPI0_B_SCK		SPI1_SOUT	FB_AD8			
94	PAD_28	PORT0[28]	PTB6	FTM0_CH6	SCI1_RTS	QSPI0_A_CS1	LCD40	FB_CLKOUT	VIU_HSYNC	SCI2_TX
96	PAD_134	PORT4[6]	PTA7	VIU_PIX_CLK						
98	PAD_46	PORT1[14]	PTC1	RMII0_MDIO/ MII0_MDC	FTM1_CH1	SPI0_PCS2	ESAI_FST	SDHC0_CMD	VIU_DATA1	RCON19
100	PAD_92	PORT2[28]	PTD13	QSPI0_B_DQS	SPI3_SCK		FB_AD2			
102	PAD_5	PORT0[5]	PTA12	TRACECK	EXT_AUDIO_MCLK				VIU_DATA13	I2C0_SCL
104	PAD_66	PORT2[2]	PTD28	FB_AD28	NF_IO12	I2C2_SCL	FTM3_CH3	SPI2_SOUT		
106	PAD_63	PORT1[31]	PTD31	FB_AD31	NF_IO15		FTM3_CH0	SPI2_PCS1		
134	PAD_7	PORT0[7]	PTA17	TRACED1	USB0_VBUS_OC	ADC1_SE1	LCD30	USB0_SOF_PULSE	VIU_DATA15	I2C1_SCL
136	PAD_126	PORT3[30]	PTE21	DCU0_B0			LCD21			
138	PAD_127	PORT3[31]	PTE22	DCU0_B1			LCD22			
140	PAD_118	PORT3[22]	PTE13	DCU0_G0			LCD13			

X1 Pin	GPIO Pad	GPIO Port	ALT0 (GPIO)	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
142	PAD_119	PORT3[23]	PTE14	DCU0_G1			LCD14			
144	PAD_110	PORT3[14]	PTE5	DCU0_R0			LCD5			
146	PAD_111	PORT3[15]	PTE6	DCU0_R1			LCD6			
162				VADCSE0						
164				VADCSE1						
166				VADCSE2						
168				VADCSE3						
170				EXT_TAMPER0						
172				EXT_TAMPER1						
174				EXT_TAMPER2/ EXT_WM0_TAMPER_IN						
176				EXT_TAMPER3/ EXT_WM0_TAMPER_OUT						
178				EXT_TAMPER4/ EXT_WM1_TAMPER_IN						
180				EXT_TAMPER5/ EXT_WM1_TAMPER_OUT						
184	PAD_69	PORT2[5]	PTD25	FB_AD25	NF_IO9		FTM3_CH6			
186	PAD_70	PORT2[6]	PTD24	FB_AD24	NF_IO8		FTM3_CH7			
188	PAD_90	PORT2[26]	PTD11	QSPI0_B_DATA1	SPI3_SIN		FB_AD4			
190	PAD_15	PORT0[15]	PTA25	TRACED9	USB1_VBUS_OC			SDHC1_CMD	DCU1_TCON5	
192	PAD_16	PORT0[16]	PTA26	TRACED10	SAI3_TX_BCLK			SDHC1_DAT0	DCU1_TCON6	
194	PAD_37	PORT1[5]	PTB15	CAN0_TX	I2C0_SDA		DCU0_TCON9			VIU_PIX_CLK
196	PAD_36	PORT1[4]	PTB14	CAN0_RX	I2C0_SCL		DCU0_TCON8			DCU1_PCLK

***This pin is not available on VF61**

5 Interface Description

5.1 Power Signals

5.1.1 Digital Supply

Table 5-1 Digital Supply Pins

X1 Pin #	Signal Name	I/O	Description	Remarks
42, 84,108, 148,182,198, 200	3V3	I	3.3V main power supply	Use decoupling capacitors on all pins.
39, 41, 83, 109,147, 181, 197, 199	GND	I	Digital Ground	
40	VCC_BATT	I/O	RTC Power supply can be connected to a backup battery.	Connect this pin to 3.3V even if the internal RTC is not used.

5.1.2 Analogue Supply

Table 5-2 Analogue Supply Pins

X1 Pin #	Signal Name	I/O	Description	Remarks
10, 12	AVDD_AUDIO	I	3.3V analogue supply	Always connect this pin **to a 3.3V supply**. For better Audio accuracy we recommend filtering this supply separately from the digital supply. This pin is connected to the Audio Codec and the analogue supply of the Vybrid.
9, 11	VSS_AUDIO	I	Analogue Ground	Always connect this pin to GND. For better Audio accuracy we recommend filtering this supply separate from the digital supply. Internally this pin is not connected with Digital GND on the Colibri VFxx module.

5.1.3 Reset

Table 5-3 Reset Pins

X1 Pin #	Signal Name	I/O	Voltage Level	Description	Remarks
26	nRESET_EXT	I	3V3	Reset Input	This pin is low active and resets the Colibri module.
87	nRESET_OUT	O	3V3	Reset Output	This pin is active low. This pin is driven low at boot up. There is a 10k Ohm pull-up on this pin.

The RESETB/RESET_OUT pin of the Vybrid SoC is bidirectional and connected to both SODIMM signals, nRESET_EXT and nRESET_OUT. Figure 4 shows the internal circuit of the reset signal.

5.2 GPIOs

Most Vybrid pins have a GPIO (General Purpose Input/Output) function. Please check which pins are GPIO capable in the function list in section 4.4. The GPIO functionality is configured by selecting the alternative function ALT0. For accessing GPIOs, the pins are grouped in ports (PORT0 to PORT4). The mapping between the port name (e.g. PORT0[27]) and pad name (e.g. PTB5) of the GPIO can be found in the same table in section 4.4. Additional to the pad name, the GPIOs also have a pad number (e.g. PAD_27) which can be found in the same table. Some software implementations might refer to the GPIO pad number.

All GPIO pins can be used as an interrupt source. The interrupt function of each GPIO can be configured to the following modes:

- Interrupt disabled (default after reset)
- Active high level sensitive interrupt
- Active low level sensitive interrupt
- Rising edge sensitive interrupt
- Falling edge sensitive interrupt
- Rising and falling edge sensitive interrupt
- Rising edge sensitive DMA request
- Falling edge sensitive DMA request
- Rising and falling edge sensitive DMA request

A digital filter can be enabled individually for each GPIO. This filter can help prevent glitches from triggering an unwanted interrupt. The filter width is the same within one GPIO port. It can only be changed per port.

5.2.1 Wakeup Source

Certain pins can be used to wake up the Colibri from a suspended state (LPStop). There is on-chip analogue glitch filtering, which can be deactivated if required. The enabling of this analogue filter is independent of the digital filter. Each wakeup pin can be individually enabled and selected whether it is triggered on a rising or falling edge.

Table 5-4 Wakeup Pins

X1 Pin#	Wakeup Source	Remarks
19	WKPU_P5	
21	WKPU_P4	
24	WKPU_P3	
27	WKPU_P9	
30	WKPU_P1	
33	WKPU_P8	
43	WKPU_P13	Preferred Wakeup Source
45	WKPU_P12	Preferred Wakeup Source
50	WKPU_P16	
59	WKPU_P0	
63	WKPU_P11	
81	WKPU_P7	
94	WKPU_P6	
95	WKPU_P15	
196	WKPU_P10	

For the Colibri VF61, the WKPU_P2 (Vybrid pin PTB2) is also connected to the Wolfson WM9715L pin 45. This allows the audio codec to wake up the system by creating a generic interrupt (GENIRQ) if the resistive touch panel interface detects a touch on the display.

For the Colibri VF50, the WKU_P2 (Vybrid pin PTB2) is connected to the TMSY pin of the resistive touch panel interface.

5.3 Ethernet

The Vybrid SoC features two 10/100 Mbit Ethernet media access controls (MACs) with L2 switch and IEEE1588 clock. On the Colibri module, there is one Ethernet transceiver (PHY), which needs only the magnetics to be present on the carrier board. Please check the datasheet of the Microchip/Micrel KSZ8041NL Ethernet PHY to learn more about the features of the chip.

X1 Pin#	Colibri Signal Name	PHY Signal Name	I/O	Voltage Level	Description
189	TXO+	TX+	O		100BASE-TX: Transmit + (Auto MDIX: Receive +)
187	TXO-	TX-	O		100BASE-TX: Transmit - (Auto MDIX: Receive -)
195	RXI+	RX+	I		100BASE-TX: Receive + (Auto MDIX: Transmit +)
193	RXI-	RX-	I		100BASE-TX: Receive - (Auto MDIX: Transmit -)
191	AGND_LAN	GND			Ethernet ground, on VFxx connected to common GND
183	LINK_AKT	LED0	O	3V3	Link activity indication LED
185	SPEED100	LED1	O	3V3	100Mbit/s indication LED

If the second Ethernet port is required, an additional PHY needs to be implemented on the carrier board. The interface between Colibri VFxx module and PHY is a Reduced Media Independent Interface (RMII). This interface is not part of the Colibri standard interfaces. The signals are mainly located on the camera interface signals.

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
59	PWM<A>, Camera Input Data<7>	RMII0_TXD0/ MII0_TXD[0]	O	3V3	Transmit data bit 0 (MAC to PHY)
67	PWM<D>, Camera Input Data<6>	RMII0_TXD1/ MII0_TXD[1]	O	3V3	Transmit data bit 1 (MAC to PHY)
85	Camera Input Data<8>, Keypad_Out<4>	RMII0_TXEN/ MII0_TXEN	O	3V3	Transmit data enable (MAC to PHY)
89	GPIO	RMII_CLKOUT	O	3V3	50 MHz Reference Clock output (MAC to PHY)
79	Camera Input Data<4>	RMII0_RXD0/ MII0_RXD[0]	I	3V3	Receive data bit 0 (PHY to MAC)
103	Camera Input Data<3>	RMII0_RXD1/ MII0_RXD[1]	I	3V3	Receive data bit 1 (PHY to MAC)
101	Camera Input Data<2>	RMII0_CRS_DV	I	3V3	Carrier Sense / Data Valid (PHY to MAC)
97	Camera Input Data<5>	RMII0_RXER/ MII0_RXER	I	3V3	Receive Error (optional) (PHY to MAC)
98	Camera Input Data<1>	RMII0_MDIO/ MII0_MDC	I/O	3V3	Management data
71	Camera Input Data<0>, LCD Back-Light GPIO	RMII0_MDC/ MII0_MDC	O	3V3	Management clock

5.4 USB

Colibri VFxx provides two USB 2.0 High Speed (480 Mbit/s) ports. Both ports can be configured independently as host or client through firmware interfaces. The ports are not true OTG controllers. The Colibri standard requires only one USB port to be configurable as host or client. This port is called USBC in the following table.
When using USB, you have to be careful to not introduce any back feeding into the module.

5.4.1 USB Data Signal

Table 5-5USB Data Pins

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Description
139	USBH_P	USB1_DP	I/O	Positive Differential Signal for USB Host port
141	USBH_N	USB1_DM	I/O	Negative Differential Signal for USB Host port
143	USBC_P	USB0_DP	I/O	Positive Differential Signal for the shared USB Host / Client port
145	USBC_N	USB0_DM	I/O	Negative Differential Signal for the shared USB Host / Client port

5.4.2 USB Control Signals

Table 5-6 USB OTG Pins

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
135	USB_ID	PTD10	I	3V3	Use this pin to detect the ID pin if you use USB OTG
137	USBC_DET	USB0_VBUS_DETECT/ PTC29	I	3V3	Use this pin to detect if VBUS is present (5V USB supply). Please note that this pin is only 3.3V tolerant This signal is connected to two pins of the Vybrid SoC

If you use the USB Host function you need to generate the 5V USB supply voltage on your carrier board. Colibri VFxx provides two optional signals for the USB supply. We recommend using the following pins to guarantee the best possible compatibility, however - you can use other GPIOs or not use the signals at all.

Table 5-7 USB Power Control Pins

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
129	USBH_PEN	PTD4	O	3V3	This pin enables the external USB voltage supply.
131	USBH_OC	PTE3	I	3V3	USB overcurrent, this pin can Signal an over current condition in the USB supply

5.5 Display

Colibri VFxx has a display controller unit (DCU) for TFT displays of up to 1024x768 resolution. The Vybrid SoC features a second DCU, but not all the interface pins are accessible via the SODIMM connector, since the pins are shared with the internal NAND flash interface. Therefore, only one display interface can be used.

Features for the DCU

- 64 graphics layers
- Each pixel can be blended from up to 6 source layers
- Hardware cursor layer with blinking option
- Display of real-time video from external video source (camera parallel or composite input)
- Fully programmable display timing and resolution
- Gamma correction with 8bit resolution on each colour component
- Temporal dithering

5.5.1 Parallel RGB LCD interface

Colibri VFxx provides a parallel LCD interface on the SODIMM connector. It supports up to 24 bit colour per pixel. The first 18bits are backward compatible with the existing Colibri PXAxxx family. The whole 24bit interface is backward compatible with the existing Colibri T20 and T30 modules.

Features

- Up to XGA (1024x768) resolution
- Up to 24 bit colour
- Supports parallel TTL displays
- Max pixel clock 60MHz

Table 5-LCD signal Pins

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	24bit RGB Interface	18bit RGB Interface	16bit RGB Interface
76	LCD RGB Data<0>	DCU0_B2	O	3V3	B2	B0	
70	LCD RGB Data<1>	DCU0_B3	O	3V3	B3	B1	B0
60	LCD RGB Data<2>	DCU0_B4	O	3V3	B4	B2	B1
58	LCD RGB Data<3>	DCU0_B5	O	3V3	B5	B3	B2
78	LCD RGB Data<4>	DCU0_B6	O	3V3	B6	B4	B3
72	LCD RGB Data<5>	DCU0_B7	O	3V3	B7	B5	B4
80	LCD RGB Data<6>	DCU0_G2	O	3V3	G2	G0	G0
46	LCD RGB Data<7>	DCU0_G3	O	3V3	G3	G1	G1
62	LCD RGB Data<8>	DCU0_G4	O	3V3	G4	G2	G2
48	LCD RGB Data<9>	DCU0_G5	O	3V3	G5	G3	G3
74	LCD RGB Data<10>	DCU0_G6	O	3V3	G6	G4	G4
50	LCD RGB Data<11>	DCU0_G7	O	3V3	G7	G5	G5
52	LCD RGB Data<12>	DCU0_R2	O	3V3	R2	R0	
54	LCD RGB Data<13>	DCU0_R3	O	3V3	R3	R1	R0
66	LCD RGB Data<14>	DCU0_R4	O	3V3	R4	R2	R1
64	LCD RGB Data<15>	DCU0_R5	O	3V3	R5	R3	R2
57	LCD RGB Data<16>	DCU0_R6	O	3V3	R6	R4	R3
61	LCD RGB Data<17>	DCU0_R7	O	3V3	R7	R5	R4
136	LCD RGB Data<18>	DCU0_B0	O	3V3	B0		
138	LCD RGB Data<19>	DCU0_B1	O	3V3	B1		
140	LCD RGB Data<20>	DCU0_G0	O	3V3	G0		
142	LCD RGB Data<21>	DCU0_G1	O	3V3	G1		
144	LCD RGB Data<22>	DCU0_R0	O	3V3	R0		
146	LCD RGB Data<23>	DCU0_R1	O	3V3	R1		
44	LCD RGB DE	DCU0_DE / DCU0_TCON3	O	3V3	Data Enable (other names: Output Enable)		
68	LCD RGB HSYNC	DCU0_HSYNC / DCU0_TCON1	O	3V3	Horizontal Sync (other names: Line Clock, L_LCKL_A0), Do not pull up these signals during power up		
56	LCD RGB PCLK	DCU0_PCLK	O	3V3	Pixel Clock (other names: Dot Clock, L_PCLK_WR)		
82	LCD RGB VSYNC	DCU0_VSYNC / DCU0_TCON2	O	3V3	Vertical Sync (other names: Frame Clock, L_FCLK) Do not pull up these signals during power up		

Typically you will also require some signals to control the Backlight and/or the display enable signal. You can use any free GPIO for this function but we recommend using the same as we did on our standard carrier boards, this minimises the required SW configurations. If you would like to use a PWM signal to control the backlight brightness use a pin with PWM function for the Backlight Control- see also section 5.12.

The HSYNC and VSYNC signals are also used as boot strapping pins. The pins need to have low logic level during the power up cycle in order to boot from the internal flash memory. Therefore, 10k pull down resistors are placed on the module. It is recommended to add buffers on the carrier board to prevent back feeding problems. The Colibri Evaluation board V3.x and all versions of the Iris Carrier board feature such buffers. Older carrier boards, such as the Colibri Evaluation board V2.x have the signals directly connected to the VGA connector. This can lead to problems if certain monitors with pull up resistors on these signals are plugged in. See also section 7.

5.5.2 HDMI

Colibri VFxx does not have an HDMI interface.

5.5.3 Analogue VGA

Colibri VFxx does not have an Analogue VGA interface. However, it is possible to add a VGA DAC on the carrier board. The Colibri Evaluation board features a reference design for such a DAC.

5.5.4 DDC (Display Data Channel)

Colibri VFxx does not provide a dedicated DDC interface. If required, one of the I²C interfaces can be used as DDC. Since the DDC is 5V compatible, a level shifter from 3.3V would be required.

5.5.5 LVDS

Colibri VFxx does not have a direct LVDS interface. However, it is very easy to use the parallel LCD port with an LVDS transmitter. The Colibri Evaluation board provides a reference design for an LVDS interface implementation. Contact Toradex if you have any questions how to connect a LVDS transmitter.

5.6 External Memory Bus

Colibri VFxx does not feature an external memory bus that is compatible within the Colibri family. There is an external bus (called FlexBus) available as a secondary function of interface pins. Some bus control signals are missing since they are only available on Vybrid pins that are connected to the internal NAND flash. Whenever it is possible, the SPI, QSPI, USB or I²C interface should be preferred for connecting a peripheral device including FPGA or DSPs.

Table 5-8 Flex Bus Pins

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
25	UART_A CTS, Keypad_In<0>	FB_AD0	I/O	3V3	Multiplexed: Address/Data 0 Non-Multiplexed: Address 0
27	UART_A RTS	FB_AD1	I/O	3V3	Multiplexed: Address/Data 1 Non-Multiplexed: Address 1
100	Keypad_Out<1>	FB_AD2	I/O	3V3	Multiplexed: Address/Data 2 Non-Multiplexed: Address 2
75	GPIO	FB_AD3	I/O	3V3	Multiplexed: Address/Data 3 Non-Multiplexed: Address 3
188	GPIO	FB_AD4	I/O	3V3	Multiplexed: Address/Data 4 Non-Multiplexed: Address 4
135	GPIO	FB_AD5	I/O	3V3	Multiplexed: Address/Data 5 Non-Multiplexed: Address 5
133	GPIO	FB_AD6	I/O	3V3	Multiplexed: Address/Data 6 Non-Multiplexed: Address 6
88	SPI CLK	FB_AD7	I/O	3V3	Multiplexed: Address/Data 7 Non-Multiplexed: Address 7
		FB_CLKOUT	O	3V3	FlexBus Clock Out
92	SPI TXD	FB_AD8	I/O	3V3	Multiplexed: Address/Data 8 Non-Multiplexed: Address 8
90	SPI RXD	FB_AD9	I/O	3V3	Multiplexed: Address/Data 9 Non-Multiplexed: Address 9
86	SPI CS	FB_AD10	I/O	3V3	Multiplexed: Address/Data 10 Non-Multiplexed: Address 10

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
129	USBH_PEN	FB_AD11	I/O	3V3	Multiplexed: Address/Data 11 Non-Multiplexed: Address 11
32	UART_B CTS	FB_AD12	I/O	3V3	Multiplexed: Address/Data 12 Non-Multiplexed: Address 12
34	UART_B RTS	FB_AD13	I/O	3V3	Multiplexed: Address/Data 13 Non-Multiplexed: Address 13
36	UART_B RXD	FB_AD14	I/O	3V3	Multiplexed: Address/Data 14 Non-Multiplexed: Address 14
38	UART_B TXD	FB_AD15	I/O	3V3	Multiplexed: Address/Data 15 Non-Multiplexed: Address 15
186	GPIO	FB_AD24	I/O	3V3	Non-Multiplexed: Data 0
184	GPIO	FB_AD25	I/O	3V3	Non-Multiplexed: Data 1
127	GPIO	FB_AD26	I/O	3V3	Non-Multiplexed: Data 2
107	GPIO	FB_AD27	I/O	3V3	Non-Multiplexed: Data 3
104	GPIO	FB_AD28	I/O	3V3	Non-Multiplexed: Data 4
99	GPIO	FB_AD29	I/O	3V3	Non-Multiplexed: Data 5
69	GPIO	FB_AD30	I/O	3V3	Non-Multiplexed: Data 6
106	GPIO	FB_AD31	I/O	3V3	Non-Multiplexed: Data 7
137	USBC_DET	FB_MUXED_TSIZ1		3V3	Can be configured either as - FB_TSIZ1: Transfer Size bit 1 - FB_BE2_b: Byte Enable for bits 23 to 16
		FB_BE1_b		3V3	Byte Enable for bits 15 to 8
94	Camera Input HSYNC	FB_CLKOUT	O	3V3	FlexBus Clock Out
105	GPIO	FB_CS0_b	O	3V3	General Purpose Chip Select
95	GPIO	FB_MUXED_BE0_b		3V3	Can be configured either as - FB_TA: Transfer Acknowledge - FB_CS3 General Purpose Chip Select - FB_BE0_b Byte Enable for bits 7 to 0
		FB_TSIZ0	O	3V3	Transfer Size bit 0
93	GPIO	FB_RW_b	O	3V3	Read/Write Indication (low for indicating write)

5.7 IDE

Colibri VFxx does not support an integrated drive electronics interface (IDE).

5.8 I2C

Colibri VFxx offers four I²C controllers. These implement the I²C version 2.0 specification with the exception that high speed mode is not supported. All can be used as master or slave. Port 0 is provided on the pins that are compatible with the Colibri family. The other ports are available as secondary functions of the SODIMM pins.

Features:

- Supports standard (0-100 kHz) and fast mode of operation (0-400 kHz)
- Independent Master Controller and Slave Controller
- Multi-master operation
- Software selectable acknowledge bit
- Interrupt driven byte-by-byte data transfer
- Arbitration loss interrupt with automatic mode switching from master to slave
- Calling address identification interrupts
- Start and stop signal generation and detection
- Repeated start signal generation
- Acknowledge bit generation and detection
- Bus busy detection
- Basic DMA interface
- SMBus support

There are lots of low speed devices which use I²C interfaces such as RTCs or sensors and the interface is also used to configure other devices like cameras or displays. The I²C Bus can also be used to communicate with System Management Bus (SMBus) devices.

Table 5-9 I²C Signals (Colibri family compatible interface)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
194	I2C SDA	I2C0_SDA	I/O	3V3	Open Drain Data Signal Port 0
196	I2C SCL	I2C0_SCL	I/O	3V3	Clock Signal Port 0

Table 5-10 I²C Signals (additional, not compatible with other Colibri family modules)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
102	nPWAIT	I2C0_SCL	I/O	3V3	Alternative pin for Clock Signal Port 0
55	GPIO	I2C1_SDA	I/O	3V3	Open Drain Data Signal Port 1
72	LCD RGB Data<5>			3V3	
63	GPIO	I2C1_SCL	I/O	3V3	Clock Signal Port 1
78	LCD RGB Data<4>			3V3	
134	GPIO			3V3	
107	GPIO	I2C2_SDA	I/O	3V3	Open Drain Data Signal Port 2
104	GPIO	I2C2_SCL	I/O	3V3	Clock Signal Port 2
29	UART_A DSR	I2C3_SDA	I/O	3V3	Open Drain Data Signal Port 3
37	UART_A RI, Keypad_In<4>	I2C3_SCL	I/O	3V3	Clock Signal Port 3

5.9 UART

Colibri VFxx provides up to five serial UART interfaces (the Vybrid SoC itself features six interfaces, but one of them is not accessible via the SODIMM pins). Three of the five interfaces are backward compatible with the Colibri family with one limitation: The Vybrid SoC does not feature the DTR, DSR, DCD and RI as dedicated signals. However, these signals can be emulated by using GPIOs which are located on these SODIMM pins. The UART0 which is located on the UART_A pins of the SODIMM is also used as a debug interface.
VF61 supports baud rates between 12000bps and 460800bps.
VF50 supports baud rates between 600bps and 256000bps.
UART Features

- Full-duplex operation
- RS485 support
- Standard Mark/space non-return-to-zero (NRZ) format
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receiver input polarity
- Up to 14-bit brake character transmission
- 11-bit break character detection option
- Transmit FIFO (16-entry for UART 0 and 8-entry for the others)
- Receive FIFO (16-entry for UART 0 and 8-entry for rest of UARTs)
- Address match feature in receiver (only UART 0 and 1)
- Support for ISO7816 protocol to interface with SIM cards and smart cards (only UART 0 and 1)
- Support for CEA709.1-B protocol used in building automation and home networking systems
- Hardware flow control (RTS/CTS)
- IrDA 1.4 support on all UARTs

Table 5-11 UART Signals (Colibri family compatible interfaces

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
33	UART_A RXD	SCI0_RX	I	3V3	Receive Data UART0
35	UART_A TXD	SCI0_TX	O	3V3	Transmit Data UART0
27	UART_A RTS	SCI0_RTS	O	3V3	Request to send UART0
25	UART_A CTS, Keypad_In<0>	SCI0_CTS	I	3V3	Clear to send UART0
23	UART_A DTR	PTA20	O	3V3	GPIO only, DTR need to be emulated
29	UART_A DSR	PTA31	I	3V3	GPIO only, DSR need to be emulated
31	UART_A DCD	PTA21/ MII0_RXCLK	I	3V3	GPIO only, DCD need to be emulated
37	UART_A RI, Keypad_In<4>	PTA30	I	3V3	GPIO only, RI need to be emulated
36	UART_B RXD	SCI2_RX	I	3V3	Receive Data UART2
38	UART_B TXD	SCI2_TX	O	3V3	Transmit Data UART2
34	UART_B RTS	SCI2_RTS	O	3V3	Request to send UART2
32	UART_B CTS	SCI2_CTS	I	3V3	Clear to send UART2
19	UART_C RXD	SCI1_RX	I	3V3	Receive Data UART1
21	UART_C TXD	SCI1_TX	O	3V3	Transmit Data UART1

Table 5-12 UART Signals (additional, not compatible with other modules)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
103	Camera Input Data<3>	SCI1_RX	I	3V3	Alternative pin for Receive Data UART1
101	Camera Input Data<2>	SCI1_TX	O	3V3	Alternative pin for Receive Data UART1
94	Camera Input HSYNC	SCI1_RTS	I	3V3	Request to send UART1
79	Camera Input Data<4>			3V3	
81	Camera Input VSYNC	SCI1_CTS	I	3V3	Clear to send UART1
97	Camera Input Data<5>			3V3	
105	GPIO			3V3	
81	Camera Input VSYNC	SCI2_RX	I	3V3	Alternative pin for Receive Data UART2
94	Camera Input HSYNC	SCI2_TX	O	3V3	Alternative pin for Transmit Data UART2
29	UART_A DSR	SCI3_RX	I	3V3	Receive Data UART3
31	UART_A DCD			3V3	
23	UART_A DTR	SCI3_TX	O	3V3	Transmit Data UART3
37	UART_A RI, Keypad_In<4>			3V3	
53	SDCard DAT<3>	SCI4_RX	I	3V3	Receive Data UART4
51	SDCard DAT<2>	SCI4_TX	O	3V3	Transmit Data UART4
37	UART_A RI, Keypad_In<4>	SCI4_RTS	O	3V3	Request to send UART4
29	UART_A DSR	SCI4_CTS	I	3V3	Clear to send UART4

5.10 SPI

Colibri VFxx has four SPI controllers. Each can operate at up to 25Mbps and provide full duplex, synchronous, serial communication between the Colibri module and external peripheral devices. Each SPI channel consists of four signals; clock, chip select (frame), data in and data out. In the Vybrid datasheets SPI is also called DSPI.

Features

- Up to 25Mbit/s
- Full-duplex
- Master and Slave mode
- 4-entry deep transmit FIFO
- 4-entry deep receive FIFO
- Up to 6 peripheral chip selects
- Programmable serial frame size of 4-16 bit (expandable by software)
- DMA support

Each SPI channel supports four different modes of the SPI protocol:

Table 5-13 SPI Modes

SPI Mode	CPOL	CPHA	Description
0	0	0	Base value of Clock is low; data is captured on rising edge, data available on first clock edge
1	0	1	Base value of Clock is low; data is captured on falling edge, clock available before data
2	1	0	Base value of Clock is high; data is captured on falling edge, data available on first clock edge
3	1	1	Base value of Clock is high; data is captured on rising edge, clock available before data

SPI can be used as a fast interface for ADCs, DACs, FPGAs, etc. Some LCD displays require to be configured over SPI prior to being driven via the RGB or LVDS interface.

Table 5-14 SPI Signals (Colibri family compatible interface)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
86	SPI CS	SPI1_PCS0	I/O	3V3	Master Mode: Peripheral Chip Select 0 output Slave Mode: Slave Select input
88	SPI CLK	SPI1_SCK	I/O	3V3	Master Mode: Serial Clock output Slave Mode: Serial Clock input
90	SPI RXD	SPI1_SIN	I	3V3	Master Mode: MISO (Master Input/ Slave Output) Slave Mode: MOSI (Master Output/Slave Input)
92	SPI TXD	SPI1_SOUT	O	3V3	Master Mode: MOSI (Master Output/Slave Input) Slave Mode: MISO (Master Input/ Slave Output)

Table 5-15 SPI Signals (additional, not compatible with other modules)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
45	GPIO	SPI0_PCS0	I/O	3V3	Master Mode: Peripheral Chip Select 0 output Slave Mode: Slave Select input
65	Camera Input Data<9>, Keypad_Out<3>	SPI0_PCS1	O	3V3	Master Mode: Peripheral Chip Select 1 output Slave Mode: not used
137	USBC_DET	SPI0_PCS2	O	3V3	Master Mode: Peripheral Chip Select 2 output Slave Mode: not used
98	Camera Input Data<1>			3V3	
71	Camera Input Data<0>, LCD Back-Light GPIO	SPI0_PCS3	O	3V3	Master Mode: Peripheral Chip Select 3 output Slave Mode: not used

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
25	UART_A CTS, Keypad_In<0>	SPI0_PCS4	O	3V3	Master Mode: Peripheral Chip Select 4 output Slave Mode: not used
27	UART_A RTS	SPI0_PCS5	O	3V3	Master Mode: Peripheral Chip Select 5 output (can also be configured as Peripheral Chip Select Strobe) Slave Mode: not used
77	GPIO	SPI0_SCK	I/O	3V3	Master Mode: Serial Clock output Slave Mode: Serial Clock input
43	WAKEUP Source<0>, SDCard CardDetect	SPI0_SIN	I	3V3	Master Mode: MISO (Master Input/ Slave Output) Slave Mode: MOSI (Master Output/Slave Input)
73	GPIO	SPI0_SOUT	O	3V3	Master Mode: MOSI (Master Output/Slave Input) Slave Mode: MISO (Master Input/ Slave Output)
97	Camera Input Data<5>	SPI1_PCS0	I/O	3V3	Alternative Pin for Master Mode: Peripheral Chip Select 0 output Slave Mode: Slave Select input
79	Camera Input Data<4>	SPI1_PCS1	O	3V3	Master Mode: Peripheral Chip Select 1 output Slave Mode: not used
129	USBH_PEN			3V3	
95	GPIO	SPI1_PCS2	O	3V3	Master Mode: Peripheral Chip Select 2 output Slave Mode: not used
32	UART_B CTS			3V3	
61	LCD RGB Data<17>	SPI1_PCS3	O	3V3	Master Mode: Peripheral Chip Select 3 output Slave Mode: not used
34	UART_B RTS			3V3	
85	Camera Input Data<8>, Keypad_Out<4>	SPI1_SCK	I/O	3V3	Alternative Pin for Master Mode: Serial Clock output Slave Mode: Serial Clock input
67	PWM<D>,Camera Input Data<6>	SPI1_SIN	I	3V3	Alternative Pin for Master Mode: MISO (Master Input/ Slave Output) Slave Mode: MOSI (Master Output/Slave Input)
59	PWM<A>, Camera Input Data<7>	SPI1_SOUT	O	3V3	Alternative Pin for Master Mode: MOSI (Master Output/Slave Input) Slave Mode: MISO (Master Input/ Slave Output)
69	GPIO	SPI2_PCS0	I/O	3V3	Master Mode: Peripheral Chip Select 0 output Slave Mode: Slave Select input
106	GPIO	SPI2_PCS1	O	3V3	Master Mode: Peripheral Chip Select 1 output Slave Mode: not used
107	GPIO	SPI2_SCK	I/O	3V3	Master Mode: Serial Clock output Slave Mode: Serial Clock input
99	GPIO	SPI2_SIN	I	3V3	Master Mode: MISO (Master Input/ Slave Output) Slave Mode: MOSI (Master Output/Slave Input)
104	GPIO	SPI2_SOUT	O	3V3	Master Mode: MOSI (Master Output/Slave Input) Slave Mode: MISO (Master Input/ Slave Output)
135	GPIO	SPI3_PCS0	I/O	3V3	Master Mode: Peripheral Chip Select 0 output Slave Mode: Slave Select input
133	GPIO	SPI3_PCS1	O	3V3	Master Mode: Peripheral Chip Select 1 output Slave Mode: not used
100	Keypad_Out<1>	SPI3_SCK	I/O	3V3	Master Mode: Serial Clock output Slave Mode: Serial Clock input
188	GPIO	SPI3_SIN	I	3V3	Master Mode: MISO (Master Input/ Slave Output) Slave Mode: MOSI (Master Output/Slave Input)
75	GPIO	SPI3_SOUT	O	3V3	Master Mode: MOSI (Master Output/Slave Input) Slave Mode: MISO (Master Input/ Slave Output)

5.11 Quad Serial Peripheral Interface (QuadSPI)

The Quad Serial Peripheral Interface is an SPI interface with four bidirectional data lines instead of one transmit and one receive data line. The interface is mainly used for connecting to flash devices. The QuadSPI is not compatible with the Colibri family. The pins are located on the SODIMM connector as secondary functions.

Features

- Various flash vendor devices supported
- Double Data Rate (DDR) and Single Data Rate (SDR) supported
- Two identical serial flash devices can be connected and accessed in parallel for data read operations with doubled readout bandwidth
- DMA support
- Memory mapped read assess to connected flash devices
- Execute in place (XiP) possible
- Peak DDR Read Bandwidth 132MB/s

Table 5-16 QuadSPI Signals (not compatible with other modules)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
36	UART_B RXD	QSPI0_A_CS0	O	3V3	Chip Select 0
94	Camera Input HSYNC	QSPI0_A_CS1	O	3V3	Chip Select 1, used to select second instance of QuadSPI device (dual die flash require CS0 and CS1)
38	UART_B TXD	QSPI0_A_SCK	O	3V3	Serial Clock
86	SPI CS	QSPI0_A_DATA 0	I/O	3V3	Serial I/O for command, address and data
129	USBH_PEN	QSPI0_A_DATA 1	I/O	3V3	Serial I/O for command, address and data
32	UART_B CTS	QSPI0_A_DATA 2	I/O	3V3	Serial I/O for command, address and data
34	UART_B RTS	QSPI0_A_DATA 3	I/O	3V3	Serial I/O for command, address and data
90	SPI RXD	QSPI0_A_DQS	I	3V3	Data Strobe signal, required on some high speed DDR devices
88	SPI CLK	QSPI0_B_CS0	O	3V3	Chip Select 0
81	Camera Input VSYNC	QSPI0_B_CS1	O	3V3	Chip Select 1, used to select second instance of QuadSPI device (dual die flash require CS0 and CS1)
92	SPI TXD	QSPI0_B_SCK	O	3V3	Serial Clock
75	GPIO	QSPI0_B_DATA 0	I/O	3V3	Serial I/O for command, address and data
188	GPIO	QSPI0_B_DATA 1	I/O	3V3	Serial I/O for command, address and data
135	GPIO	QSPI0_B_DATA 2	I/O	3V3	Serial I/O for command, address and data
133	GPIO	QSPI0_B_DATA 3	I/O	3V3	Serial I/O for command, address and data
100	Keypad_Out<1>	QSPI0_B_DQS	I	3V3	Data Strobe signal, required on some high speed DDR devices

5.12 PWM (Pulse Width Modulation)

The PWM function of Colibri VFxx is provided by the FlexTimer Module (FTM). The Colibri family specifies four PWM pins at the SODIMM connector. Additional to the four standard PWM pins, the module provides an additional 13 PWM capable pins as secondary functions of the SODIMM pins. This leads to a total of 17 PWM output pins.

The FlexTimer Module of the Vybrid SoC consists of four 16bit counters (FTM0 to FTM3). Each of these counters can have up to 8 channels. The channels can have independent duty cycles but are using the same counter. Therefore, the PWM<A> and PWM<C> need to be run with the same frequency but can have different duty cycle. The same restriction also applies between PWM<B> and PWM<D>.

The FTM channels can not only be used as PWM outputs, they can also be configured as input capture or output compare. Additionally, two SODIMM pins can be used as quadrature decoder inputs with filter function.

Features

- 16bit counter, can be used as free-running counter or with initial and final value
- Counter can be configured to count up or up-down
- FTM source clock can be selected flexible
- Pre-scale divider (1 to 128)
- Capture can occur on rising, falling or on both edges.
- Input filter can be selected for some channels
- In Output Compare mode, the output signal can be set, cleared or toggled on match
- All channels can be configured for centre-aligned PWM mode
- The output pins can be paired for equal, complementary or independent output
- Dead time insertion is available for each complementary pair
- Polarity of each channel is configurable
- Dual edge capture for pulse and period width measurement
- Quadrature decoder input with filters, relative position counter and interrupt on position count

The PWM interface can be used as an easy way to emulate a DAC and generate a variable DC voltage if used with a suitable RC circuit. Other uses include control of LED brightness, display backlights or servo motors. With the additional features of the FTM, 3-phase motors, general purpose or stepper motors can be driven with a minimum amount of external components.

Table 5-17 FlexTimer Module Signals (Colibri family compatible interface)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
59	PWM<A>, Camera Input Data<7>	FTM0_CH0	I/O	3V3	FTM channel (PWM Output/ input capture/ output compare)
28	PWM<B>	FTM1_CH0	I/O	3V3	FTM channel (PWM Output/ input capture/ output compare)
30	PWM<C>	FTM0_CH1	I/O	3V3	FTM channel (PWM Output/ input capture/ output compare)
67	PWM<D>, Camera Input Data<6>	FTM1_CH1	I/O	3V3	FTM channel (PWM Output/ input capture/ output compare)

Table 5-18 FlexTimer Module Signals (additional, not compatible with other modules)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
24	Battery Fault Detect	FTM0_CH3	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
21	UART_C TXD	FTM0_CH4	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
19	UART_C RXD	FTM0_CH5	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
94	Camera Input HSYNC	FTM0_CH6	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
81	Camera Input VSYNC	FTM0_CH7	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
71	Camera Input Data<0>, LCD Back-Light GPIO	FTM1_CH0	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
98	Camera Input Data<1>	FTM1_CH1	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
106	GPIO	FTM3_CH0	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
69	GPIO	FTM3_CH1	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
99	GPIO	FTM3_CH2	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
104	GPIO	FTM3_CH3	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
107	GPIO	FTM3_CH4	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
127	GPIO	FTM3_CH5	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
184	GPIO	FTM3_CH6	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
186	GPIO	FTM3_CH7	I/O	3V3	FTM channel (PWM Output/ input capture / output compare)
28	PWM<B>	FTM1_QD_PHA	I	3V3	The Quadrature Decoder Phase A input
67	PWM<D>, Camera Input Data<6>	FTM1_QD_PHB	I	3V3	The Quadrature Decoder Phase B input

5.13 OWR (One Wire)

Colibri VFxx does not feature a One Wire interface.

5.14 SD/MMC

Colibri VFxx provides two SDIO interfaces. One interface is located on the standard SODIMM pins while the second interface is available on Colibri family incompatible SODIMM pins. The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, CE-ATA cards and eMMC devices. The SDIO interface on the Vybrid SoC uses the DAT3 pin for detecting whether a card is plugged in or not. Due to compatibility issues with the Colibri family, it is not possible to use this feature. Instead, a GPIO should be used to detect the presence of the card by connecting it to the card detect switch of the holder.

Features

- Supports SD Memory Card Specification 2.0
- Supports SDIO Card Specification Version 2.0
- Supports addressing high capacity SD 2.0 or SD-HC cards up to 32 GByte
- Supports SPI mode
- Up to 200Mbits per second data rate using 4 parallel data lines (SD 4-bit mode) at 50 MHz
- Up to 208Mbits per second data rate using 4 parallel data lines (MMC 4-bit mode) at 52 MHz
- The IO voltage is 3.3V on the SODIMM pins.

Table 5-19 SDIO Signals (Colibri family compatible interface)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
47	SDCard CLK	SDHC1_CLK	O	3V3	Serial Clock
190	SDCard CMD	SDHC1_CMD	I/O	3V3	Command
192	SDCard DAT<0>	SDHC1_DAT0	I/O	3V3	Serial Data 0
49	SDCard DAT<1>	SDHC1_DAT1	I/O	3V3	Serial Data 1
51	SDCard DAT<2>	SDHC1_DAT2	I/O	3V3	Serial Data 2
53	SDCard DAT<3>	SDHC1_DAT3	I/O	3V3	Serial Data 3
43	WAKEUP Source<0>, SDCard CardDetect	PTB20	I	3V3	Card Detect (standard GPIO)

Table 5-20 SDIO Signals (additional, not compatible with other modules)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
71	Camera Input Data<0>, LCD Back-Light GPIO	SDHC0_CLK	O	3V3	Serial Clock
98	Camera Input Data<1>	SDHC0_CMD	I/O	3V3	Command
101	Camera Input Data<2>	SDHC0_DAT0	I/O	3V3	Serial Data 0
103	Camera Input Data<3>	SDHC0_DAT1	I/O	3V3	Serial Data 1
79	Camera Input Data<4>	SDHC0_DAT2	I/O	3V3	Serial Data 2
97	Camera Input Data<5>	SDHC0_DAT3	I/O	3V3	Serial Data 3
67	PWM<D>,Camera Input Data<6>	SDHC0_WP	I	3V3	Write Protection (optional)
127	GPIO	SDHC1_WP	I	3V3	Write Protection (optional, not Colibri standard)

5.15 Analogue Audio (Colibri VF61 only)

Colibri VF61 features an Analogue Audio interface which is provided by the Wolfson WM9715L audio codec. The codec is connected over the AC97 interface to the Vybrid SoC. Please consult the Wolfson WM9715L datasheet for more information.

Table 5-21 Audio Interface Pins (VF61)

X1 Pin#	Colibri Signal Name	WM9715 Pin#	WM9715 Pin Name	I/O	Description
1	MIC_IN	21	MIC1	I	Microphone Input
3	MIC_GND	(28)	(MICBIAS)	O	Microphone pseudo-ground, is switched by using the MICBIAS output of the WM9715
5	LINEIN_L	23	LINE_IN_L	I	Left Line Input

X1 Pin#	Colibri Signal Name	WM9715 Pin#	WM9715 Pin Name	I/O	Description
7	LINEIN_R	24	LINE_IN_R	I	Right Line Input
13	HEADPHONE_GND	37	OUT3	O	Headphone pseudo-ground (do not connect to ground!)
15	HEADPHONE_L	39	HPOUT_L	O	Headphone Left Output
17	HEADPHONE_R	41	HPOUT_R	O	Headphone Right Output

5.16 DAC output (Colibri VF50 only)

Colibri VF50 features a digital-to-analogue converter (DAC) output on the pins of the headphone output instead of an analogue audio interface. The DAC can be used for low quality audio output due to the buffer and DMA function. The DAC output has a 1µF series capacitor between the Vybrid pin and the SODIMM connector. This allows for using the output as a DC-free audio output.

Features

- 2 Channels
- 12bit resolution
- 3.3V reference voltage
- 16-word data buffer
- DMA support
- Output load current maximum 1 mA

Table 5-22 DAC Signals (VF50)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Description
15	HEADPHONE_L	DACO0	O	Digital-to-analogue converter output 0
17	HEADPHONE_R	DACO1	O	Digital-to-analogue converter output 1
13	HEADPHONE_GND	(VSS_AUDIO)	O	Connected to the analogue ground of the module
1	MIC_IN	-	-	Not connected
3	MIC_GND	-	-	Not connected
5	LINEIN_L	-	-	Not connected
7	LINEIN_R	-	-	Not connected

5.17 Touch Panel Interface

The implementation of the resistive touch interface depends on the type of Colibri module. The VF61 module features the Wolfson WM9715L which provides the four wire touch interface. The touch interface of the VF50 module is provided by using the ADC and GPIO interfaces of the Vybrid SoC.

5.17.1 Colibri VF61 Touch Panel Interface

The Wolfson WM9715L audio codec provides the touch interface for the Colibri VF61 module. Please consult the Wolfson WM9715 documentation for more information.

Table 5-23 Touch Panel Interface Pins (VF61)

X1 Pin#	Colibri Signal Name	WM9715 Pin#	WM9715 Pin Name	I/O	Voltage Level	Description
14	TSPX	14	X+/BR	I/O	AVDD	X+ (4-wire)
16	TSMX	16	X-/TL	I/O	AVDD	X- (4-wire)
18	TSPY	15	Y+/TR	I/O	AVDD	Y+ (4-wire)
20	TSMY	17	Y-/BL	I/O	AVDD	Y- (4-wire)

5.17.2 Colibri VF50 Touch Panel Interface

Since the Colibri VF50 does not feature an audio codec, the touch interface is provided by using the internal ADC input of the Vybrid SoC. Some resistive touch panels require more current than the GPIO of the Vybrid allows to be drawn. Therefore, additional transistors are used for providing the higher current. The following figure shows the external circuit of the resistive touch interface on the module.

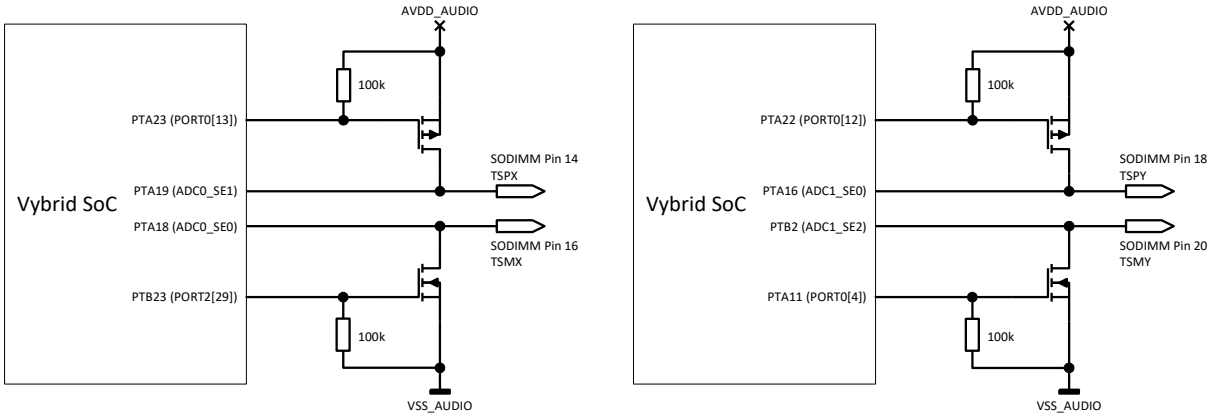

Figure 5 Colibri VF50 Touch Panel Interface Circuit

The touch panel interface of the Colibri VF50 is compatible with the four wire touch interface of the Colibri VF61 and the rest of the Colibri family.

Table 5-24 Touch Panel Interface Pins (VF50)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
14	TSPX	ADC0_SE1	I	AVDD	ADC input for X+ (Pin PTA19 of Vybrid)
		PTA23	O	AVDD	FET gate driver (GPIO register PORT0[13])
16	TSMX	ADC0_SE0	I	AVDD	ADC input for X- (Pin PTA18 of Vybrid)
		PTA12	O	AVDD	FET gate driver (GPIO register PORT0[5])
18	TSPY	ADC1_SE0	I	AVDD	ADC input for Y+ (Pin PTA16of Vybrid)
		PTA22	O	AVDD	FET gate driver (GPIO register PORT0[12])
20	TSMY	ADC1_SE2	I	AVDD	ADC input for Y- (Pin PTA11 of Vybrid)
		PTA11	O	AVDD	FET gate driver (GPIO register PORT0[4])

5.18 Analogue Inputs

The analogue-to-digital converter (ADC) input is provided by the Vybrid SoC. There are four analogue inputs available which are located at the standard SODIMM pins which are compatible within the Colibri family. These pins are dedicated as ADC inputs only. They cannot be configured for other functions like GPIO. Additional, some of the GPIO capable pins on the SODIMM connector feature as alternative function ADC capability. The ADC function of these pins is not compatible with other Colibri modules. It should also be noted that these signals are routed as digital signals on the module. Therefore, the noise level on these pins might be higher than on the dedicated ADC input signals.

The Vybrid SoC has two independent analogue-to-digital converters internally. Each of these converters is multiplexed to up to 10 external signal pads. Additionally, the converters can be multiplexed to measuring the internal temperature sensor, the DAC outputs or the reference voltage.

Features

- 2 independent ADC
- Linear successive approximation algorithm
- 12bit resolution with 10/11 bit accuracy
- 12bit, 10bit or 8bit output modes
- Up to 1MS/s sampling rate
- Configurable sample time and conversion speed
- Interrupt on conversion complete
- Asynchronous clock source for lower noise operation
- 3.3V reference voltage
- Input voltage level 0 to 3.3V
- Temperature sensor
- Hardware average function
- Self-calibration mode
- DMA

Table 5-25 Dedicated Analogue Input Signals (Colibri family compatible interface)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
8	Analogue Input <0>	ADC0_SE8	I	AVDD	Dedicated ADC input
6	Analogue Input <1>	ADC1_SE8	I	AVDD	Dedicated ADC input
4	Analogue Input<2>	ADC0_SE9	I	AVDD	Dedicated ADC input
2	Analogue Input<3>	ADC1_SE9	I	AVDD	Dedicated ADC input

Table 5-26 Analogue Input Signals (additional, not compatible with other modules)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
16	TSMX	ADC0_SE0	I	AVDD	ADC input (only available on Colibri VF50)
14	TSPX	ADC0_SE1	I	AVDD	ADC input (only available on Colibri VF50)
59	PWM<A>, Camera Input Data<7>	ADC0_SE2	I	AVDD	ADC input
30	PWM<C>	ADC0_SE3	I	AVDD	ADC input
21	UART_C TXD	ADC0_SE4	I	AVDD	ADC input
95	GPIO	ADC0_SE5	I	AVDD	ADC input
18	TSPY	ADC1_SE0	I	AVDD	ADC input (only available on Colibri VF50)
134	GPIO	ADC1_SE1	I	AVDD	ADC input

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
20	TSMY	ADC1_SE2	I	AVDD	ADC input (only available on Colibri VF50)
24	Battery Fault Detect	ADC1_SE3	I	AVDD	ADC input
19	UART_C RXD	ADC1_SE4	I	AVDD	ADC input
22	VDD_FAULT/SENSE	ADC1_SE5	I	AVDD	ADC input

5.19 Parallel Camera Interface

The Video-In (VIU3) subsystem can receive data from TV decoder chips, camera sensors and other video devices. The parallel camera interface pins are located on Colibri family compatible SODIMM connector pins. However, the supported input formats and signal mapping is possibly different from other Colibri modules. Please compare the datasheets of the modules to verify compatibility.

Some cameras require a master clock signal. The Colibri family normally provides a clock output at pin 75 of the SODIMM connector. Unfortunately, on the Colibri VFxx, this pin is not able to output a master clock signal. If the camera requires a clock signal, either use an external oscillator or use one of the other SODIMM pins of the Colibri VFxx which do have clock output functionality. More information about the available clock output pins can be found in section 0.

Features

- RGB888 (3 cycles), ITU656 10bit and ITU656 8bit compatible
- QVGA to XVGA resolutions
- Up to 1/8 video down-scaling on horizontal and vertical direction
- Up to 2/1 horizontal video up-scaling
- Horizontal mirroring
- Brightness and contrast adjust
- RGB to YUV conversion
- YUV to RGB conversion
- Simple de-interlace function
- Internal DMA
- Max pixel clock input 64MHz

Table 5-27 -Parallel Camera Interface Pins

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	RGB888 3 cycle	ITU656 10bit	ITU656 8bit
65	Camera Input Data<9>, Keypad_Out<3>	VIU_DATA9	I	3V3	—	Y9/C9	Y7/C7
85	Camera Input Data<8>, Keypad_Out<4>	VIU_DATA8	I	3V3	—	Y8/C8	Y6/C6
59	PWM<A>, Camera Input Data<7>	VIU_DATA7	I	3V3	R7/G7/B7	Y7/C7	Y5/C5
67	PWM<D>,Camera Input Data<6>	VIU_DATA6	I	3V3	R6/G6/B6	Y6/C6	Y4/C4
97	Camera Input Data<5>	VIU_DATA5	I	3V3	R5/G5/B5	Y5/C5	Y3/C3
79	Camera Input Data<4>	VIU_DATA4	I	3V3	R4/G4/B4	Y4/C4	Y2/C2
103	Camera Input Data<3>	VIU_DATA3	I	3V3	R3/G3/B3	Y3/C3	Y1/C1
101	Camera Input Data<2>	VIU_DATA2	I	3V3	R2/G2/B2	Y2/C2	Y0/C0
98	Camera Input Data<1>	VIU_DATA1	I	3V3	R1/G1/B1	Y1/C1	—
71	Camera Input Data<0>, LCD Back-Light GPIO	VIU_DATA0	I	3V3	R0/G0/B0	Y0/C0	—
96	Camera Input PCLK	VIU_PIX_CLK	I	3V3	CLK	CLK	CLK

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	RGB888 3 cycle	ITU656 10bit	ITU656 8bit
94	Camera Input HSYNC	VIU_HSYNC	I	3V3	HSYNC	—	—
81	Camera Input VSYNC	VIU_VSYNC	I	3V3	VSYNC	—	—

Two additional camera interface signals can be found on alternative functions on some SODIMM pins. The pins can only be used in the RGB888 mode and are not compatible with other Colibri modules.

Table 5-28 –Additional Parallel Camera Interface Pins

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
35	UART_A TXD	VIU_DE	I	3V3	Data Enable (optional)
19	UART_C RXD			3V3	
28	PWM<B>			3V3	
21	UART_C TXD	VIU_FID	I	3V3	Field Identification (optional, identification of the upper or lower field for interlaced input formats)
77	GPIO			3V3	

5.20 Analogue Video ADC inputs (Colibri VF61 only)

Colibri VF61 features four analogue video inputs. The inputs accept PAL or NTSC composite video signals. The analogue to digital converter provides YUV888-formatted data to the video interface unit (VIU). The following figure shows the multiplexing schema for the video input system.

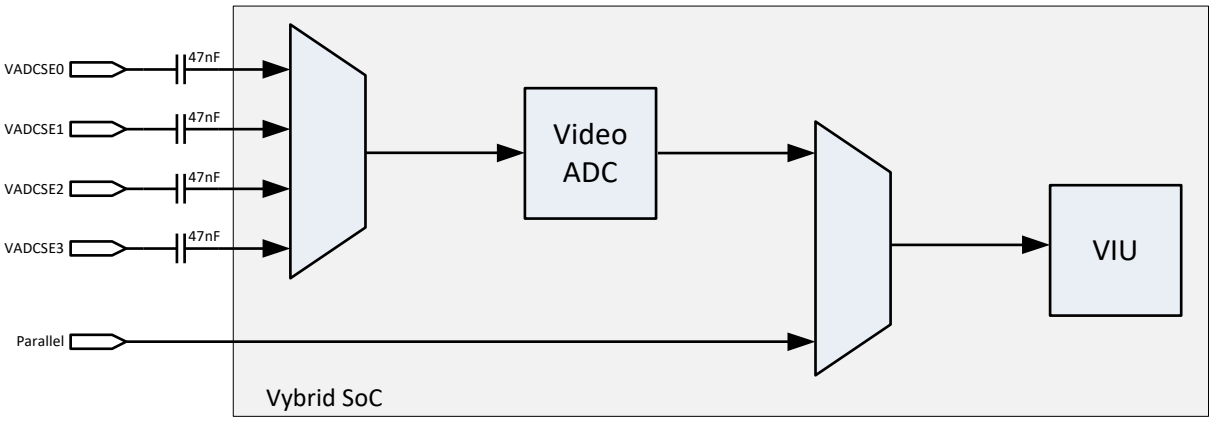

Figure 6 Colibri VF61 Video Input Multiplexing Schema

These analogue video inputs are not available on other Colibri modules. Therefore, the interface is not compatible with the Colibri family. The input signals are placed on unused SODIMM pins of the VF61. These pins are used for the external memory bus on some modules while other modules provide GPIO functionality on these pins. Since the analogue video signals are only inputs and series capacitors of 47nF are placed between the SODIMM connector and Vybrid pins, there are no electrical issues known when the module is placed on a carrier board which uses these pins for the external memory bus.

Features

- 10bit resolution
- CVBS format
- Programmable anti-aliasing filter, gain and clamp
- PAL and NTSC decoder
- Automatic standards detection
- 2D adaptive comb filter
- Time base correction for VCR signals
- Luma pass band is flat to >6MHz

Table 5-29 Analogue Video Input Signals (Colibri VF61 only)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Description
162		VADCSE0	I	Composite video input 0
164		VADCSE1	I	Composite video input 1
166		VADCSE2	I	Composite video input 2
168		VADCSE3	I	Composite video input 3

5.21 S/PDIF (Sony-Philips Digital Interface I/O)

The Vybrid SoC features an S/PDIF input as well as an output interface. The interface can be used to transmit and receive digital audio. The interface is compatible with the AES/EBU IEC 60958 standard and Tech 3250-E with some exceptions. For more information about the limitation, please consult the reference manual for the Vybrid SoC.

The S/PDIF signals are not located on SODIMM connector pins as secondary functions. The location is not compatible with other Colibri modules.

Table 5-30 S/PDIF Signals (not compatible with other modules)

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
36	UART_B RXD	SPDIF_IN1	I	3V3	Serial Data Input
34	UART_B RTS	SPDIF_OUT1	O	3V3	Serial Data Output

5.22 Audio Codec Interfaces

5.22.1 Synchronous Audio Interface (SAI)

The Synchronous Audio Interface (SAI) allows connecting I²S or AC97 audio codecs. The Wolfson W9715L audio codec of the Colibri VF61 is connected over the SAI2 to the Vybrid SoC. At the SODIMM connector, the SAI3 is available as a secondary function. The pins locations are not compatible with the rest of the Colibri family.

Features

- Maximum frame size 32 words
- Word size between 8bit and 32bit
- Asynchronous 32x32bit FIFO for each transmit and receive channel
- DMA support

Table 5-31 SAI Signals

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
192	SDCard DAT<0>	SAI3_TX_BCLK	O	3V3	Transmit Bit Clock
53	SDCard DAT<3>	SAI3_TX_DATA	O	3V3	Transmit Data
29	UART_A DSR	SAI3_TX_SYNC	O	3V3	Transmit Frame Sync
49	SDCard DAT<1>	SAI3_RX_BCLK	I	3V3	Receive Bit Clock
51	SDCard DAT<2>	SAI3_RX_DATA	I	3V3	Receive Data
37	UART_A RI, Keypad_In<4>	SAI3_RX_SYNC	I	3V3	Receive Frame Sync
65	Camera Input Data<9>, Keypad_Out<3>	CKO1	O	3V3	Audio Master Clock

Table 5-32 Typical usage of SAI

X1 Pin#	Vybrid Signal Name	I2S Codec	I/O	Voltage Level	AC97 Codec
192	SAI3_TX_BCLK	I2S_SCLK	O	3V3	AC97_BIT_CLK
53	SAI3_TX_DATA	I2S_DOUT	O	3V3	AC97_SDATA_OUT
29	SAI3_TX_SYNC	I2S_LRCLK	O	3V3	AC97_SYNC
49	SAI3_RX_BCLK	-	I	3V3	-
51	SAI3_RX_DATA	I2S_DIN	I	3V3	AC97_SDATA_IN
37	SAI3_RX_SYNC	-	I	3V3	-
65	CKO1	SYS_MCLK	O	3V3	AC97_MCLK

5.22.2 Enhanced Serial Audio Interface (ESAI)

The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices such as audio codecs, S/PDIF transceivers or DSPs. The Vybrid SoC features up to 12 pins for connecting the ESAI to an external device. 8 of these pins are available externally as secondary functions of the SODIMM pins. Most peripherals do not require the missing RX bit clock, RX frame sync or the high frequency RX and TX clock signals. Please check the datasheet of the peripheral to see which signals are required. The ESAI interface is not compatible with other Colibri modules.

Features

- Up to six transmitters and four receivers
- Programmable word length (8, 12, 16, 20, 24bits)
- AC97 and I²S support
- 128 word transmit FIFO shared by six transmitter
- 128 word receive FIFO shared by four receivers

Table 5-33 ESAI Signals

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
98	Camera Input Data<1>	ESAI_FST	O	3V3	Frame sync for transmitter and receivers in synchronous mode and for the transmitter in asynchronous mode
71	Camera Input Data<0>, LCD Back-Light GPIO	ESAI_SCKT	I/O	3V3	Transmit serial bit clock, direction can be programmed
101	Camera Input Data<2>	ESAI_SDO0	O	3V3	Serial transmit data 0
103	Camera Input Data<3>	ESAI_SDO1	O	3V3	Serial transmit data 1
79	Camera Input Data<4>	ESAI_SDO2/ ESAI_SDI3	I/O	3V3	Serial transmit data 2 or serial receive data 3
97	Camera Input Data<5>	ESAI_SDO3/ ESAI_SDI2	I/O	3V3	Serial transmit data 3 or serial receive data 2
59	PWM<A>, Camera Input Data<7>	ESAI_SDO4/ ESAI_SDI1	I/O	3V3	Serial transmit data 4 or serial receive data 1
67	PWM<D>, Camera Input Data<6>	ESAI_SDO5/ ESAI_SDI0	I/O	3V3	Serial transmit data 5 or serial receive data 0

5.23 Clock Output

Colibri VFxx provides two general purpose external clock signals (CKO) which are accessible through three SODIMM pins. The location of these pins is not compatible with the Colibri family.

Additional to the general purpose clock outputs, the module features dedicated clock outputs for example for the RMII or audio interface. Please check the relevant sections in this document for more information about the dedicated clock output signals.

The general purpose clock outputs can be sourced from a large variety of internal clock sources and PLLs. In addition, it is possible to set an individual divider value from 1 to 16. Therefore, the CKO pins can also be used for observing the internal clocks.

Table 5-34 Clock Output Signals

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
65	Camera Input Data<9>, Keypad_Out<3>	CKO1	O	3V3	General Purpose Clock Output 1
35	UART_A TXD			3V3	
33	UART_A RXD	CKO2	O	3V3	General Purpose Clock Output 2

5.24 Keypad

You can use any free GPIOs to realize a Matrix keypad interface.

5.25 CAN

Colibri VFxx features two Controller Area Network (CAN) interfaces. The interface is located as secondary functions on the SODIMM pins. The interface is therefore not compatible with all the modules in the Colibri family. If only one CAN interface is required, the interface on Pin 63/55 is preferable since it is compatible with the Colibri iMX6 modules. In order to be compliant with the CAN standard, a transceiver on the carrier board is required.

Features

- Full implementation of the CAN protocol version 2.0B
- Bit rate up to 1Mb/s
- Flexible mailboxes of 0 to 8 bytes data length
- 6 frames receive FIFO
- Listen-only mode
- Programmable transmission priority scheme
- 16bit free running time stamp timer
- Short latency
- Receive FIFO ID filtering

Table 5-35 CAN Signals

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
63	GPIO	CAN1_RX	I	3V3	CAN receive pin, compatible with Colibri iMX6
55	GPIO	CAN1_TX	O	3V3	CAN transmit pin, compatible with Colibri iMX6
196	I2C SCL	CAN0_RX	I	3V3	CAN receive pin
194	I2C SDA	CAN0_TX	O	3V3	CAN transmit pin

5.26 JTAG

There is a JTAG interface available on PCB test points. On the Evaluation Board 3.1 the signals are accessible through the pogo pins. The reference voltage is 3.3V, hence jumper JP 29 must be in position 2-3.

A JTAG interface is not required to work with the Colibri VFxx. You should always be able to reprogram the module via Recovery Mode (serial downloader).

6 Recovery Mode

The UART_A (SCI0) can be used to download new software. This is normally only required if the Bootloader does not boot anymore. In the Freescale documentation of the Vybrid the recovery mode is also called serial downloader.

To enter the recovery mode, either connect the recovery mode pads on the front of the module together (see picture below) or pull SODIMM pin 91 to GND with a 10KOhm resistor while power up the module. If the Colibri Evaluation Board V3.x is used, the SW9 button can be pressed during switching on the power supply for the module.

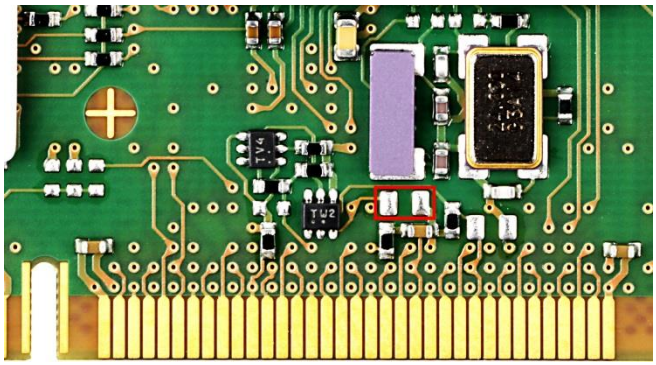

Figure 7 Location of recovery mode pads

The serial loader requires hardware flow control signals RTS/CTS. Enable the hardware flow control in your RS232 host adapter or short the two signals on the carrier board. You can find additional information in our Developer Centre:
http://developer.toradex.com/knowledge-base/vfxx-recovery-mode

7 Bootstrap Options

The Vybrid SoC has several different boot modes (BOOT_MODE[1:0]). The VFxx knows the following boot modes:

Table 7-1 Boot Mode Pins

BOOT_MODE1	BOOT_MODE0	Boot Type
0	0	Boot from fuse settings (default)
0	1	Serial Downloader (Recovery Mode)
1	0	Boot with RCON strapping pin settings (not available)

The module boots by default with the fused RCON settings (BOOT_MODE[1:0] = 00). The fuse settings are configured to boot the module from the internal NAND flash.

As described in the previous section, the Colibri module can be set into the recovery mode. If pin 91 of the SODIMM connector is pulled down during the power up sequence an internal circuit sets the boot mode to the serial downloader (BOOT_MODE[1:0] = 01).

The boot mode "Boot with RCON strapping pin settings" is not available for the Colibri VFxx modules, since the modules are fused. The Freescale documentation of the SoC can be a little confusing, but this boot mode is only available if the SoC is not fused.

Table 7-2 BOOT_MODE Strapping Signals

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	Voltage Level	Description
82	LCD RGB VSYNC	BOOTMOD0	I	3V3	Internally pulled down with 10kΩ
68	LCD RGB HSYNC	BOOTMOD1	I	3V3	Internally pulled down with 10kΩ

Use the VSYNC and HSYNC signals with caution. Make sure that the signals are not pulled up externally during the power up cycle of the module. Therefore, we recommend adding buffers to the sync signals on the carrier board. The Colibri Evaluation board V3.x and all versions of the Iris Carrier board feature such buffers. The older carrier boards, such as the Colibri Evaluation board V2.x connect the sync signals directly to the VGA and LCD display connectors. This can lead to problems if a monitor or display pulls up these signals.

8 Suspend

The Vybrid SoC on the Colibri VFxx has several different suspend modes which help to reduce the power consumption of the module. The following suspend modes are supported:

Table 8-1 Suspend Modes

Name	Description
Run	Device operates at the highest specified frequency, all peripherals are operational.
Wait	The device waits for an interrupt. The A5, the M4 or both cores are halted. The normal recovery is from an interrupt.
LPRun	Low Power Run mode is a dynamic power-saving mode. The running clocks are scaled down to lower frequencies.
ULPRun	Ultra-Low Power Run mode is an extension of the LPRun mode. The clock frequencies are scaled down to 32kHz or 128kHz
Stop	Lowest power mode in which all power rails are retained. Clocks to the peripherals are gated by the clock control module (CCM). SRAM contents are retained.
LPStop3	Selected power rails are switched off (e.g.1.2V Core is switched off). First 64K SRAM is retained
LPStop2	Selected power rails are switched off (e.g.1.2V Core is switched off). First 16K SRAM is retained
LPStop1	Selected power rails are switched off (e.g.1.2V Core is switched off). SRAM content is lost
VBAT	Only the RTC battery voltage (VCC_BATT) is available. The module main power (3V3) is not available. Only RTC is running

Since the normal GPIO pins lose their state in LPStop3 mode and lower, only the pins which are wake up capable can generate an interrupt which will wake up the system. More information about these wakeup sources can be found in section 5.2.1 of this document.

The DDR3 RAM on the module is powered in all states (except VBAT state) and retains its contents if it goes into the self-refresh operation. More information about the suspend mode can be found in the reference manual of the Freescale Vybrid SoC.

*Vybrid modules prior to version 1.2A do not support suspend.

9 Known Issues

The USB serial downloader is not working. If the Bootloader needs to be recovered, use the UART_A serial loader or the JTAG interface.

10 Technical Specifications

10.1 Absolute Maximum Rating

Table 10-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
Vmax_3V3	Main Module Supply	-0.3	3.6	V
Vmax_AVDD	Analogue Supply	-0.3	3.6	V
Vmax_VCC_BATT	RTC Supply	-0.3	3.6	V
Vmax_IO	Most pins with GPIO functions	-0.5	3V3+0.3V	V
Vmax_AIN	Analog Input	-0.3	AVDD+0.3V	V
Vmax_USB	USB Voltage	-0.5	5.25	V

10.2 Recommended Operating Conditions

Table 10-2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
3V3	Digital Supply	3.135	3.3	3.465	V
AVDD	Analog Supply	3.0	3.3	3.6	V
VCC_BATT	RTC Supply	2.4	3.3	3.6	V

10.3 Electrical Characteristics

Table 10-3 Typical Power Consumption Colibri VF50

Symbol	Description (VCC=3.3V)	Typ	Unit
IDD_IDL	CPU Idle	202	mA
IDD_HIGHCPU	Maximal CPU Load	233	mA
IDD_SUSPEND	Module in Suspend State	49	mA

Table 10-4 Typical Power Consumption Colibri VF61

Symbol	Description (VCC=3.3V)	Typ	Unit
IDD_IDL	CPU Idle	233	mA
IDD_HIGHCPU	Maximal CPU Load (A5 and M4 full load)	278	mA
IDD_HIGHCPUA5	Maximal CPU Load A5, M4 in idle	278	mA
IDD_SUSPEND	Module in Suspend State	51	mA

10.4 Power-Up Ramp Time Requirements

TBA

10.5 Mechanical Characteristics

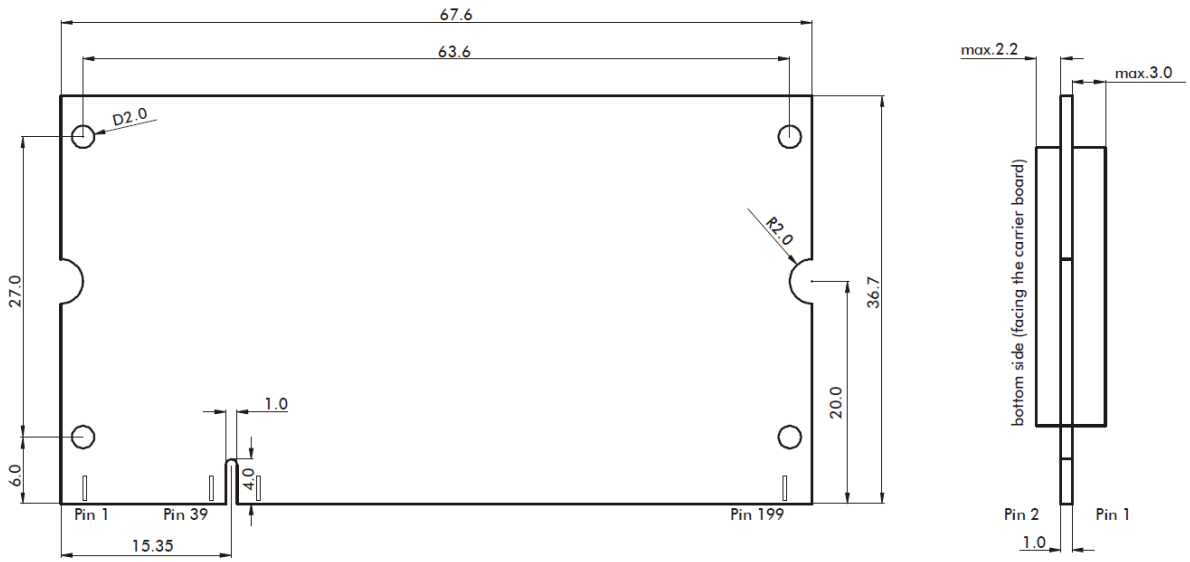

Figure 8 Mechanical dimensions of the Colibri modules
Tolerance for all measures: +/- 0.1mm

10.5.1 Sockets for the Colibri Modules

The Colibri modules fit into a regular 2.5V (DDR1) SODIMM200 memory socket.
A selection of SODIMM200 socket manufacturers is detailed below:

AUK Connectors:	http://www.aukconnector.com/
CONCRAFT:	http://www.concraft.com.tw/connector_products.html
Morethanall Co Ltd.:	http://www.morethanall.com/
Tyco Electronics (AMP):	http://www.te.com/usa-en/home.html
NEXUS COMPONENTS GmbH	https://www.nexus-de.com/en

10.6 Thermal Specification

Table 10-5 1.1 Thermal Specification

Module	Description	Min	Typ	Max	Unit
Colibri VFxx	Operating temperature range	0		70	°C
Colibri VFxx IT	Operating temperature range	-40		85	°C
Colibri VFxx Colibri VFxx IT	Storage Temperature	-55		100	°C
Colibri VFxx Colibri VFxx IT	Thermal Design Power at max Temperature Vybrid Chip and DDR RAM		TBA		W
Colibri VFxx Colibri VFxx IT	Thermal Resistance Junction-to-Ambient, Vybrid Chip only. (Theta-JA) [1]		28		°C/W
Colibri VFxx Colibri VFxx IT	Thermal Resistance Junction-to-Case, Vybrid Chip only. (Theta-JC) [1]		10		°C/W
Colibri VFxx Colibri VFxx IT	Thermal Resistance Junction-to-Top of Package, Vybrid Chip only, (Psi-JT) [1]		2		°C/W

[1] A High K JEDEC four layer Board as defined by JEDEC Standard JESD51-6, board mounted horizontal, natural convection.

10.7 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH etc. can be found on our website at:
http://www.toradex.com/support/product-compliance

DISCLAIMER: