FUJITSU SEMICONDUCTOR
DATA SHEET

MDD1)11-112-01

32-bit Microcontroller

FR Family FR81S

MB91570 Series DS Major Changes

MB91F575B/F575BS/F575BH/F575BHS
MB91F577B/F577BS/F577BH/F577BHS

This material covers the major changes from DS705-00009-0v01 to DS705-00009-1v0.

2012.01.11

■ MAJOR CHANGES MADE IN THIS EDITION

Page	Section	Change Results
-	General	The following products are added. MB91F575B/F575BS/F575BH/F575BHS MB91F577B/F577BS/F577BH/F577BHS
1	■FEATURES	Descriptions are changed.
4	■FEATURES ●Peripheral Functions	Names of the following item are corrected. ·Up/Down counter ↓ ·Up/Down counter: 2 channels ·Power on reset / internal low-voltage detection reset ↓ ·Power on reset ·Low-voltage detection reset ↓ ·Low-voltage detection reset (external low-voltage detection) ·Low-voltage detection reset (internal low-voltage detection)
4 5, 37	■FEATURES●Peripheral Functions, ■PRODUCT LINEUP ■BLOCK DIAGRAM	·HS-SPI Note: In this series, the HS-SPI function is prohibited
5, 6	■PRODUCT LINEUP	Product lineup is changed in accordance with addition of those products.
		Items added ·Sub clock Item names corrected ·DMA Transfer → DMA Controller ·16-bit Base Timer → Base Timer (16bit) ·Free-run Timer → Free-run Timer (32bit) ·Input capture → Input capture (32bit) ·Output Compare → Output Compare (32bit) ·16-bit Reload timer → Reload Timer (16bit) ·PPG → PPG timer (16bit) ·D/A → D/A converter ·A/D → A/D converter(8bit/10bit) ·Multi-Function → Multi-Function serial communication ·Internal low-voltage detection reset → Low-voltage detection reset (Internal low-voltage detection) ·On Chip Debug: Built-in OCD →·On Chip Debug: Yes

Page	Section	Change Results
19, 20, 23	■PIN DESCRIPTION	Terminologies are unified ·DEBUG I/F → DEBUG I/F pin ("pin" is added) ·##Power Supply → ##Power Supply pin ("pin" is added) ·##GND → ##GND pin ("pin" is added) ·##Reference Voltage → ##Reference Voltage pin ("pin" is added) ·OSC Input pin, OSC Output pin → oscillation Input pin, oscillation Output pin
20		The function of MD0 of pin number 114 is changed. Mode Pin → Mode Pin 0
20		The function of MD1 of pin number 115 is changed. Mode Pin → Mode Pin 1
20		The I/O circuit type and function of MD2 of pin number 116 are changed. A → R2 Mode Pin → Mode Pin 2
23		The function description of AVSS/AVRL of pin number 82 is changed. ADC GND / Low Reference Voltage ↓ ADC, DAC GND pin/ Low Reference Voltage pin
24-26	■ I/O CIRCUIT TYPE	As to the I/O circuit types, H, I, I2, I3, J, K, L, M, and N, · The circuit diagrams are corrected. (The hysteresis symbol on TTL is deleted.)
27		As to the I/O circuit type B, ·The circuit diagram is corrected. (The hysteresis symbol on TTL is deleted.)
27		The I/O circuit type, R2, is added.
27		Remarks for X and Y in the I/O CIRCUIT TYPE are the same as those of other series of the devices. Main clock → Main oscillation I/O Sub clock → Sub oscillation I/O

Page	Section	Change Results
37	■BLOCK DIAGRAM	Name of the on-chip Flash Memory is corrected. Work Flash → WorkFlash (No space between letter k and F) Names of the I/O pins of CAN are corrected. CANRX0-2, CANTX0-2 → RX0-2, TX0-2 Names of the I/O pins of A/D converter are corrected. ADTG, AN0-40 ↓ ADTG, AN0-39 The following is added to I/O pins of A/D converter. ADC enabled (ADER) Description of the Low Voltage Detection is corrected. Low Voltage Detection ↓ Low Voltage Detection (External Power Supply) Low Voltage Detection (Internal Power Supply)
38, 39	■MEMORY MAP	The memory map is changed in accordance with addition of those products.
41	■I/O MAP	The data access attribute of address 000044_H DICR is corrected. B,H,W → B
49		The address 000318_H IPVAR is deleted.
		The address $00031E_H$ IPVSR is deleted.
55, 76		The data access attribute and initial value of the address $00056D_H$ CSVCR are corrected as shown below. Data access attribute: B,H,W → B Initial value: -001110- → -001110-, -001010-*3 *3: The initial value is different by part number. For details, refer to the CSVCR register in chapter "Clock Supervisor"
81	■ELECTRICAL CHARASTERISTICS 1. Absolute Maximum Ratings	Assignment of the corresponding pins described in note *8 are corrected. P050 to P056 → P050 to P053
83	3.DC characteristics	Description of conditions for V_{IH2}, V_{IH6} are corrected CMOS schmitt → CMOS hysteresis
		Description of V_{IH12} (Pin name: X0, X1, X0A, X1A) are deleted.

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84	3.DC characteristics	Pin name of V_{IL5} to V_{IL8} are corrected. P036 → P037
		Minimum value of V_{IL9}, V_{IL10}, V_{IL11} are corrected. V_{SS} → V_{SS}-0.3
		Maximum value of V_{IL10} is corrected. $0.5\times V_{CC}5$→ $0.3\times V_{CC}5$
		Maximum value of V_{IL11} is corrected. $0.5\times V_{CC}5$ → 0.8
		Description of V_{IL12} (Pin name: X0, X1, X0A, X1A) are deleted.
85		Condition of V_{OH1}, V_{OH2}, V_{OH3} are corrected. $V_{CC}E$ = 3.3V → $V_{CC}E$ = 3.0V
86		Condition of V_{OL1}, V_{OL2}, V_{OL3} are corrected. $V_{CC}E$ = 3.3V → $V_{CC}E$ = 3.0V
		Pin name of $V_{OL4,}$ V_{OL5} are corrected. P036 → P037
89		Name of the on-chip Flash Memory is corrected. work flash → WorkFlash (No space between letter k and F)
90	■ ELECTRICAL CHARASTERISTICS 4. AC characteristics (1) Main Clock Timing	The minimum value of the Internal operating clock cycle time, F_{CP}, F_{CPP}, $F_{CPT,}$ is determined. - → 2 (MHz)
		The maximum value of the Internal operating clock cycle time, t_{CP}, t_{CPP}, $t_{CPT,}$ is determined. - → 500 (ns)
91	(1-2) Sub Clock Timing	Comment on a part number of the products is added. (1-2) Sub clock timing ↓ (1-2) Sub clock timing (products without S-suffix)
92	•Guaranteed operation range	The following note is added: Note: The CPU will be reset at the power supply voltage 4V±0.3V or less.
92	•Example of an oscillation circuit	Capacitance of the C1 and C2 in the circuit diagram is corrected. C1=27pF → 10pF C2=27pF → 10pF The following note is added: Note: As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation. Design your print circuit board so that the oscillator can start oscillation within 20ms.

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95	■ ELECTRICAL CHARASTERISTICS 4. AC characteristics (3) Power-on Conditions	The table (3) Power-on Conditions is corrected. The descriptions of the following parameters are deleted: Power supply on rise time, Power supply start voltage, and Power supply peak voltage. Descriptions of the following parameters are added: Level detection voltage, Level detection hysteresis width, Level detection time, and Slope detection undetected standard.
95		The item number of the notes under the table of (3) Power-on Conditions is corrected. *: This time is to start the slope detection··· ↓ *3: This time is to start the slope detection··· The following are added under the table (3) Power-on Conditions. *1: If the fluctuation of the power supply is faster than the low voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range. *2: When setting the power supply fluctuation to this standard or less, it is possible to suppress the slope detection. This is the standard when the power supply fluctuation is stable.
95		The diagram under the table (3) Power-on Conditions is deleted.
96	■ ELECTRICAL CHARASTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1)UART timing	The following is added to the Bit setting in (4-1) UART timing: SCR:SPI=0 Table in (4-1) UART timing is changed. Parameter: [Valid SIN→SCK↑] → [Valid SIN→SCK↑setup time] (t_{IVSHI}, t_{IVSHE}) Remarks: Internal shift clock mode output pin : C_L=50pF ↓ Internal shift clock mode: C_L=50pF (When drive capability is 2mA or more.) C_L=20pF (When drive capability is 1mA) External shift clock mode output pin : C_L=50pF ↓ External shift clock mode: C_L=50pF (When drive capability is 2mA or more.) C_L=20pF (When drive capability is 1mA)

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98	■ ELECTRICAL CHARASTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1)UART timing	The following is added to the Bit setting in (4-1) UART timing: SCR:SPI=0 Table in (4-1) UART timing is changed. Parameter: [Valid SIN→ SCK ↓] is corrected to [Valid SIN→ SCK ↓ setup time] (t_{IVSLI} , t_{IVSLE}) Remarks: Internal shift clock mode output pin : C_L=50pF ↓ Internal shift clock mode: C_L=50pF (When drive capability is 2mA or more.) C_L=20pF (When drive capability is 1mA) External shift clock mode output pin : C_L=50pF ↓ External shift clock mode: C_L=50pF (When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)
99	(4) Multi-function Serial (4-1)UART timing	The diagram, External shift clock mode, in (4-1) UART timing is corrected. Serial clock “L” pulse width t_{SLSH} which a double-headed arrow shows is corrected from the interval between V_{IL}-V_{IH} to V_{IL}-V_{IL}.
100, 101	(4) Multi-function Serial (4-1)UART timing	In (4-1) UART timing, the following bit setting is added: Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=0, SCR:SPI=1
102, 103	(4) Multi-function Serial (4-1)UART timing	In (4-1) UART timing, the following bit setting is added: Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=1, SCR:SPI=1
104	(4) Multi-function Serial (4-2) External clock (EXT=1)	(4-2)External clock (EXT = 1): asynchronous only Is added.

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105	(4-3) I^2C timing	In (4-3) I^2C timing, the following is corrected: The title number is corrected as shown below. (4-2) I^2C timing → (4-3) I^2C timing One of the symbols is corrected as shown below. t_{BUS} → t_{BUF} Condition of Noise filter is corrected to [-]. Conditions: C_L=50pF → C_L=50pF (When drive capability is 2mA or more.) C_L=20pF (When drive capability is 1mA.) The first note “*1” under the table is corrected as shown below: *1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA output lines. ↓ *1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines.
107	(5)LIN-UART timing	In the bit setting, ESCR: SCES=0 & ECCR: SCDE=0, the following are corrected. Parameter: [Valid SIN→SCK↑] → [Valid SIN→SCK↑setup time] (t_{IVSHI}, t_{IVSHE}) Parameters and symbols are corrected as shown below. Serial clock "H" pulse width, t_{SHSL} ↓ Serial clock "L" pulse width, t_{SLSH} Serial clock "L" pulse width, t_{SLSH} ↓ Serial clock "H" pulse width, t_{SHSL} Remarks: Internal shift clock mode output pin: C_L=80pF+1·TTL ↓ Internal shift clock mode: C_L=80pF+1·TTL External shift clock mode output pin: C_L=80pF+1·TTL ↓ External shift clock mode: C_L=80pF+1·TTL

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109	(5)LIN-UART timing	In the bit setting, ESCR: SCES=1 & ECCR: SCDE=0, the following are corrected. Parameter: [Valid SIN→SCK ↓] → [Valid SIN→SCK ↓setup time] (t_{IVSLI}, t_{IVSLE}) Remarks: Internal shift clock mode output pin: C_L=80pF+1·TTL ↓ Internal shift clock mode: C_L=80pF+1·TTL External shift clock mode output pin: C_L=80pF+1·TTL ↓ External shift clock mode: C_L=80pF+1·TTL
110	(5)LIN-UART timing	The diagram, External shift clock mode, in (5)LIN-UART timing is corrected. Serial clock “L” pulse width t_{SLSH} which a double-headed arrow shows is corrected from the interval between V_{IL}-V_{IH} to V_{IL}-V_{IL}.
111	(5)LIN-UART timing	In the bit setting, ESCR: SCES=0 & ECCR: SCDE=1, the following are corrected. Parameter: [Valid SIN→SCK ↓] → [Valid SIN→SCK ↓setup time] (t_{IVSLI}) Remarks: Internal shift clock mode output pin: C_L=80pF+1·TTL ↓ Internal shift clock mode: C_L=80pF+1·TTL The figure title is added to the timing chart. ·Internal shift clock mode

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112	(5)LIN-UART timing	In the bit setting, ESCR: SCES=1 & ECCR: SCDE=1, the following are corrected. Parameter: [Valid SIN→SCK↑] → [Valid SIN→SCK↑setup time] (t_{IVSHI}) Remarks: Internal shift clock mode output pin: C_L=80pF+1·TTL ↓ Internal shift clock mode: C_L=80pF+1·TTL The figure title is added to the timing chart. ·Internal shift clock mode
115	■ ELECTRICAL CHARASTERISTICS 4. AC characteristics (9) Low voltage detection (External low-voltage detection)	The title name is corrected as shown below. (9) Low voltage detection ↓ (9) Low voltage detection (External low-voltage detection) The specification table of (9) Low voltage detection (External low-voltage detection) is corrected. The figure under the specification table of (9) Low voltage detection (External low-voltage detection) is deleted. The parameter "Power-supply voltage fluctuation rate" and its note (*2) are added.
116	(10) Low voltage detection (Internal low-voltage detection)	The title name is corrected. (10) Internal low voltage detection ↓ (10) Low voltage detection (Internal low-voltage detection) The specification table of (10) Low voltage detection (Internal low-voltage detection) is corrected. The figure under the specification table of (9) Low voltage detection (Internal low-voltage detection) is deleted.
128	■ ELECTRICAL CHARASTERISTICS 5. A/D converter	The specification of the analog port input current I_{AIN} is determined. Min. - → -5 (μA) Max. 10 → +5 (μA) The note under the table is corrected. Note: Be sure to use the clock with a frequency between 8MHz and 17MHz for the ADC compare clock in order to ensure its accuracy.

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130	■ ELECTRICAL CHARASTERISTICS 5. A/D converter	In the diagram of an analog circuit model, part numbers and the maximum value of C are corrected. MB91F575/MB91F577 → MB91570series C = 15pF(MAX) ↓ C = 16.5pF(MAX)* *: except DA shared pin
131	6. D/A converter	The remark about the reference voltage supply current, $I_{DVR,}$ is corrected. Per 1ch → Per 1ch* The following note is added below the specification table. *: Reference voltage supply current (V_{CC} = AV_{CC} = 5.0 V) is specified.
132	7. Flash memory	The values of the following items in the specification table are corrected. · Sector erase time · Erase cycle/Data retain time Remarks and notes are corrected. The title "(1) Electrical characteristics" are put on the specification table. Notes for power-off during Flash writing are added as (2).
133	■Ordering part number	Ordering part numbers are changed in accordance with the additions to our product lineup.