Application Note- Clock/DLL Considerations in 72Mb QUAD,QUADP,DDR-II,DDR-IIP SRAM

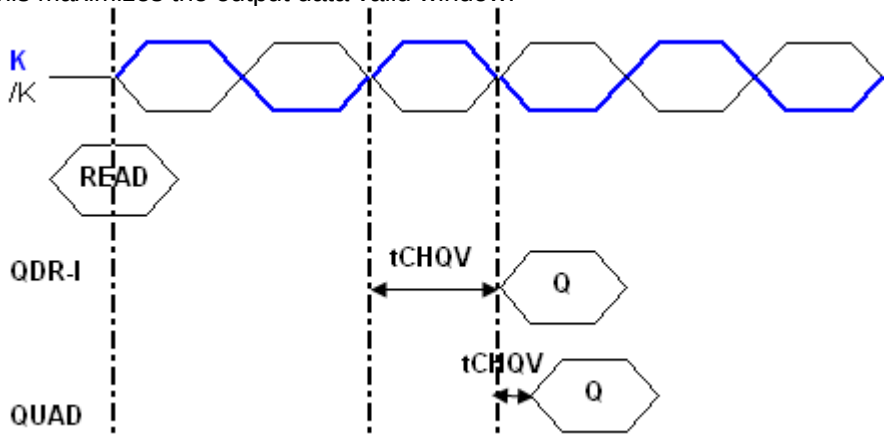
Abstract

This document summarizes the Clock Considerations for the 72Mb QUAD,QUADP,DDR-II,DDR-IIP Sync SRAMs.

Contents

1. DLL(Delay Locked Loop)

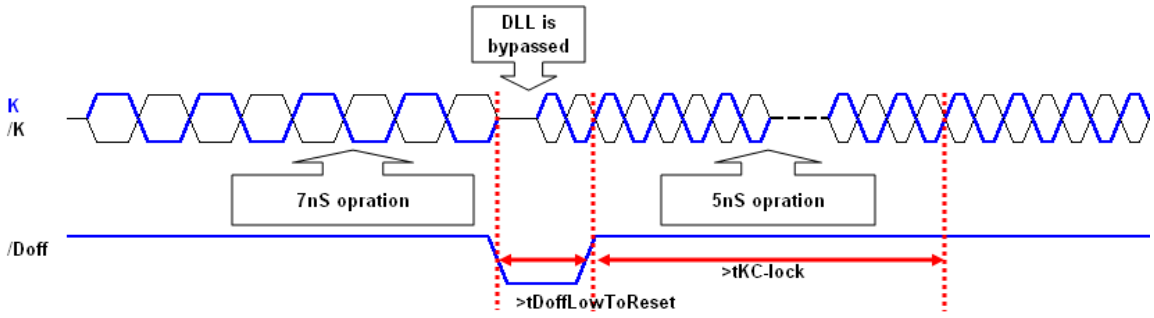
A DLL is a new feature that was added to the QUAD,QUADP,DDR-II,DDR-IIP SRAM product families. The DLL aligns the output data coincident with the rising edge of C and /C clock. In single clock mode, they will be synchronized with K and /K. The following picture shows the difference between QDR-I and QUAD. QUAD has a half cycle more latency but a faster output time than QDR-I. This maximizes the output data valid window.



The DLL locks to the input clocks. It requires a stable C,/C or K,/K input for a minimum tKC-lock(=1024 cycle) period. When it is locked, the input clocks must have a low phase jitter, which is specified at tKC-VAR in the datasheet. If the input clocks have jitter of more than tKC-VAR, the DLL must execute the DLL reset procedure.

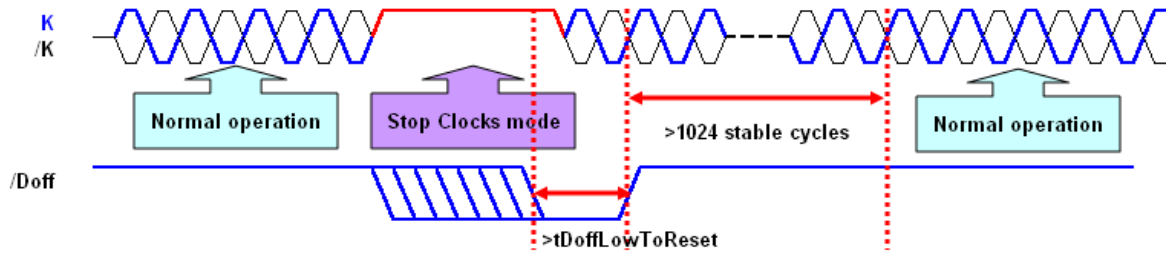
2. DLL reset

DLL reset allows the ability to lock to a new target clock frequency. When /Doff pin is at a logical Low for more than tDoffLowToReset, the device will clear the old lock value. The DLL is bypassed when /Doff is Low. When /Doff pin goes to a logical High again, the DLL will turn on again. After a period of tKC-lock, the DLL will lock to the new value.



3. Stopped-clocks mode

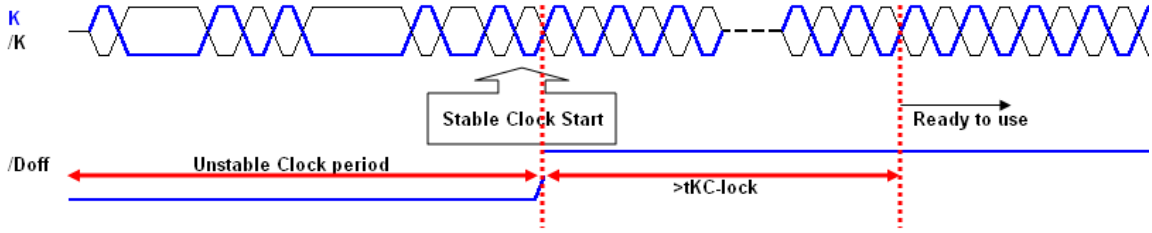
Stopped-clocks mode can be used to minimize power consumption. During the stopped-clocks or No-clocks modes, the input clock pins must be at VIH or VIL levels in order to save power. This stopped clock mode also requires the DLL reset procedure to be executed when it resumes normal mode.



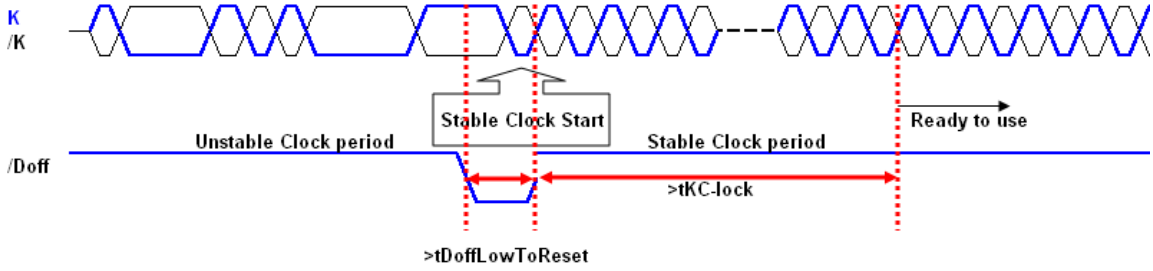
Note) K and /K can be either VIH or VIL during the Stop clocks mode.

4. Power up sequence

During power up, the input clock from the SRAM controller may be unstable. In order to lock the DLL to the correct value, it is best to bypass the input clocks during power up by setting /Doff low. Please refer to the product datasheet for the recommended power up sequence.



If /Doff needs to be high during power up, then /Doff must be low for a period of at least tDoffLowToReset period and then return to a high level for the DLL to reset to the stable clock.



Summary

This application note covers how the DLL locks to the right frequency and how to reset it. This document also describes how to resolve issues related to abrupt changes in clock frequency. For any questions, please email to jhkim@issi.com or jiff_lee@issi.com