

ACCOMPLISHMENT OF CIRCUIT PARTITIONING USING VHDL AND CLUSTERING PERTAINING TO VLSI DESIGN

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Abstract— The relevance of VLSI in performance computing, telecommunications, and consumer electronics has been expanding progressively, and at a very hasty pace. In order to build complex digital logic circuits it is often essential to sub-divide multi – million transistors design into manageable pieces. Circuit partitioning is a general approach used to solve problems that are too large and complex to be handled at once. In partitioning, the problem is divided into small and manageable parts recursively, until the required complexity level is reached. In the area of VLSI, circuit complexity is rapidly multiplying, together with the reducing chip sizes; the integrated chips being produced today are highly sophisticated. There are many diverse problems that occur during the development phase of an IC that can be solved by using circuit partitioning which aims at obtaining the sub circuits with minimum interconnections between them. This paper aims at circuit partitioning using clustering technique by applying two clustering algorithms NNA(Nearest Neighbour) and PAM(Partitioning around medoids). These two algorithms were tested on a BCD to Seven Segment Code Converter circuit consisting of eight nodes and were implemented on VHDL. The tested results show that PAM yield better subcircuits than NNA.

Keywords: *Circuit Partitioning, VLSI, NNA, PAM*

I. INTRODUCTION

Advances in semiconductor technology and in the integration level of integrated circuits have enhanced many features, increased the performance; improved reliability of electronic equipment, and at the same time reduced the cost, power consumption and system size. As size and complexity of digital system has increased, more computer aided design tools are introduced into hardware design processes. VLSI

design automation has attracted a great deal of interest. A recent survey [1] lists almost 200 papers on the subject. Circuit partitioning in VLSI design is key role in physical design. The objective of circuit partitioning is to divide the circuit into number of subcircuits with minimum interconnections between them.

In past two decade, partitioning problems has been studied by researchers and various heuristic algorithms have been developed [2]-[4]. The circuit partitioning is also achieved by using some of the clustering algorithm [6]. In this paper to achieve circuit partitioning, with minimum interconnections is obtained by applications of two clustering algorithms PAM and NNA. These two clustering algorithms are applied to BCD to Seven segment circuit consisting of eight nodes. Results show that PAM gives better clusters with minimum interconnections. Both the clustering algorithms are run on VHDL code and is tested.

II. IMPLEMENTATION

The implementation consists of three stages consisting of data extraction, partitioning and result. In data extraction, a VLSI circuit of BCD to 8 segment converter is considered. The circuit considered is shown below

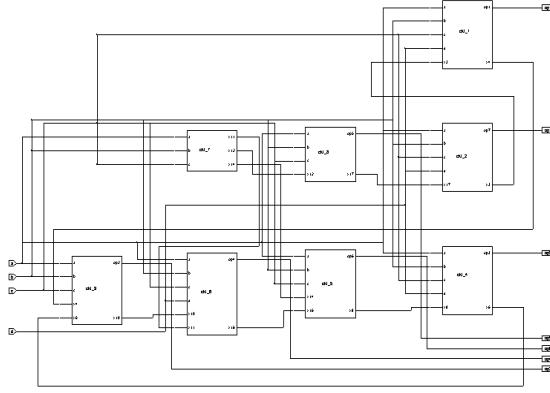


Fig. 1

In the above circuit each rectangular box is considered as a node. The circuit consists of 8 nodes with interconnection between them. The sub circuits within one the node is shown in fig 2. The input to this circuit is a BCD(Binary coded Decimal) code and output is seven segment code.

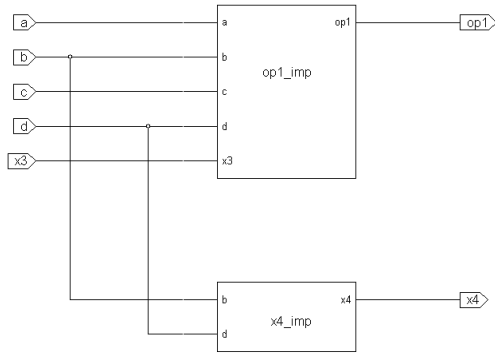


Fig 2

Figure 3 shows the internal view of op1_mp which consists some of the basic gates like AND OR and inverter gates. Similarly each node consists of all the basic gates

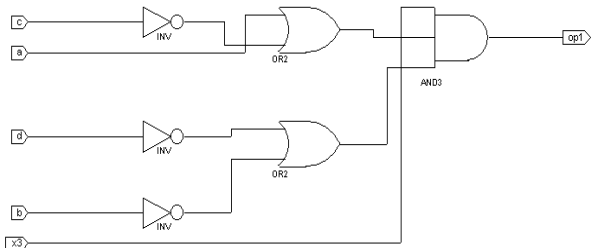


Fig. 3

The out put is the seven segment display which is depicted in fig 4. The input to the circuit and the corresponding output obtained is shown in table 1.

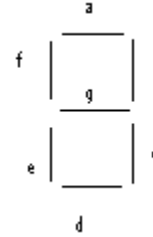


Fig. 4

From the table 1 it is clear that whenever the input of '0', in the seven segment display except 'g' all other values are '1'. Since the input is BCD the input values are taken from '0' to '9' only.

Table 1: Input and Output for the BCD to Seven segment Circuit

Input 1	Input 2	Input 3	Input 4	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	0	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	0	1	1

III. SUMMARY OF CLUSTERING ALGORITHM

Clustering is referred as unsupervised learning segmentation. The clusters are formed by finding the similarities between data according to characteristics found in the data. It can be thought of as partitioning or segmenting the data into groups that might or might not be disjointed. In this paper we are using Nearest Neighbor Algorithm and PAM (Partitioning around mediods).

A. Nearest Neighbor Algorithm

This is serial algorithm in which the items are iteratively merged into the existing clusters that are closest. In this algorithm a threshold, t is used to determine if items will be added to existing clusters or if a new cluster is created. The complexity of the algorithm depends on the number of items. For each loop each item must be compared to each item already in a cluster. The time complexity is $O(n^2)$.

B. PAM Algorithm

This algorithm [9] represents a cluster by a medoid. Using this algorithm handles outliers well. Quality of clusters is measured by the sum of all distances from a non-medoid object to the medoid for the cluster it is in. We use C_{jih} to be the cost change for an item t_j associated with swapping medoid t_i with non-medoid t_h . The total complexity per iteration is $n(n-k)^2$. The cost is the change to the sum of all distances from items to their cluster medoids. The total impact to quality by a medoid change TC_{ih} is given by

$$TC_{ih} = \sum_{j=1}^n C_{jih}$$

IV. RESULTS AND CONCLUSION

In data extraction, the circuit which is a BCD to seven segment code converter consisting of 8 nodes is considered. The circuit is represented by an adjacency matrix where the values represent the distances between the nodes. The adjacency matrix is fed into an algorithm which gives the sub-circuits with the lowest amount of interconnections between them. The partition is tested on the circuit. The table below gives the performance of PAM and Nearest Neighbour algorithm. The algorithm is implemented on Xilinx 6.1 using Project Navigator using VHDL.

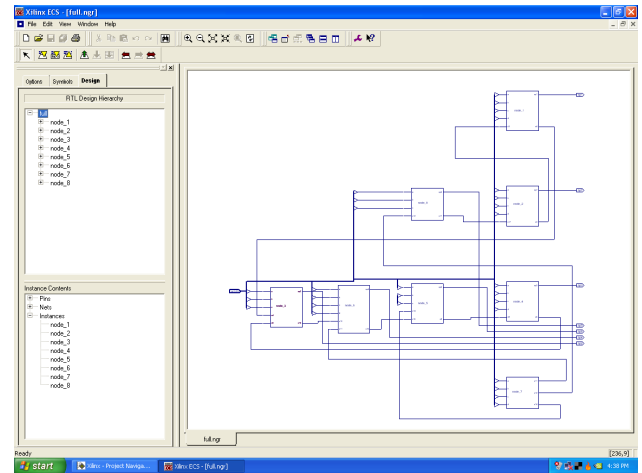
V. CONCLUSION

In this paper the Circuit Partitioning which plays a critical role in physical design of an integrated circuit with minimum interconnections is

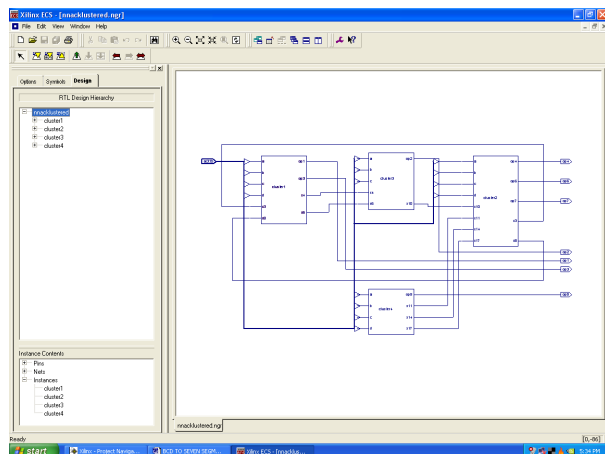
obtained by implemented using two clustering algorithms PAM and NNA. Experimental results show that NNA gives four clusters where PAM gives two clusters for the same input. The circuit also shows the minimum interconnections between them.

Table 2: Performance of PAM and NNA

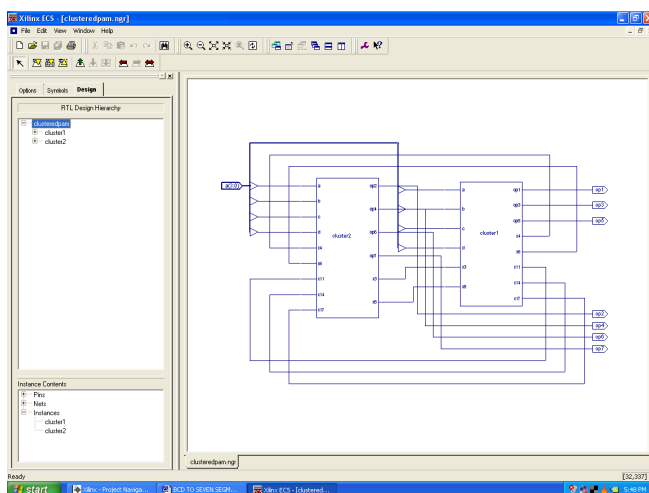
Input	No. of Clusters	
	PAM	Nearest Neighbour
BCD to seven segment	2	4



Screen shot showing the BCD to Seven segment Display



Screen shot depicting the circuit after application of NNA Algorithm consisting of 4 clusters



Screen shot depicting the circuit after application of PAM Algorithm consisting of 2 clusters

VI. REFERENCES

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