HU

Dept of Electrical and Computer Engineering

420 Intro to VLSI Design

Lecture 0: Course Introduction and Overview

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Spring 2005

Getting Started

- Syllabus
  - About the Instructor
  - Labs, Problem Sets, and Project
  - Grading
  - Collaboration
- Textbook
- Student Expectations
- CAD Tools and Projects

Today's Topics

- Course Objectives
- The Billion $ Industry
- What is an integrated circuit?
- What is CMOS, VLSI, ASIC?
- Review of the Fundamentals
  - How are CMOS transistors built?
  - Building logic gates from transistors
  - Transistor layout and fabrication

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Course Objectives (I)

- By the end of the semester, you will be able to……
  - VLSI Circuit Analysis:
    - Understand MOS transistor operation, design eqns.
    - Understand parasitics & perform simple calculations
    - Understand static & dynamic CMOS logic
    - Estimate delay of CMOS gates, networks, & long wires
    - Estimate power consumption
    - Understand design and operation of latches & flip/flops

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Course Objectives (II)

- CMOS Processing and Layout
  - Understand the VLSI manufacturing process.
  - Have an appreciation of current trends in VLSI manufacturing.
  - Understand layout design rules.
  - Design and analyze layouts for simple digital CMOS circuits
  - Design and analyze hierarchical circuit layouts.
  - Understand ASIC Layout styles.

Course Objectives (III)

- VLSI System Design
  - Understand the design flows used in industrial IC design.
  - Design simple combinational and sequential logic circuits using using a Hardware Description Language (HDL).
  - Design a small standard-cell chip in its entirety using a variety of CAD tools and check it for correct operation.

Course Objectives (IV)

- Special Topics
  - Understand issues related to the integration of analog and digital circuits on a single chip
  - Understand the adverse affects of space/nuclear radiation on ICs

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The Billion $ Industry

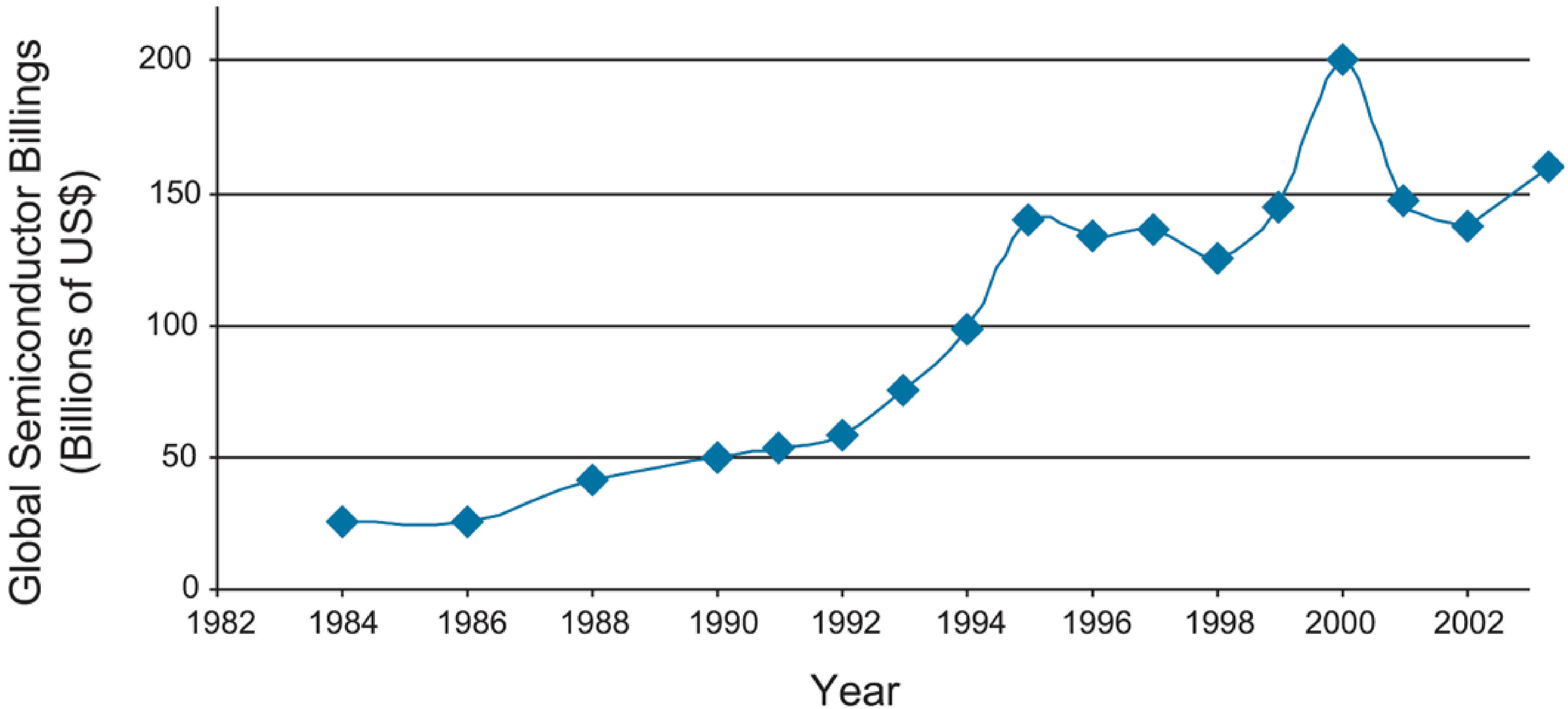
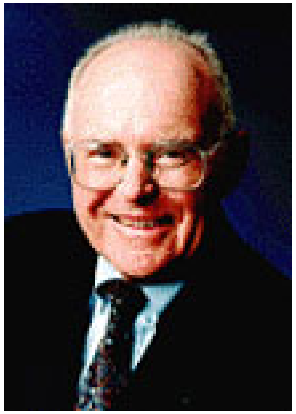


FIG 1.1 Size of worldwide semiconductor market

Source: Semiconductor Industry Association.

VLSI Trends: Moore's Law

- In 1965, Gordon Moore predicted that transistors would continue to shrink, allowing:
  - Doubled transistor density every 18-24 months
  - Doubled performance every 18-24 months
- History has proven Moore right
- But, is the end is in sight?
  - Physical limitations
  - Economic limitations



Gordon Moore
Intel Co-Founder and Chairmain Emeritus
Image source: Intel Corporation www.intel.com

IC Evolution (I)

- SSI – Small Scale Integration (1965)
  - contained 1 – 10 logic gates
- MSI – Medium Scale Integration (1970)
  - logic functions, counters ($30\text{-}10^3$)
- LSI – Large Scale Integration (1980)
  - first microprocessors on the chip (10^3- 10^5)
- VLSI – Very Large Scale Integration (1985)
  - now offers 64-bit microprocessors, complete with cache memory (L1 and often L2), floating-point arithmetic unit(s), etc.
  - (10^5-10^7)

IC Evolution (II)

- ULSI – Ultra Large Scale Integration (1990)
  - $10^7 – 10^9$
- Giga-Scale Integration (2005)
  - $10^9 – 10^{11}$
- Tera-Scale Integration (2020)
  - $10^{11} - 10^{13}$

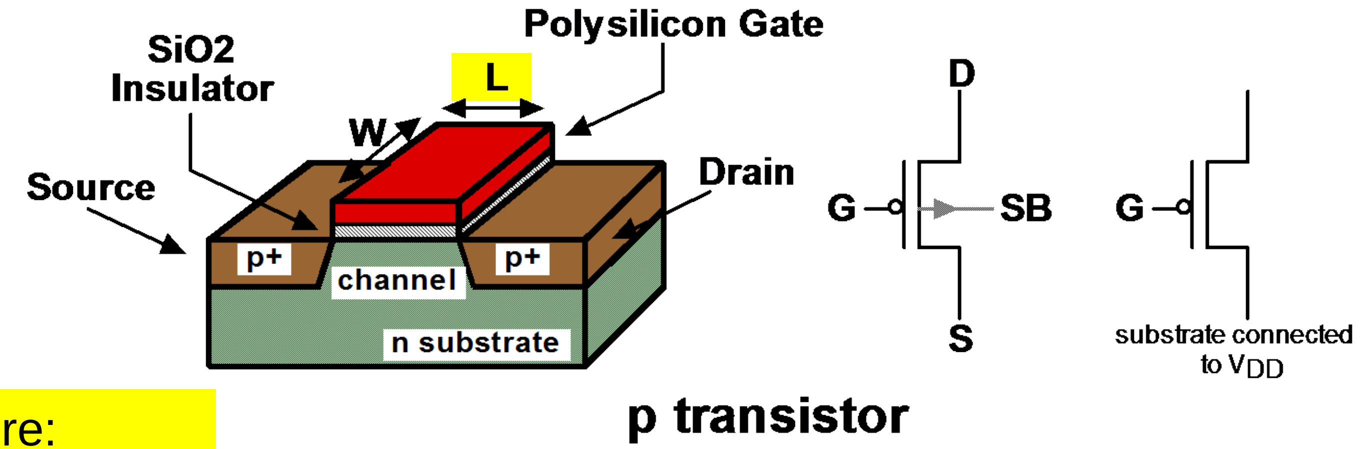
IC Evolution (III)

- Bipolar technology
  - TTL (transistor-transistor logic)
  - ECL (emitter-coupled logic)
- MOS (Metal-oxide-silicon)
  - although invented before bipolar transistor, was initially difficult to manufacture
  - nMOS (n-channel MOS) technology developed in 1970s
    required fewer masking steps, was denser, and consumed less power than equivalent bipolar ICs => an MOS IC was cheaper than a bipolar IC and led to investment and growth of the MOS IC market.

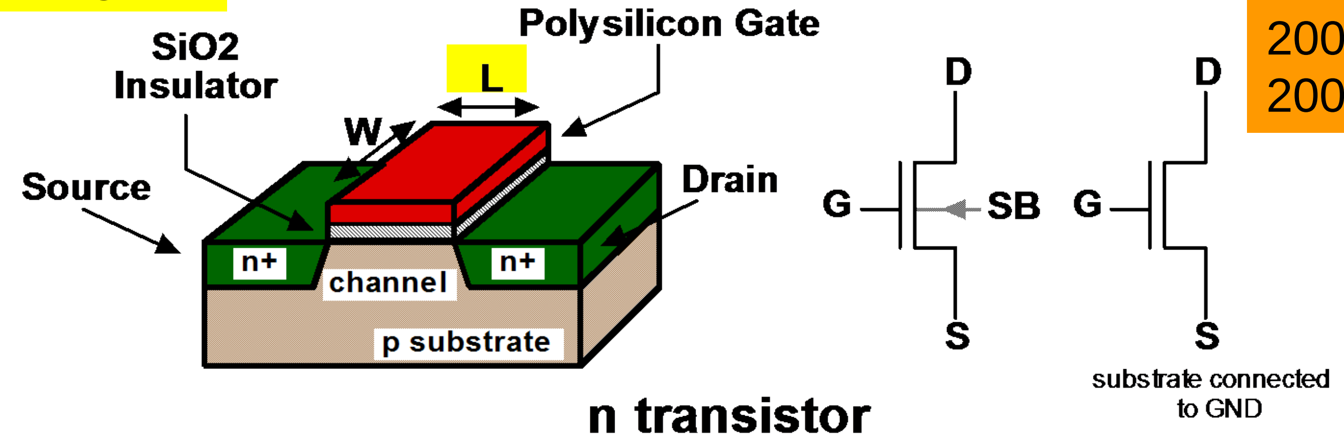
IC Evolution (IV)

  - aluminum gates for replaced by polysilicon by early 1980
  - CMOS (Complementary MOS): n-channel and p-channel MOS transistors =>
    lower power consumption, simplified fabrication process
- Bi-CMOS - hybrid Bipolar, CMOS (for high speed)
- GaAs - Gallium Arsenide (for high speed)
- Si-Ge - Silicon Germanium (for RF)

VLSI Tech: CMOS



Key feature:
transistor **length L**



2002: L=130nm
2003: L=90nm
2005: L=65nm?

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CMOS Devices

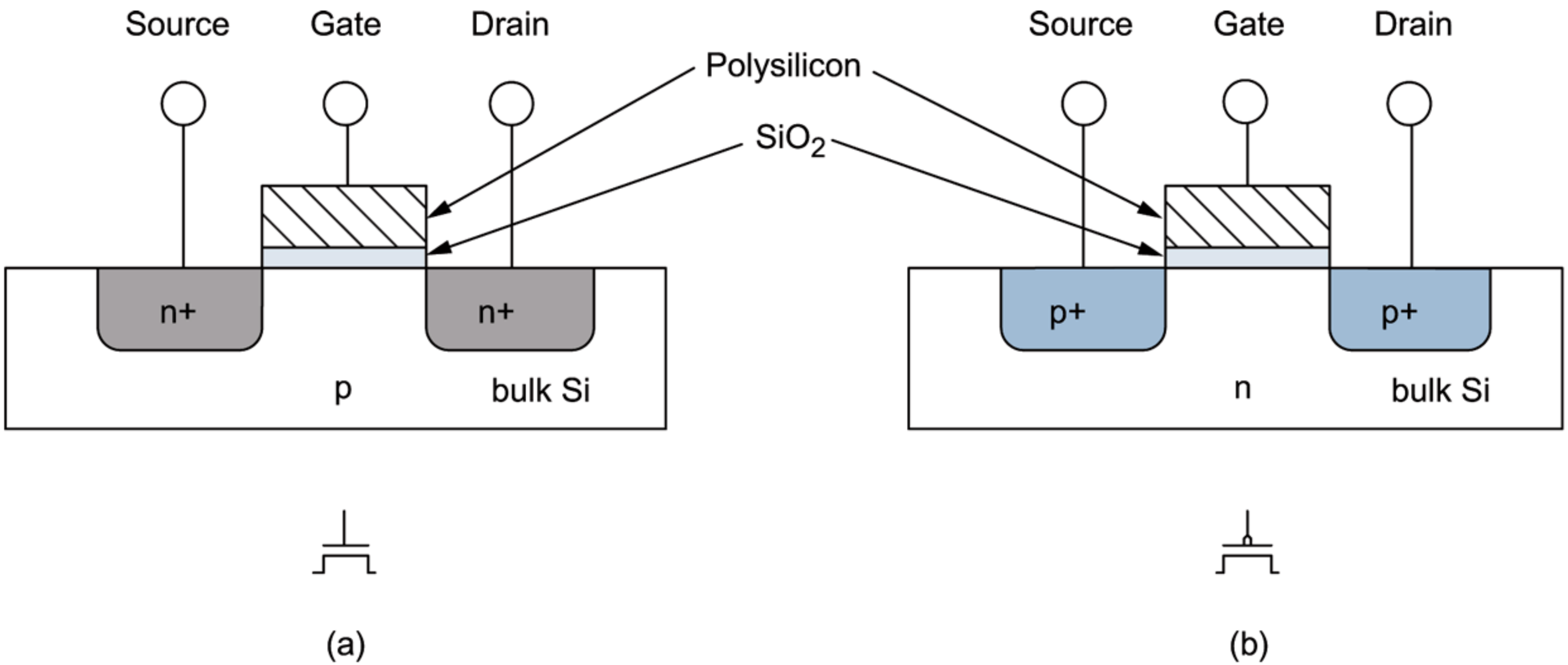
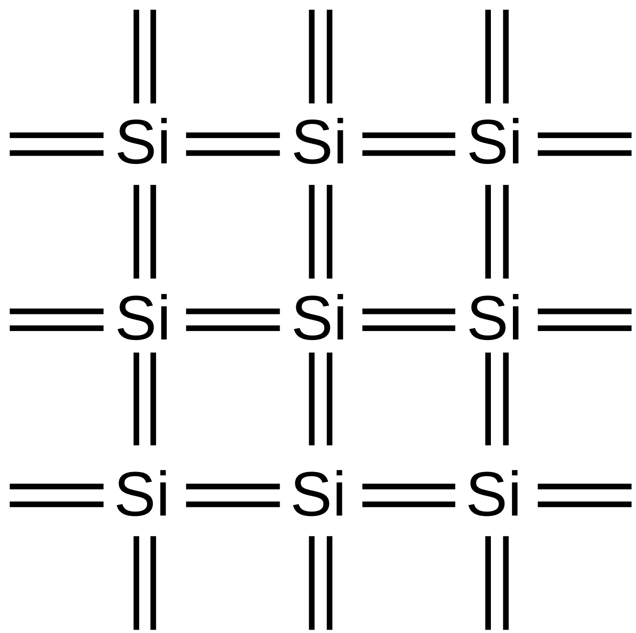


FIG 1.8 nMOS transistor (a) and pMOS transistor (b)

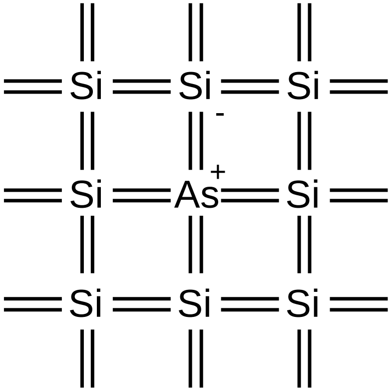
Silicon Lattice

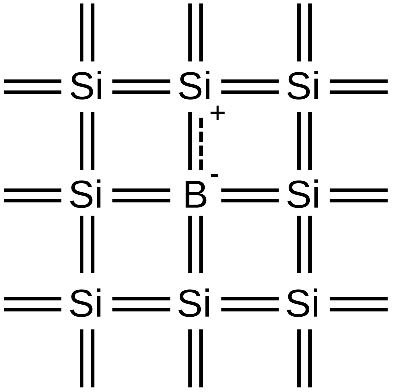
- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors



Dopants

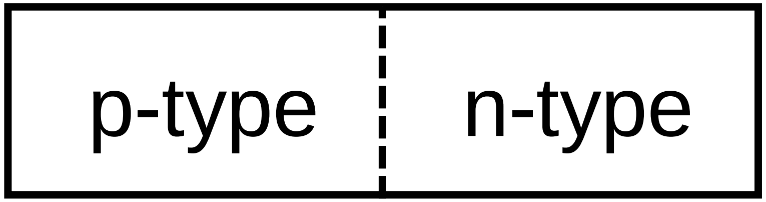
- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)

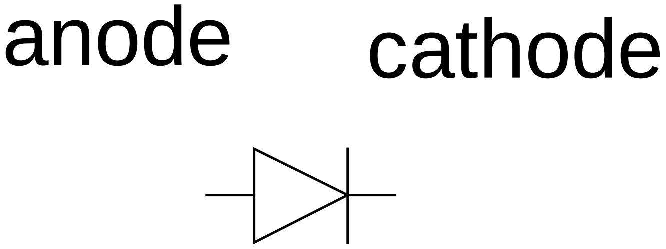




p-n Junctions

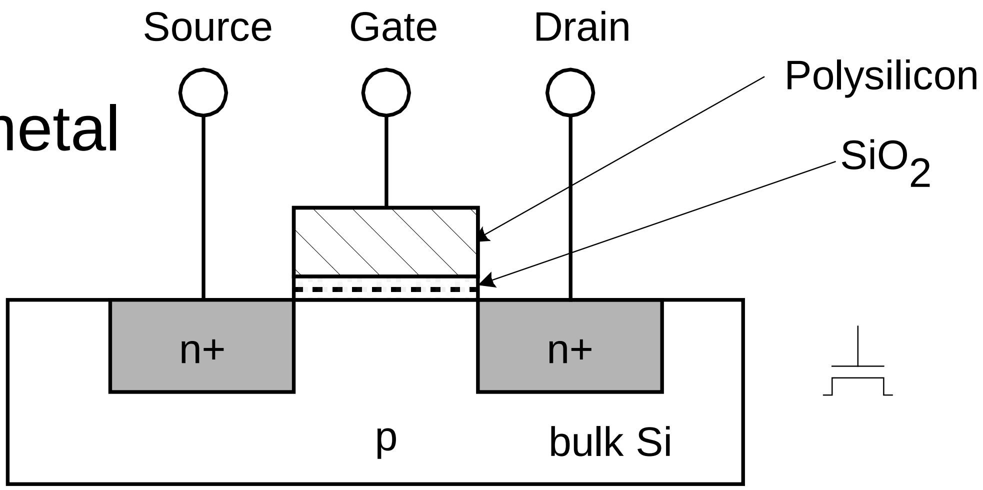
- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction





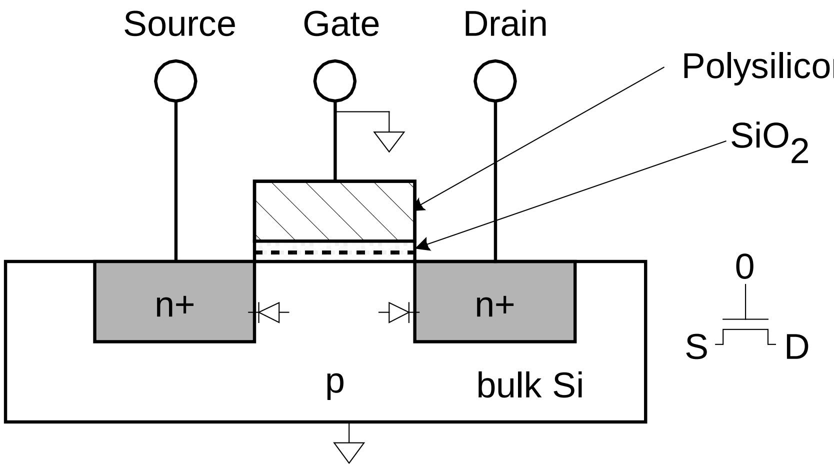
nMOS Transistor

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal



nMOS Operation

- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



nMOS Operation Cont.

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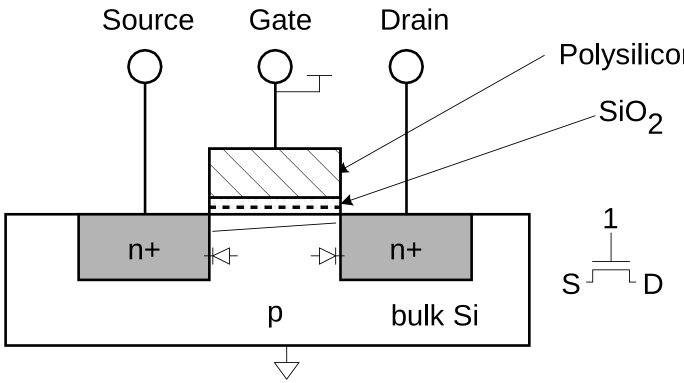
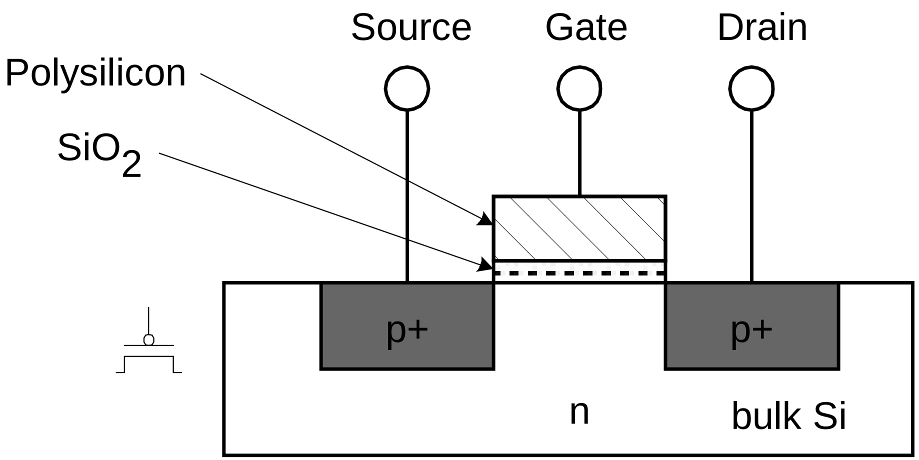
- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior

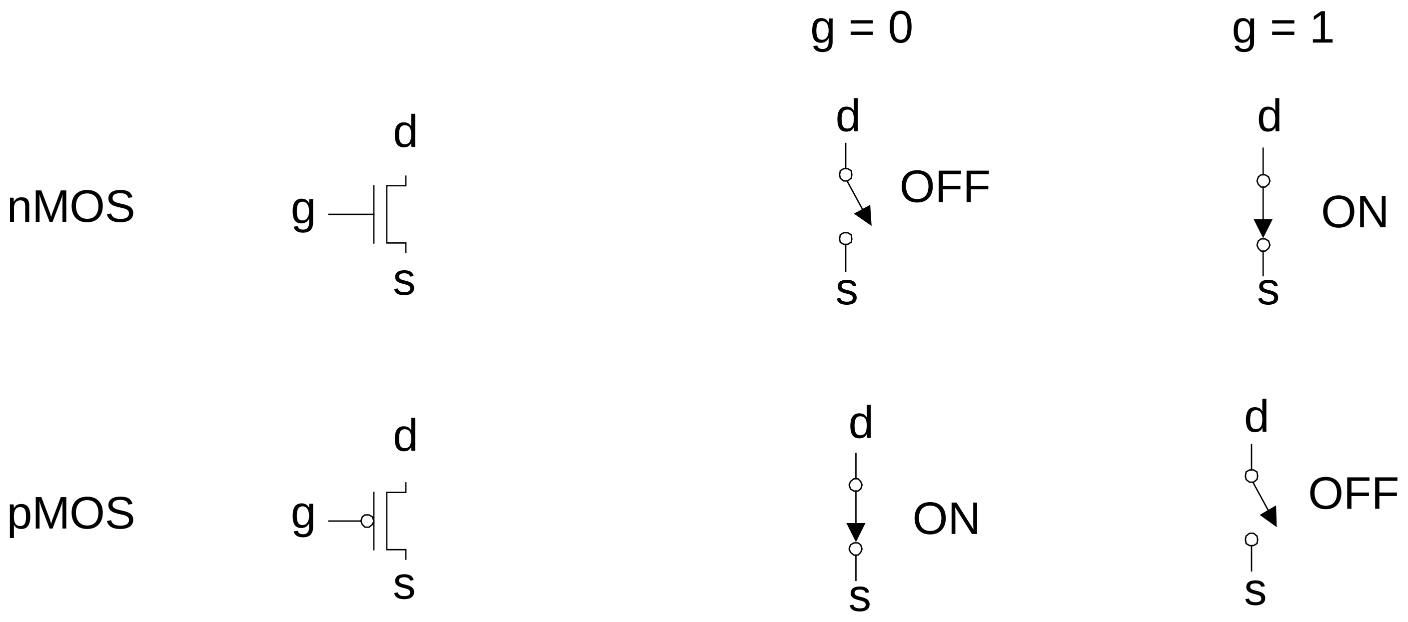


Power Supply Voltage

- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

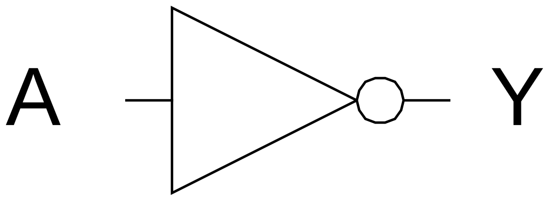
HU Transistors as Switches

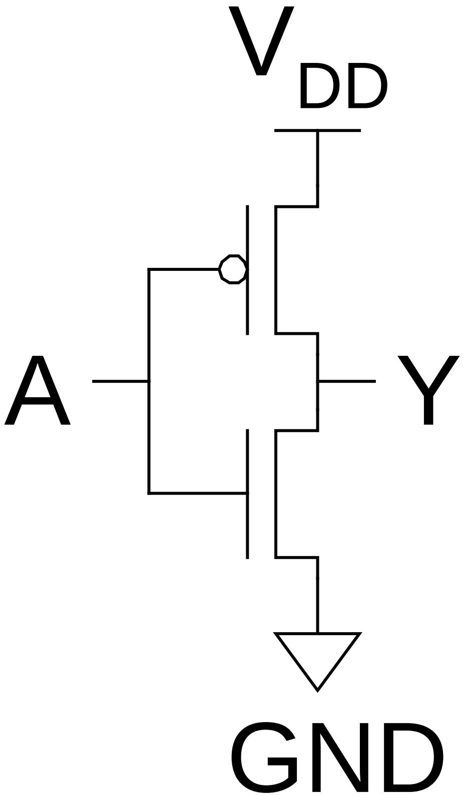
- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS Inverter

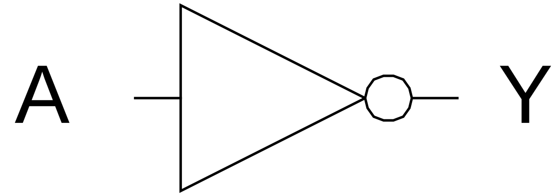
A	Y
0	
1	

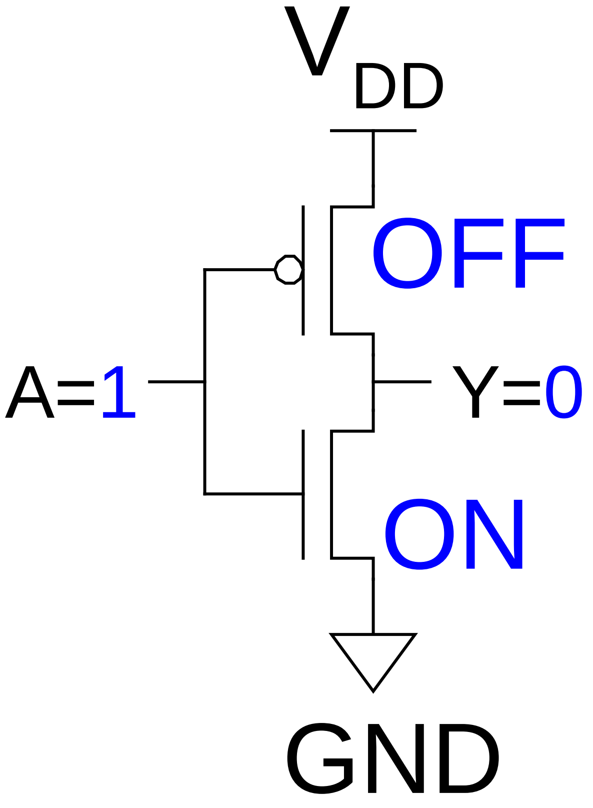




CMOS Inverter

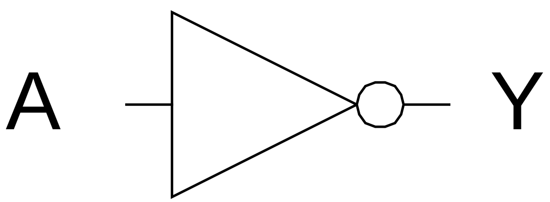
A	Y
0	
1	**0**

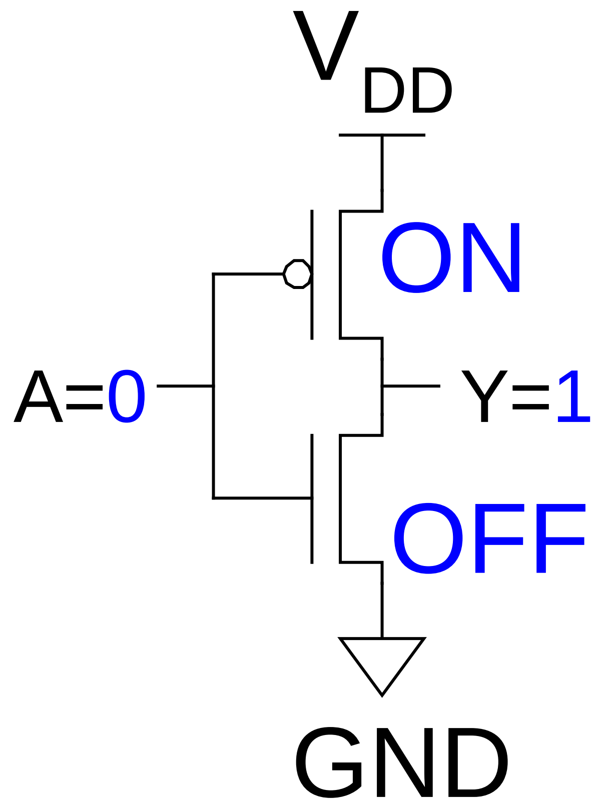




CMOS Inverter

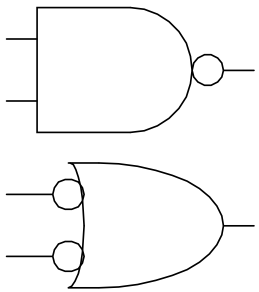
A	Y
0	**1**
1	0

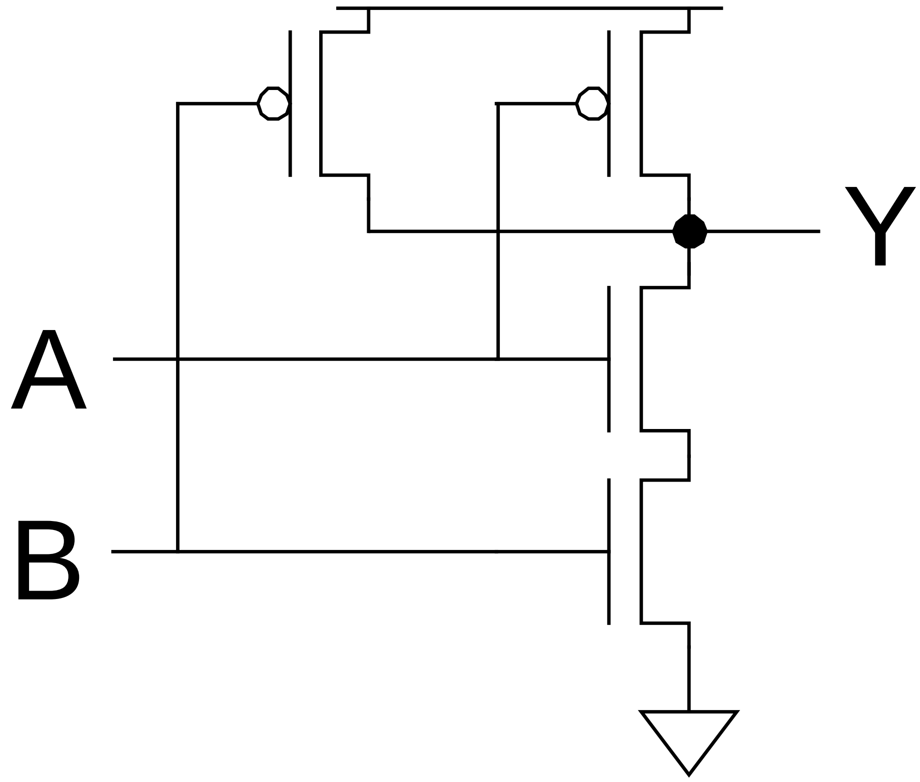




CMOS NAND Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	





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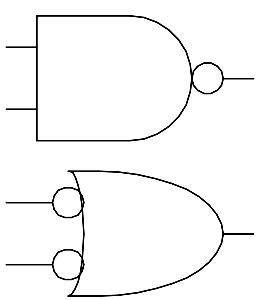
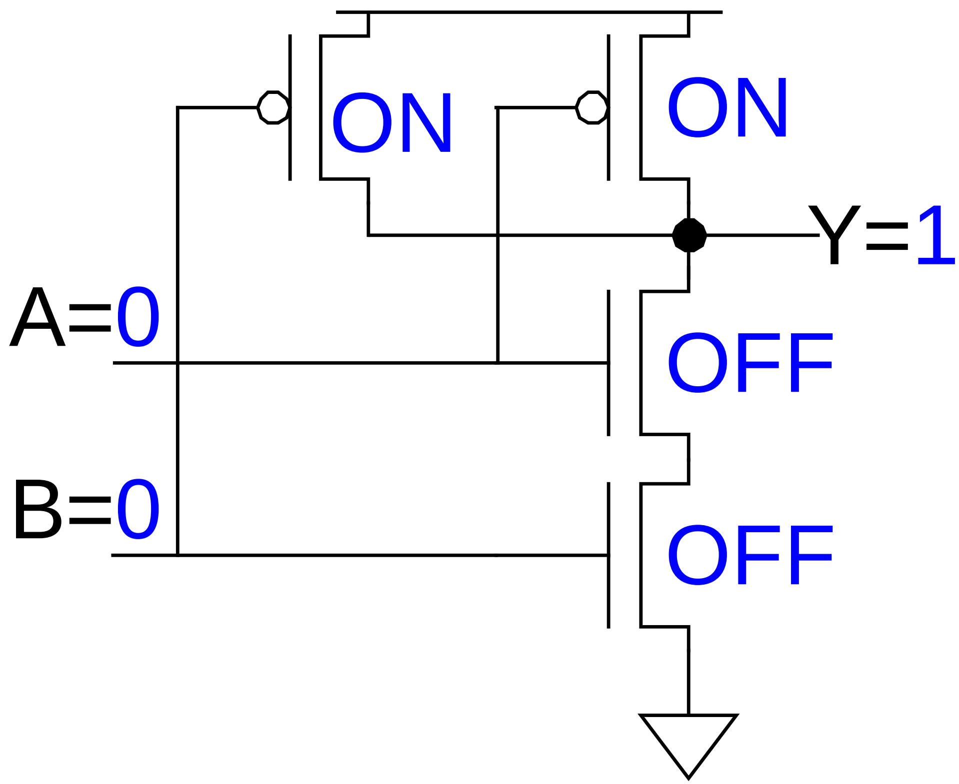
CMOS NAND Gate

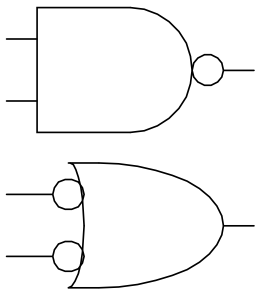
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

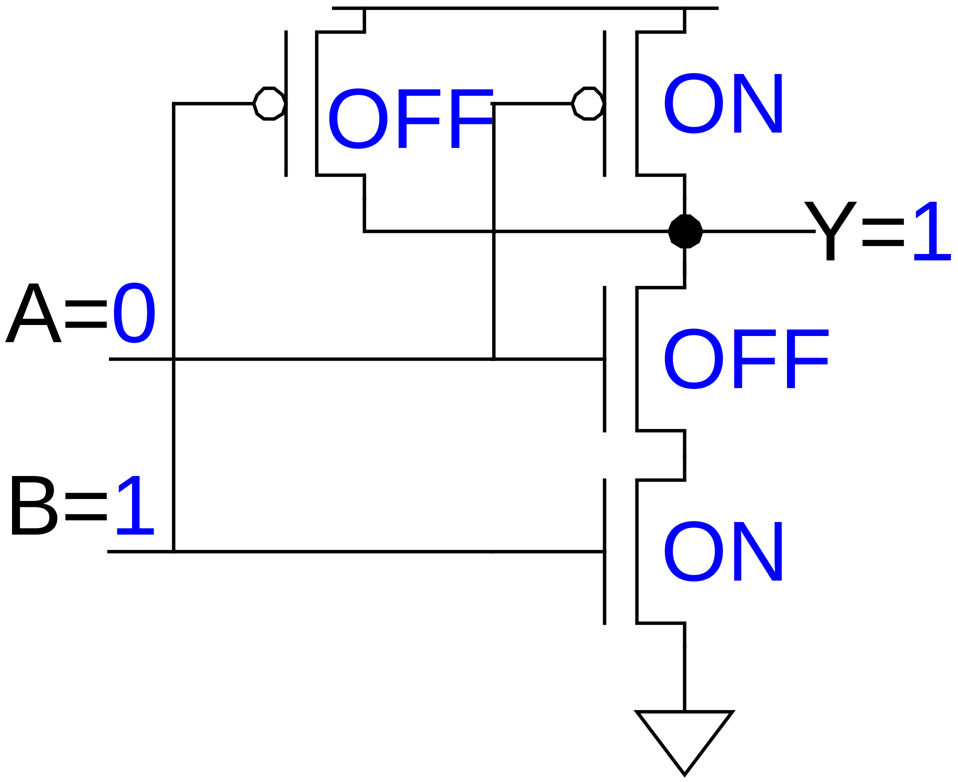




CMOS NAND Gate

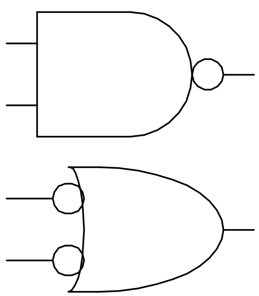
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

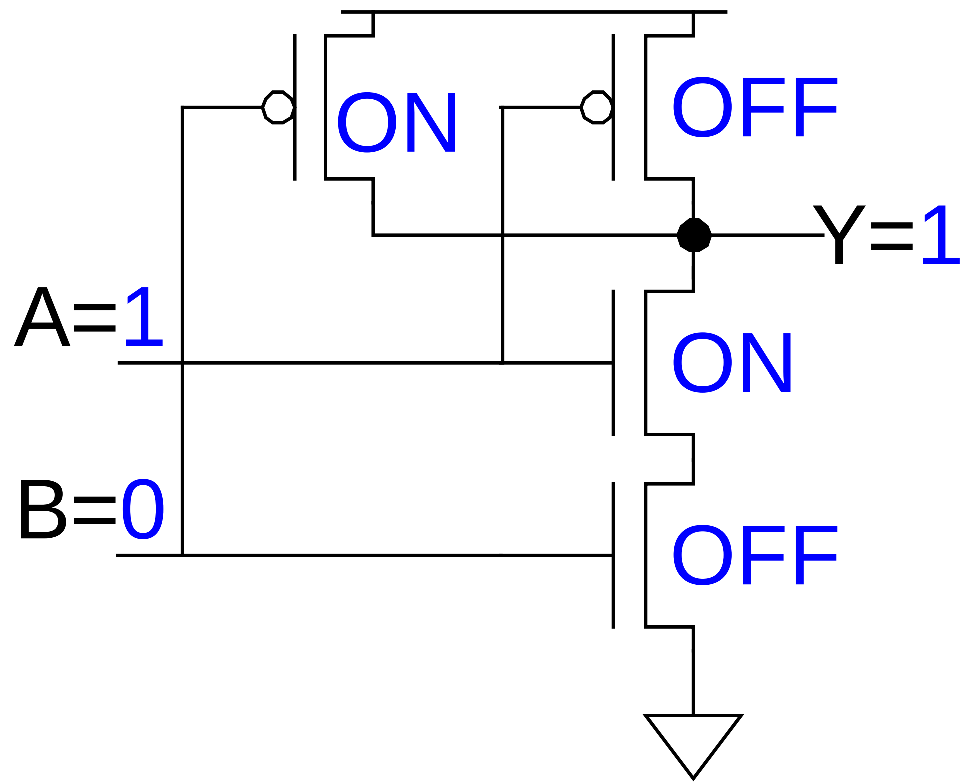




CMOS NAND Gate

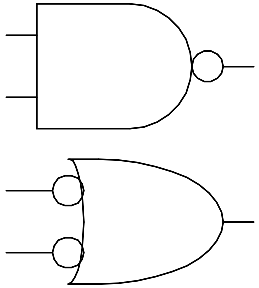
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

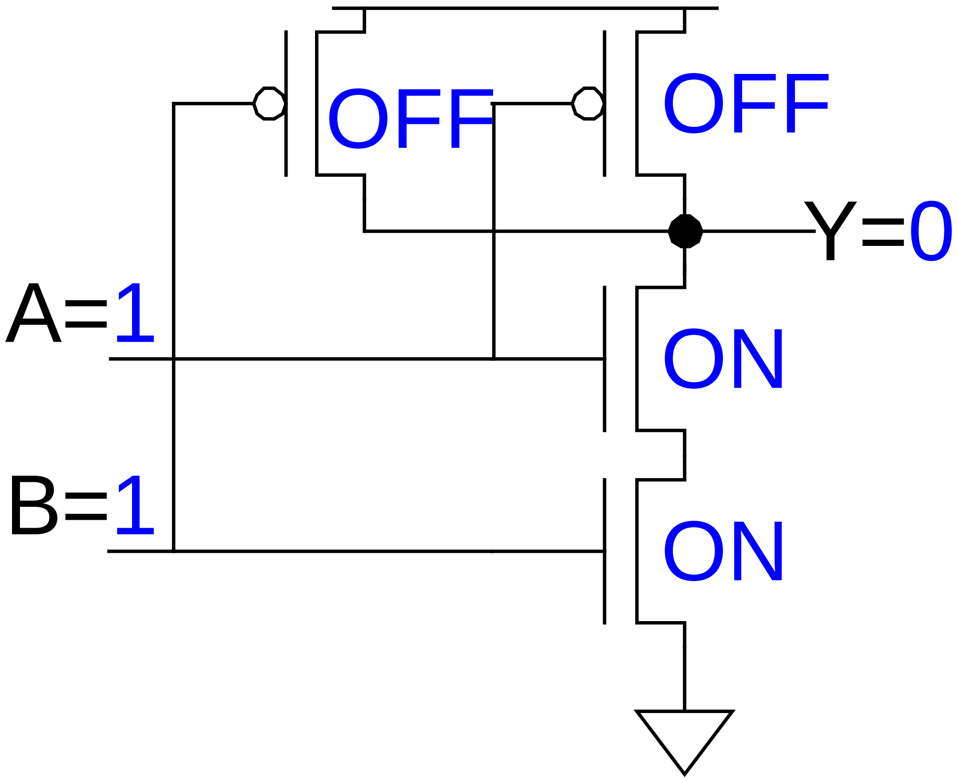




CMOS NAND Gate

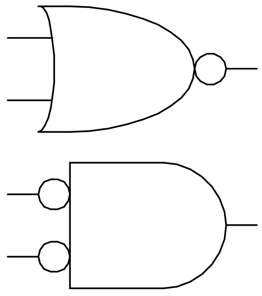
A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

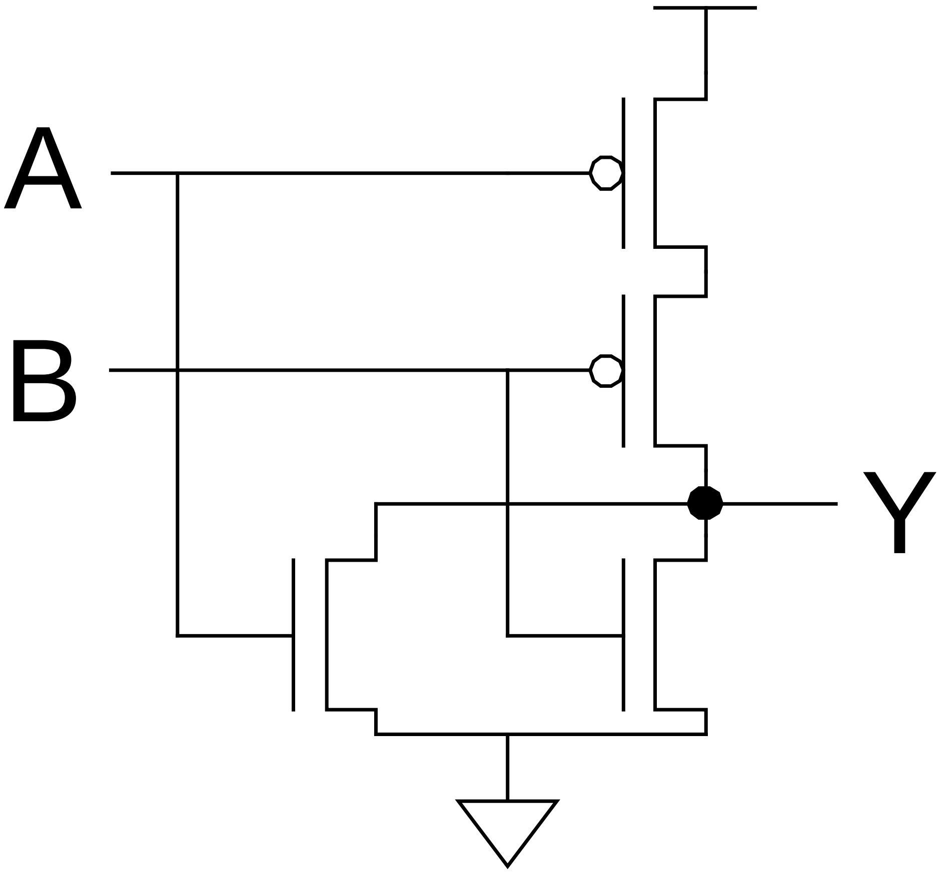




CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0





3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

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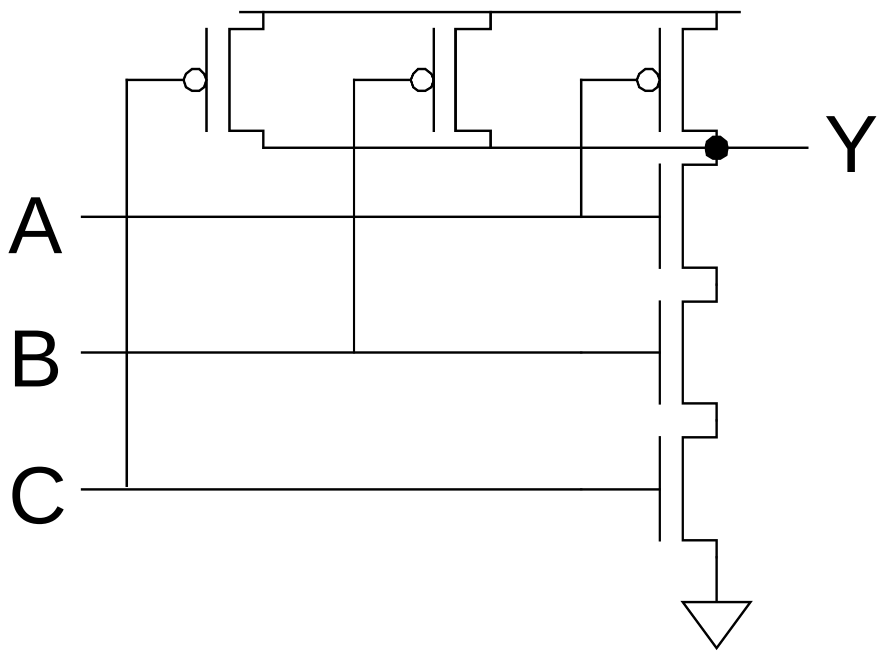
3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

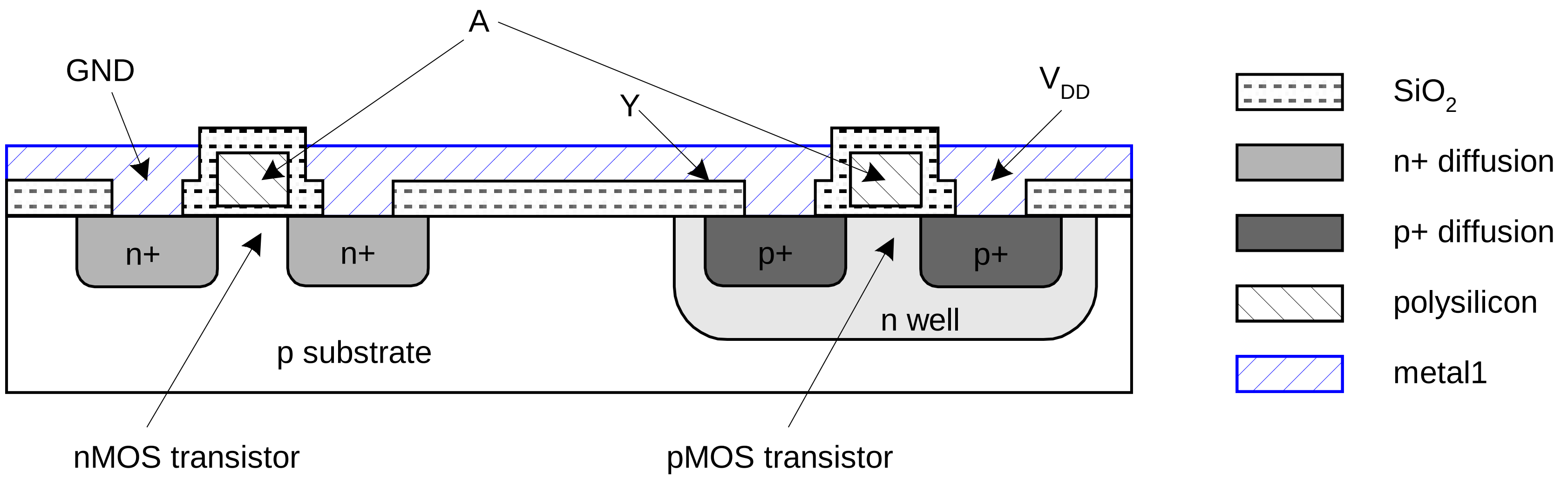


CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

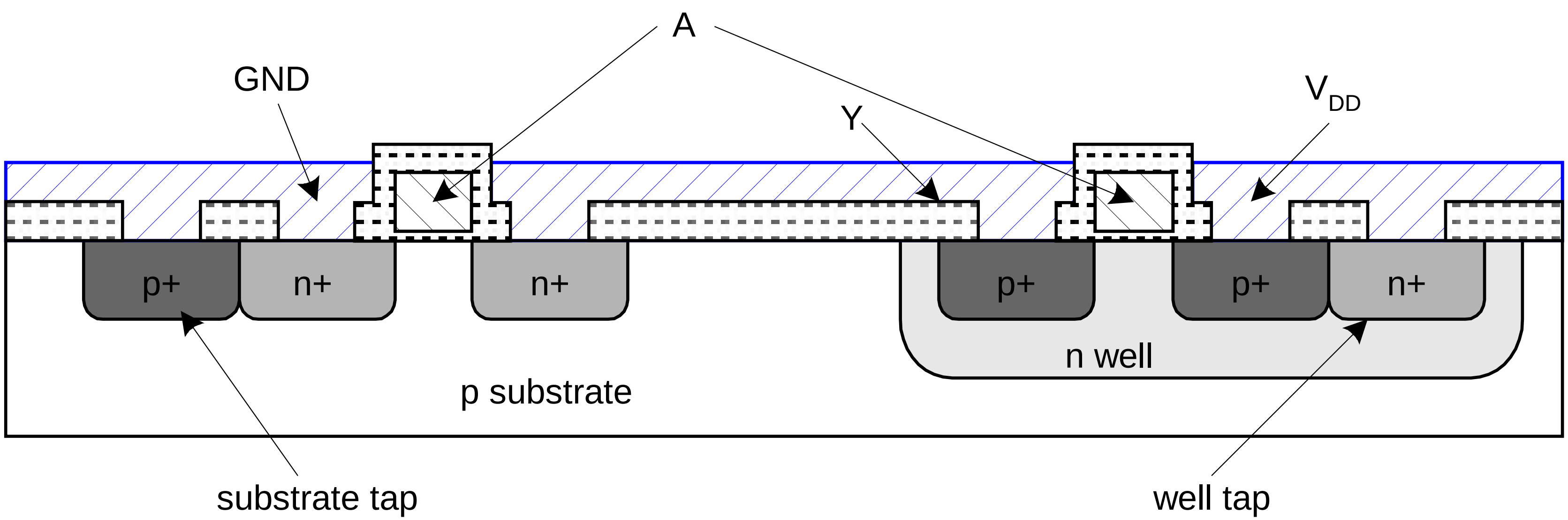
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



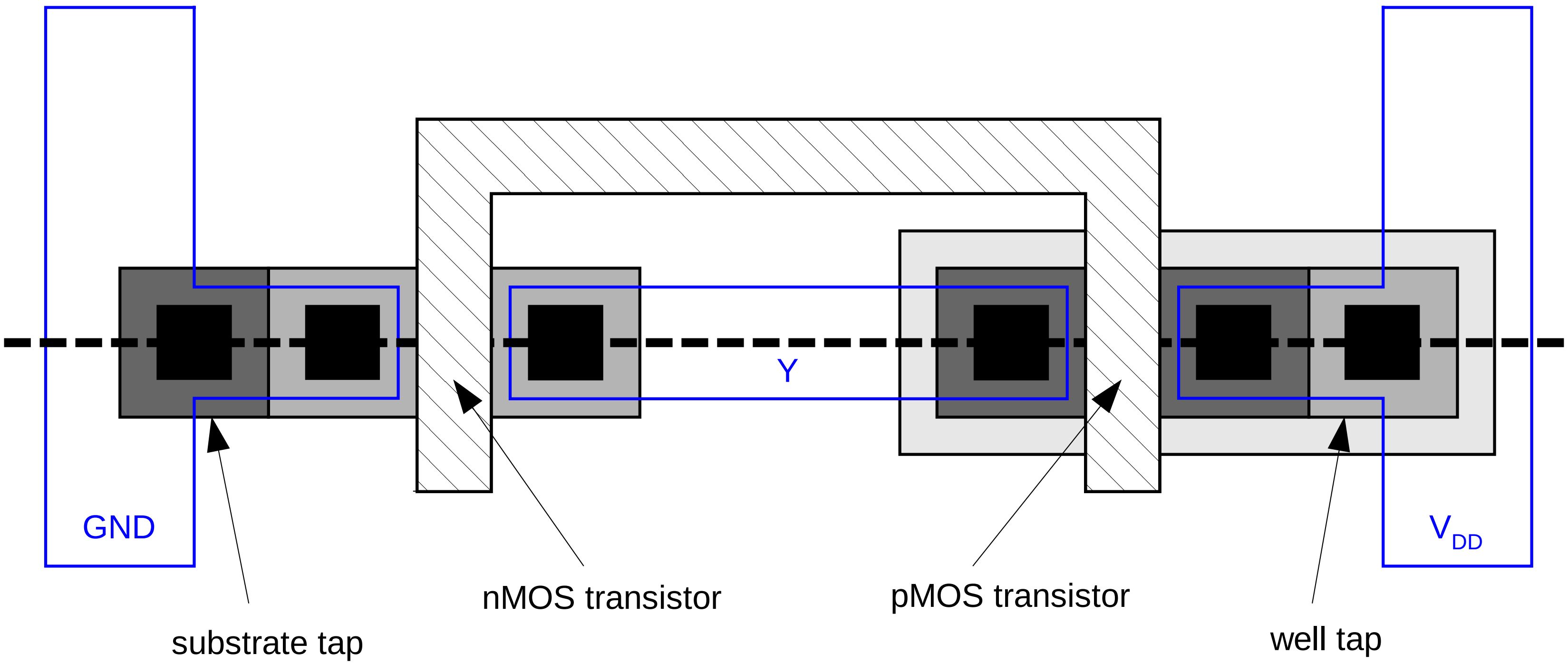
HU Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



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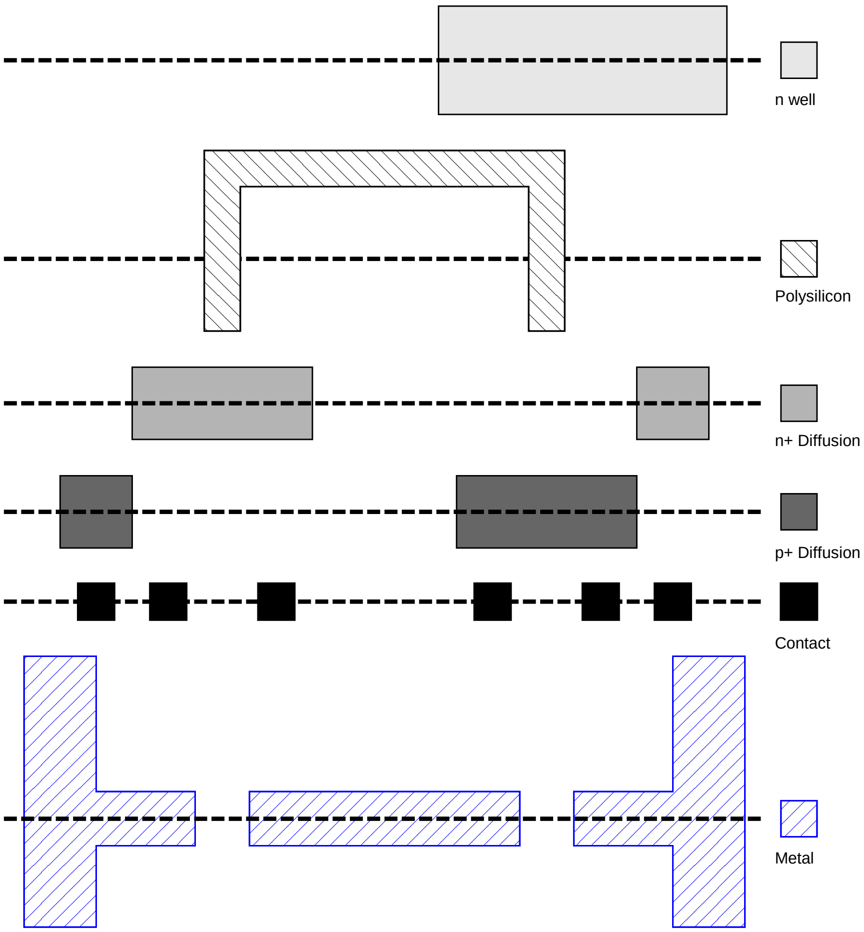
Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



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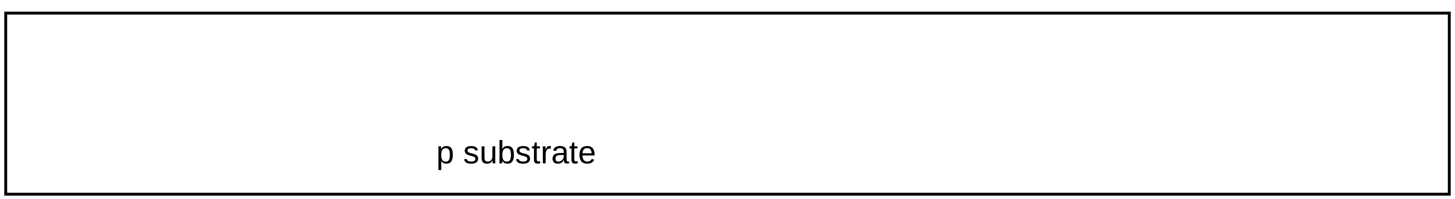
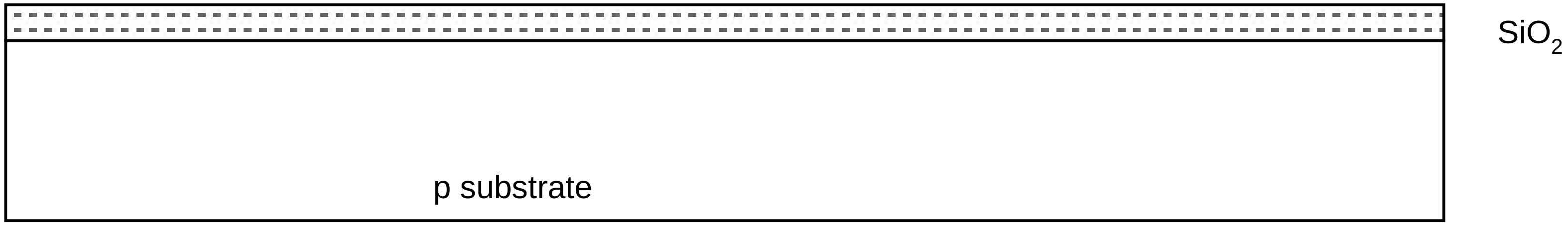
Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2



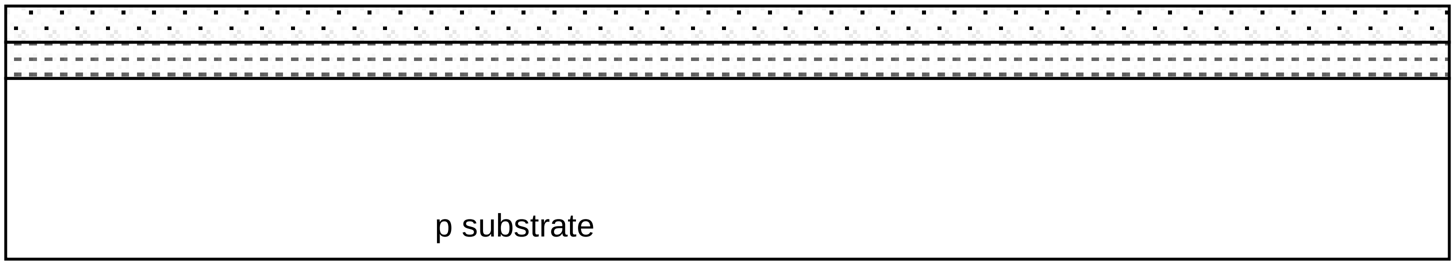
Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace



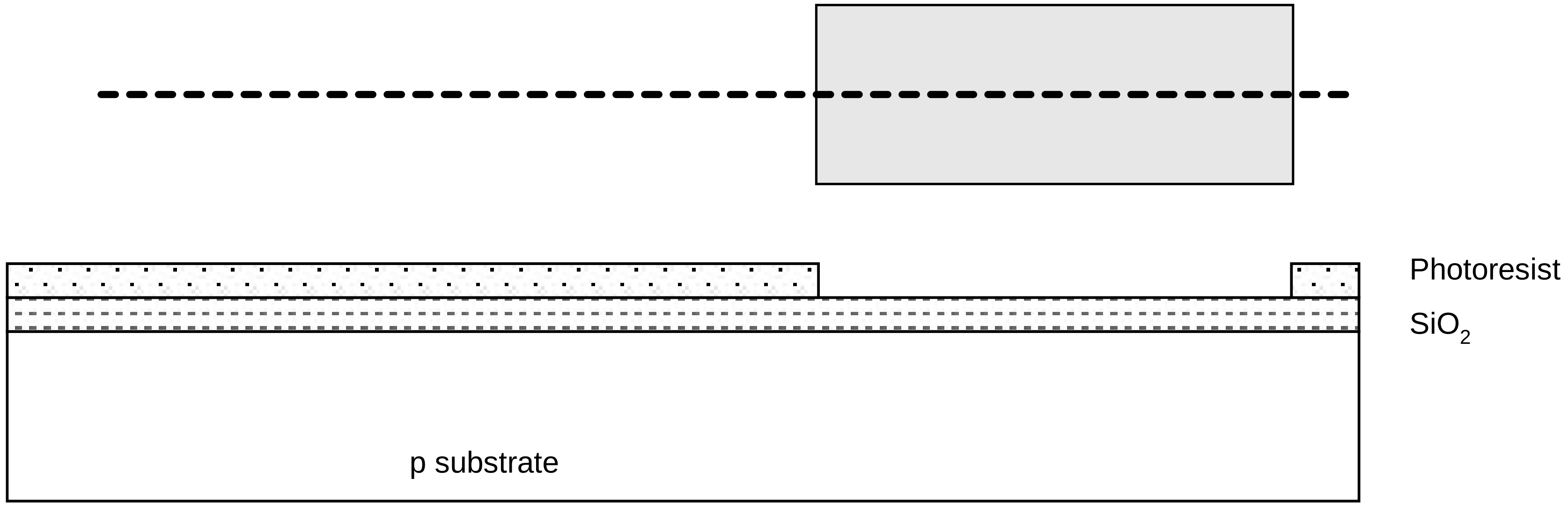
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



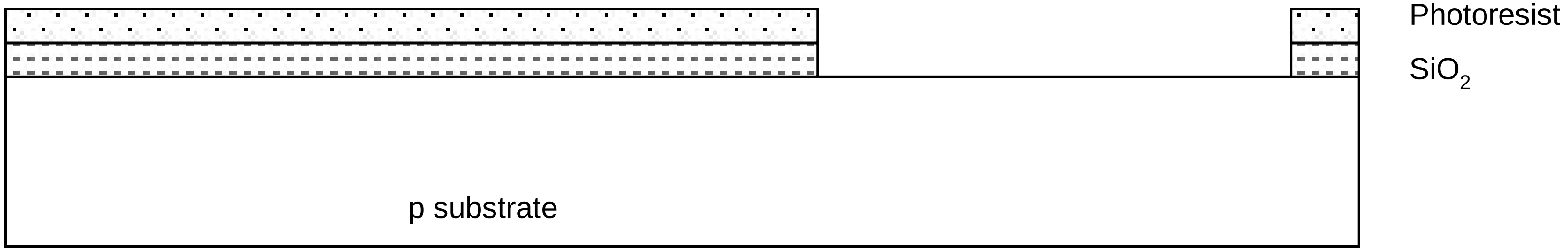
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



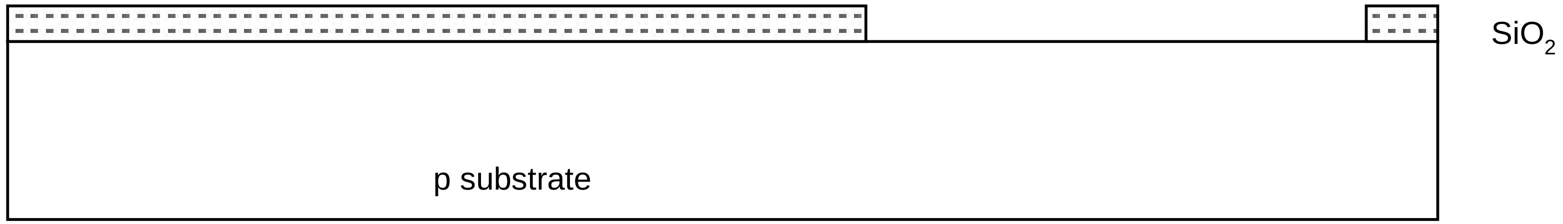
Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed



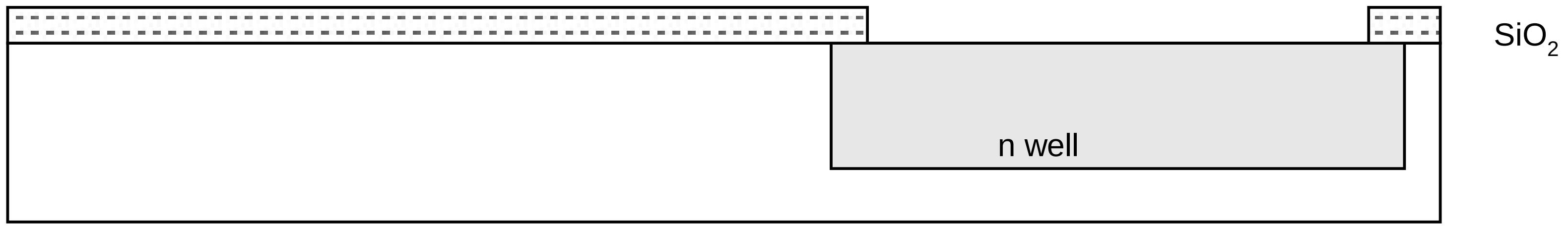
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn't melt in next step



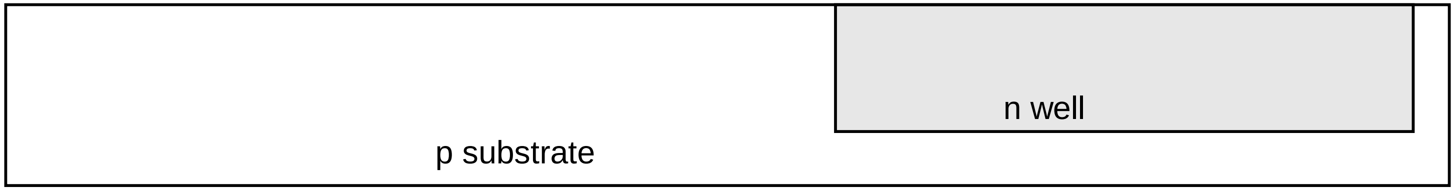
n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implanatation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si



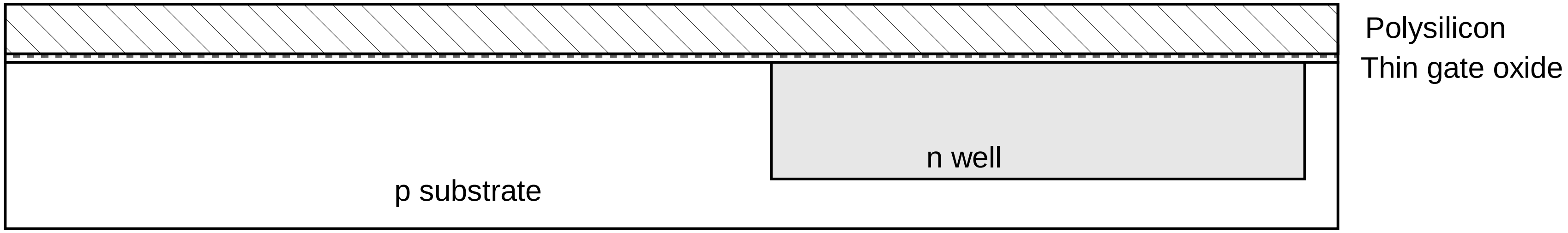
Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps



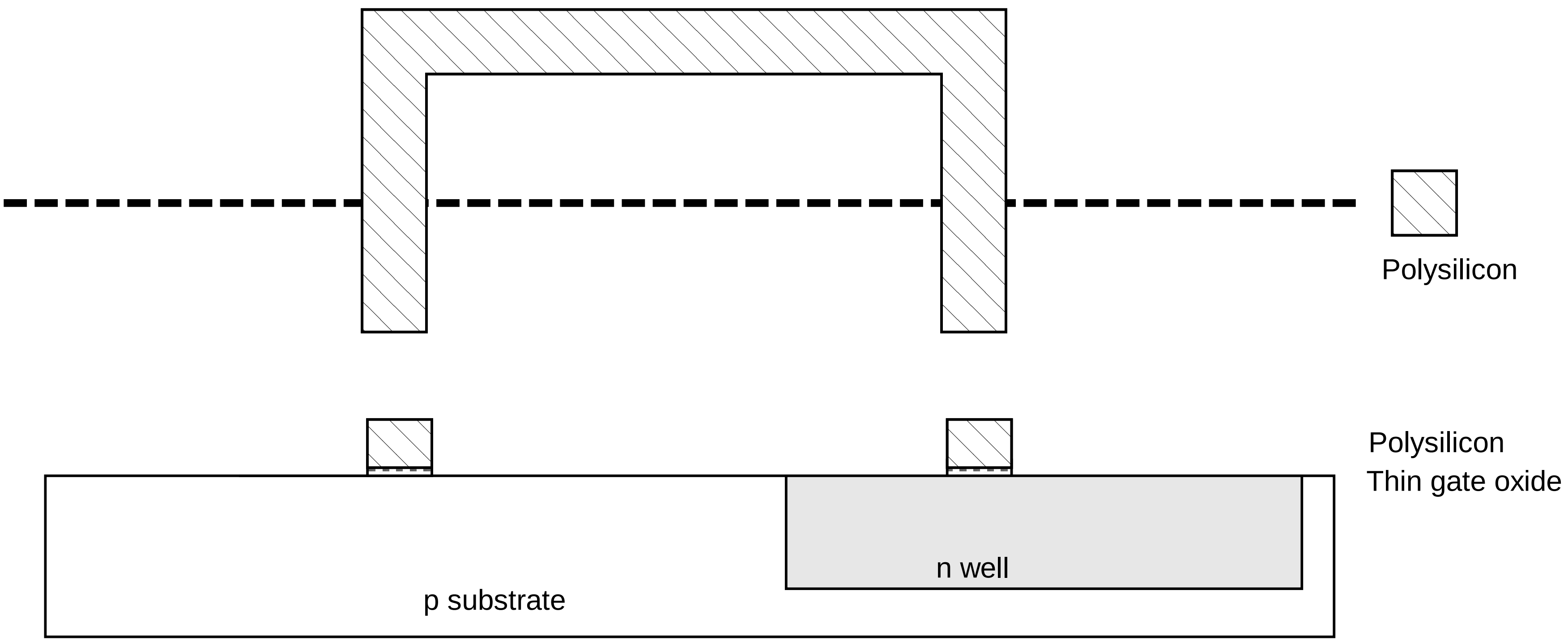
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



Polysilicon Patterning

- Use same lithography process to pattern polysilicon



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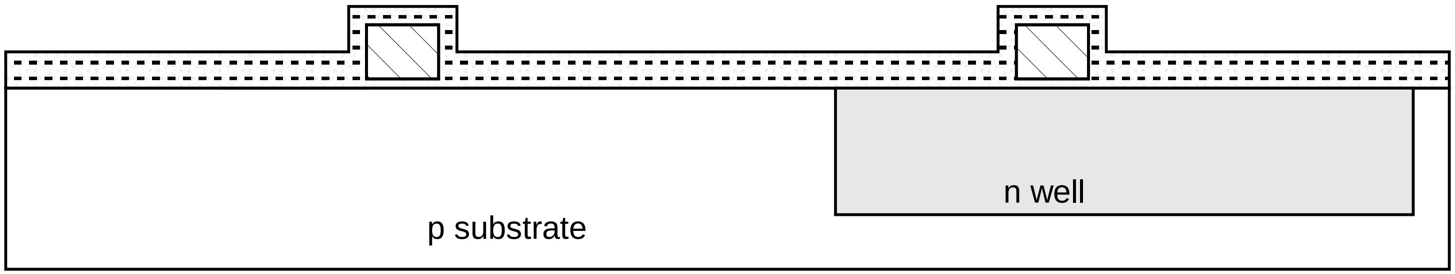
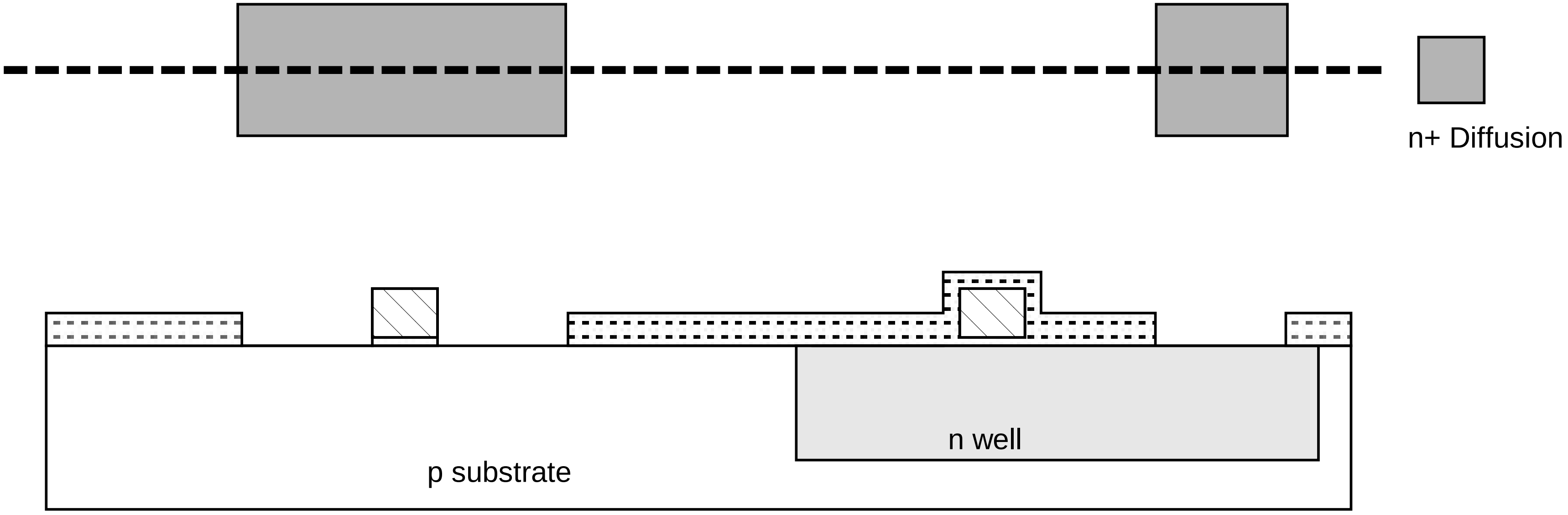
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



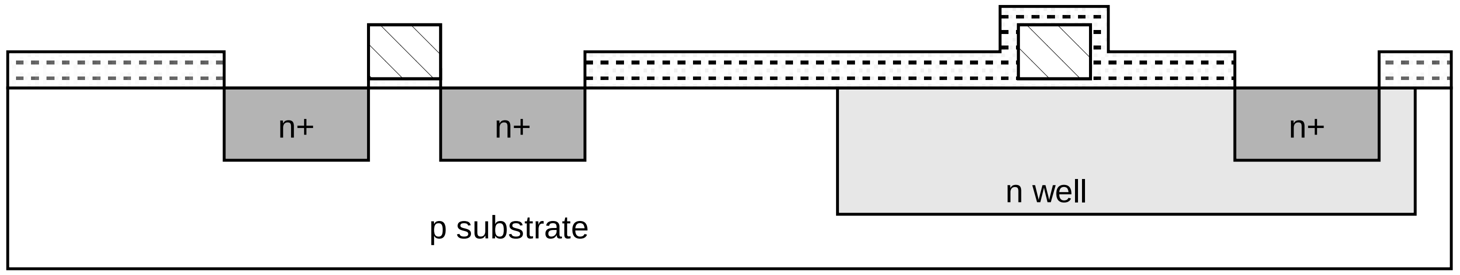
N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



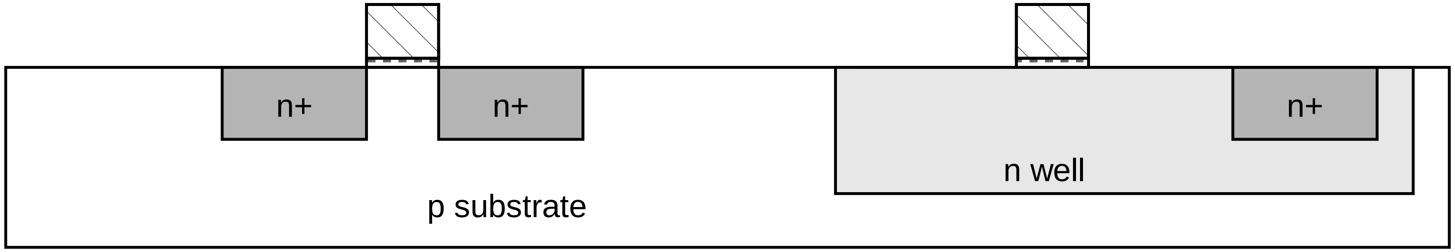
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



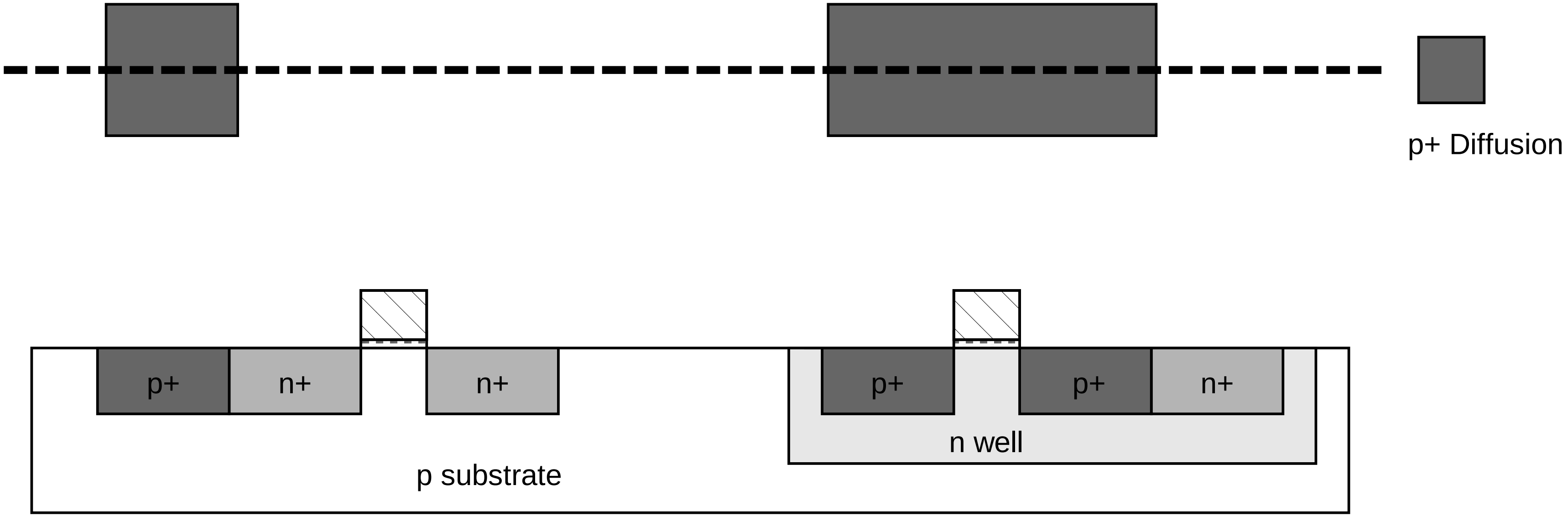
N-diffusion cont.

- Strip off oxide to complete patterning step



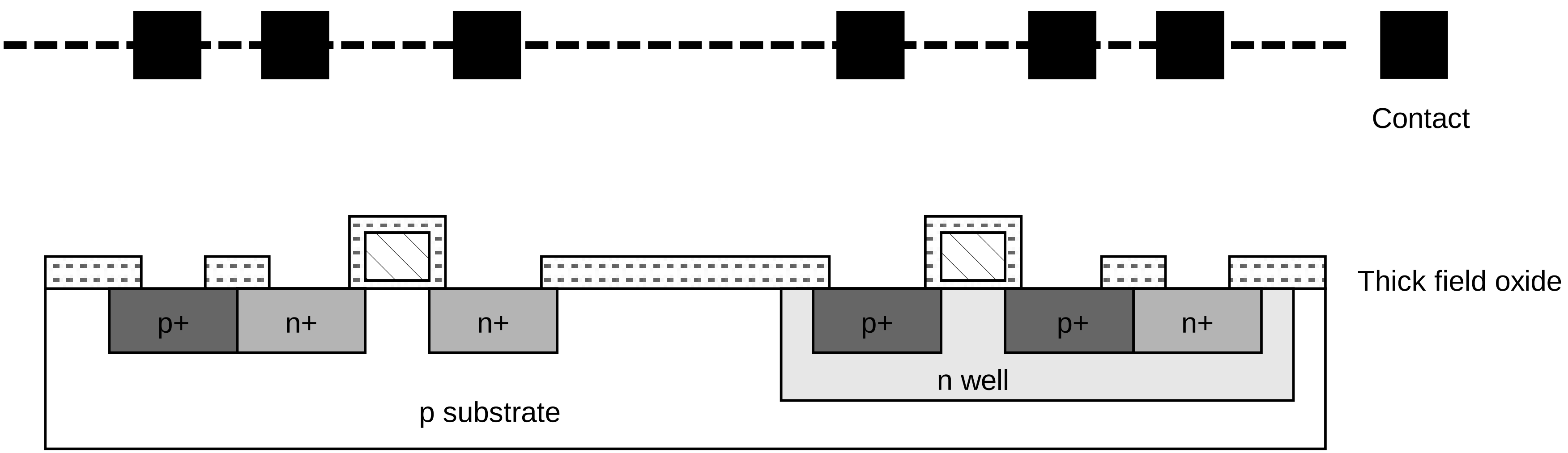
P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



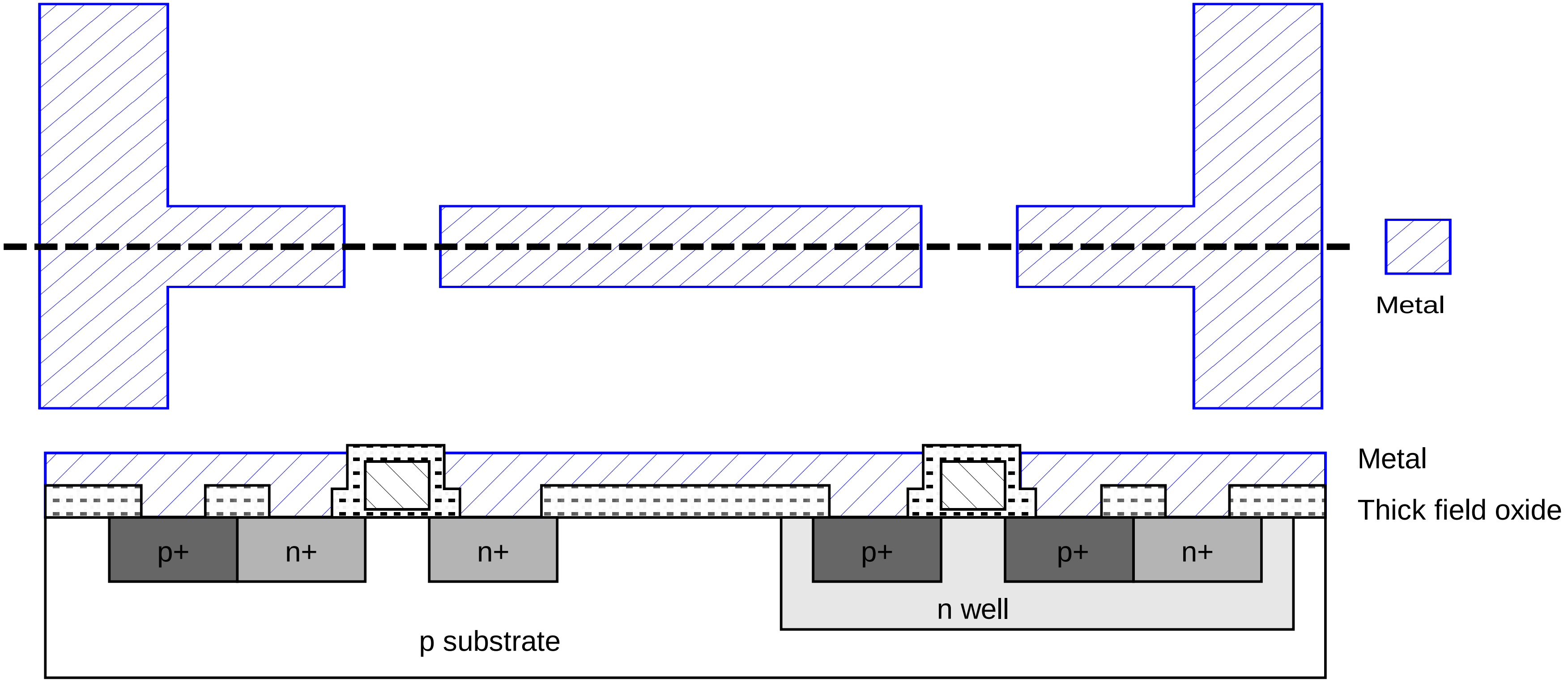
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



Metalization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires

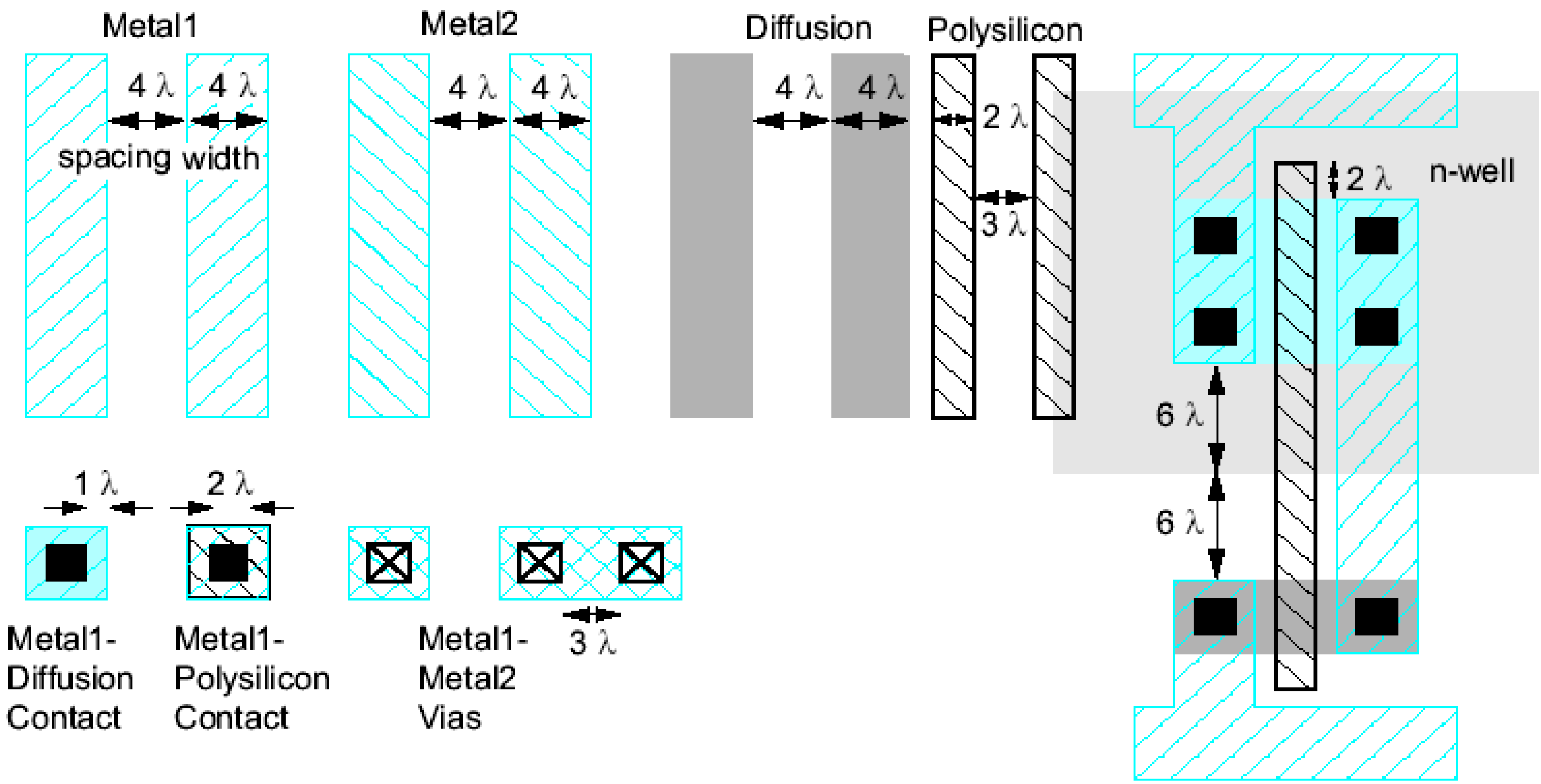


Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size *f* = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. $\lambda = 0.3\ \mu m$ in $0.6\ \mu m$ process

Simplified Design Rules

- Conservative rules to get you started



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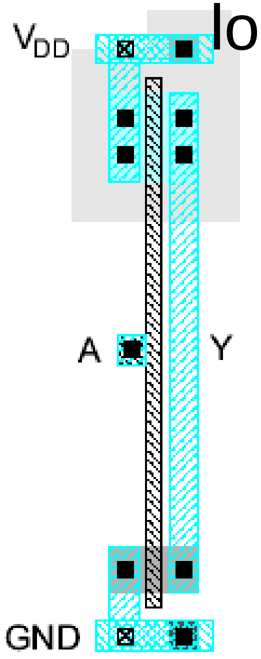
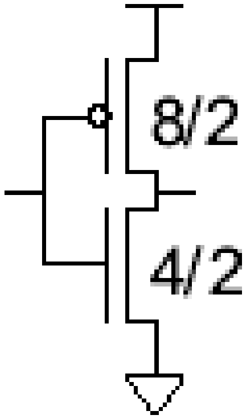
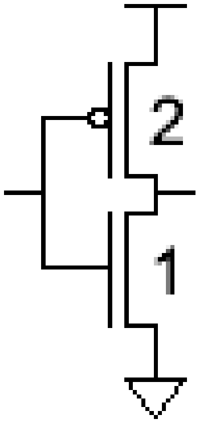
Inverter Layout

- Transistor dimensions specified as Width / Length
  - Minimum size is 4λ / 2λ, sometimes called 1 unit
  - In *f* = 0.6 μm process, this is 1.2 μm wide, 0.6 μm long







Summary

- MOS Transistors are stack of gate, oxide, silicon
- Can be viewed as electrically controlled switches
- Build logic gates out of switches
- Draw masks to specify layout of transistors

- Now you know everything necessary to start designing schematics and layout for a simple chip!