Chapter 2

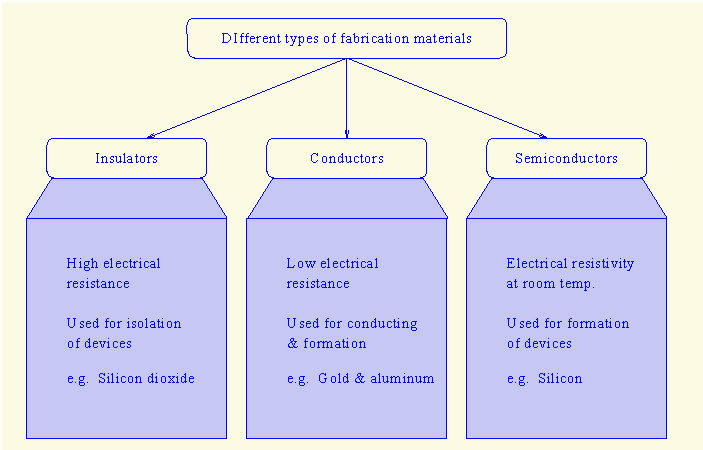
Design and Fabrication of VLSI Devices

Design and Fabrication of VLSI Devices

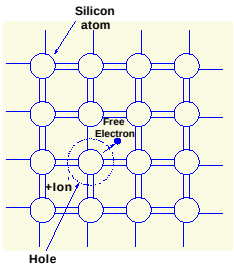
Objectives:

- **To study the materials used in fabrication of VLSI devices.**
- **To study the structure of devices and process involved in fabricating different types of VLSI circuits**

Fabrication Materials

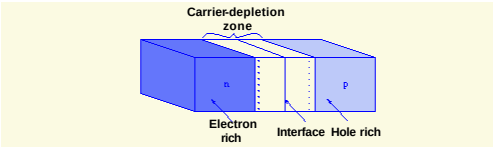


Electron and Holes

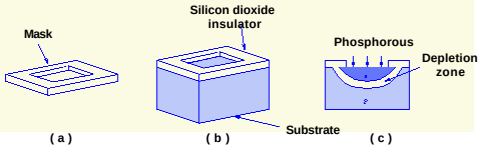


- Holes travel as do electrons
- Material can be enriched in holes or electrons by introducing impurities
- Holes in crystals can be enriched by embedding some boron atoms
- Electrons in Crystals can be enriched by embedding phosphorus atoms

The Three Regions in a n-p Junction

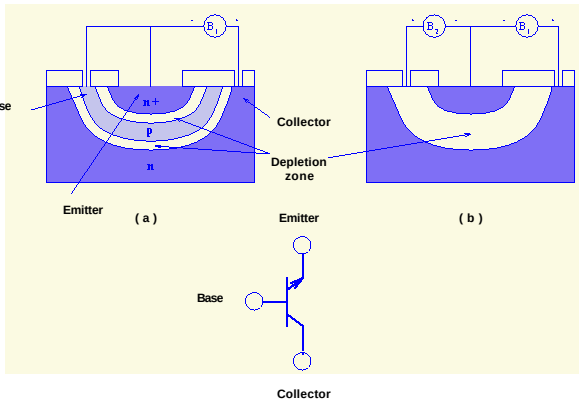


Formation of a Diffused Junction



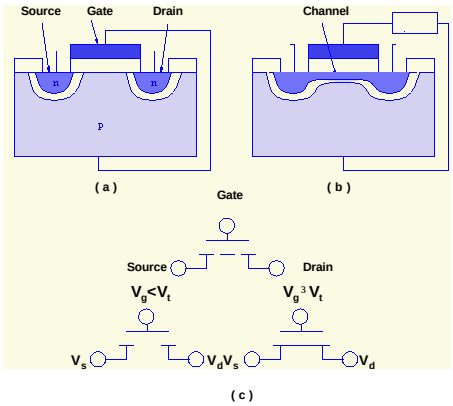
A *mask* is a specification of geometric shapes that need to be created on a certain layer. Masks are used to create a specific patterns of each material in a sequential manner and create a complex pattern of several layers

TTL Transistor



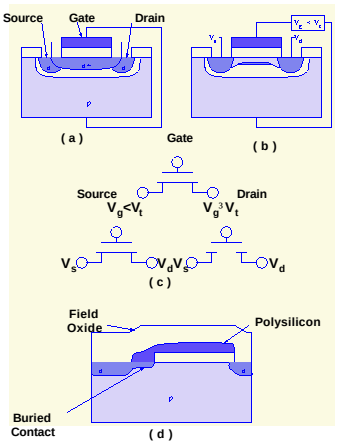
A nMOS Transistor

Enhancement Mode



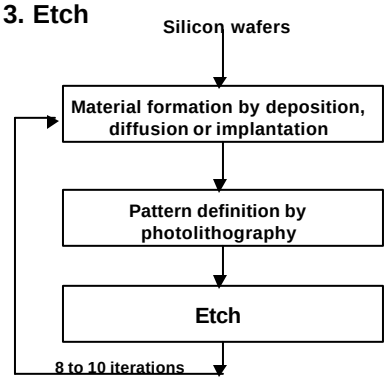
A nMOS Transistor

Depletion Mode



Fabrication of VLSI Circuits

1. Create
2. Define
3. Etch



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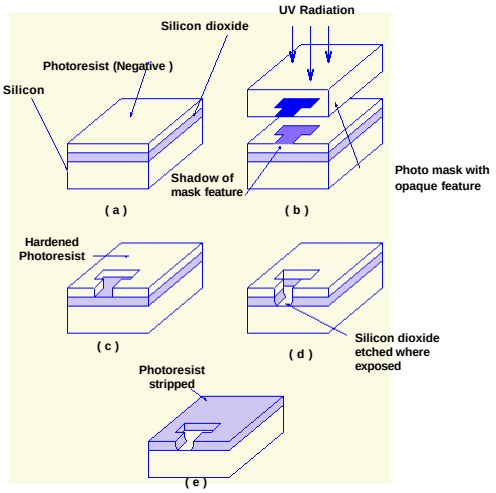
Photolithographic Process



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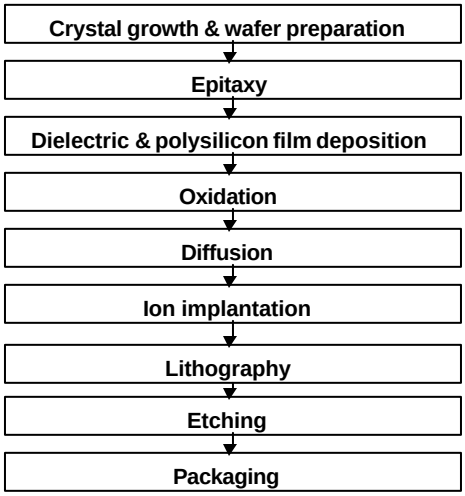
Details of Fabrication Processes



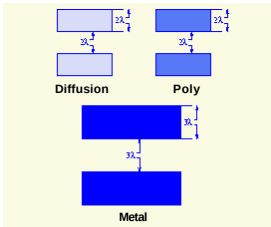
Basic Design Rules

1. **Size Rules**
2. **Separation Rules**
3. **Overlap Rules**

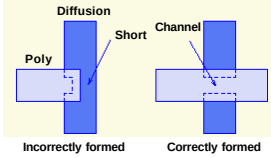
Basic nMOS Design Rules

Diffusion Region Width	2l
Polysilicon Region Width	2l
Diffusion-Diffusion Spacing	3l
Poly-Poly Spacing	2l
Polysilicon Gate Extension	2l
Contact Extension	l
Metal Width	3l

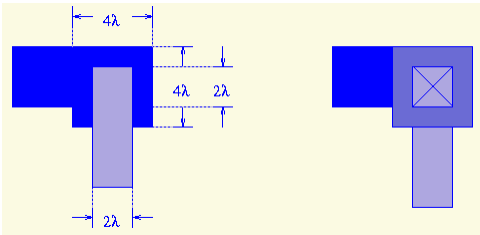
Size and Separation Rules



Incorrectly and Correctly Formed Channels



Overlap Rules for Contact cuts

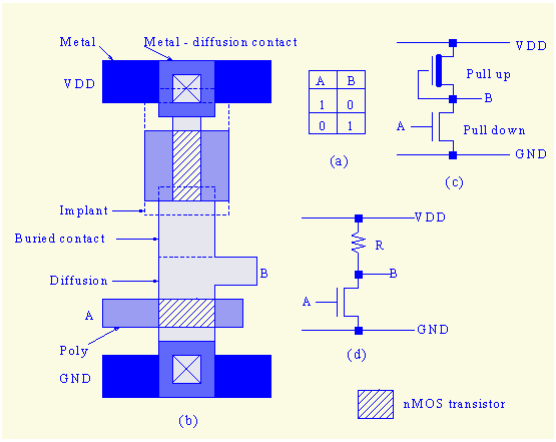


Layout of Basic Devices

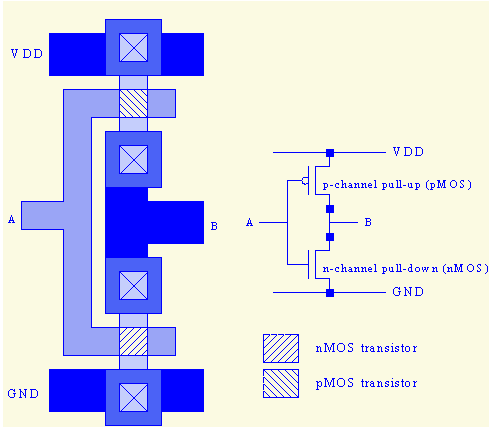
- nMOS Inverter
- CMOS Inverter
- nMOS NAND Gate
- CMOS NAND Gate
- nMOS NOR Gate
- CMOS NOR Gate

Complicated devices are constructed by using basic devices

An nMOS Inverter



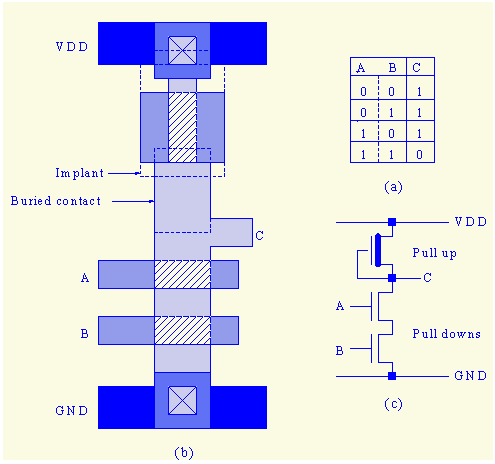
A CMOS Inverter



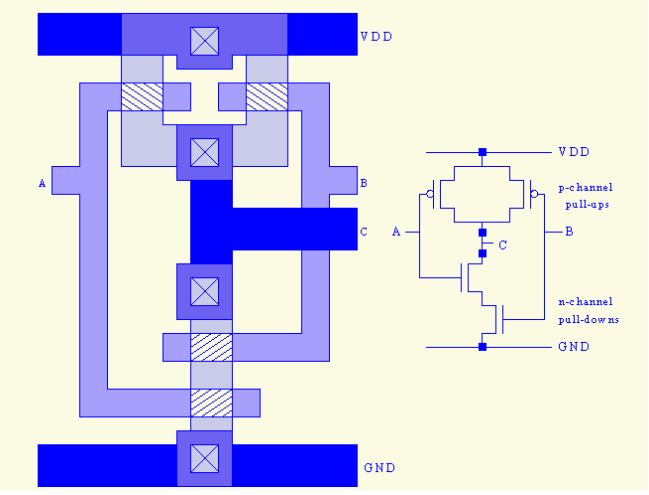
Comparison of CMOS and MOS Characteristics

CMOS	MOS
Zero static power dissipation	Power is dissipated in the circuit with output of gate at "0"
Power dissipated during logic transition	Power dissipated during logic transition
Requires 2N devices for N inputs for complementary static gates	Requires (N+1) devices for N inputs
CMOS encourages regular layout styles	Depletion, load and different driver transistors create irregularity in layout

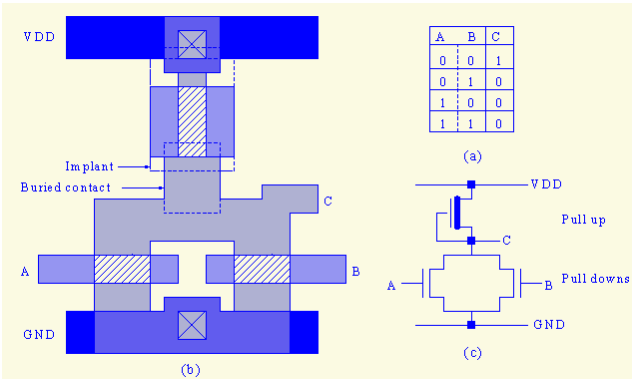
A nMOS NAND Gate



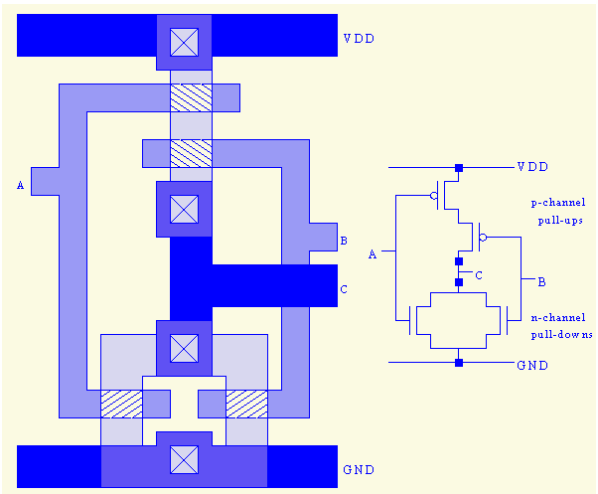
A CMOS NAND Gate



A nMOS NOR Gate



A CMOS NOR Gate



Additional Fabrication Factors

- Scaling
- Parasitic Effects
- Yield Statistics and Fabrication Costs
- Delay Computation
- Noise and Crosstalk
- Power Dissipation

Scaling and Parasitic Effects

The process of shrinking the layout, in which every dimension is multiplied by a factor is called *scaling*

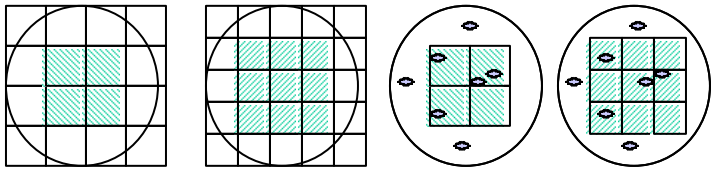
Parameter	Full scaling	CV scaling
Dimensions: width, length, oxid thickness	1/s	1/s
Voltage: power, threshold	1/s	1
Gate capacitance	1/s	1/s
Current	1/s	s
Propagation delay	1/s	$1/s^2$

Parasitic effects includes the stray capacitance, the capacitance between the signal paths and ground, and the inherent capacitance of the MOS transistor

Integrated Circuit Costs

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per Wafer} * \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi * (\text{Wafer\_diam} / 2)^2}{\text{Die Area}} - \frac{\pi * \text{Wafer\_diam}}{\sqrt{2 * \text{Die Area}}} - \text{Test dies} \approx \frac{\text{Wafer Area}}{\text{Die Area}}$$



$$\text{Die Yield} = \frac{\text{Wafer yield}}{\left\{1 + \frac{\text{Defects\_per\_unit\_area} * \text{Die\_Area}}{\alpha}\right\}^{\alpha}}$$

Die Cost is going roughly with (die area)^3 or (die area)^4

Die Yield

Raw Dice Per Wafer

wafer diameter	*die area (mm^2)*					
	100	*144*	*196*	*256*	*324*	*400*
6”/15cm	139	90	62	44	32	23
8”/20cm	265	177	124	90	68	52
10”/25cm	431	290	206	153	116	90
die yield	23%	19%	16%	12%	11%	10%

typical CMOS process: α =2, wafer yield=90%, defect density=2/cm2, 4 test sites/wafer

Good Dice Per Wafer (Before Testing!)

6”/15cm	31	16	9	5	3	2
8”/20cm	59	32	19	11	7	5
10”/25cm	96	53	32	20	13	9

typical cost of an 8”, 4 metal layers, 0.5um CMOS wafer: ~$2000

Real World Examples

Chip	*Metal layers*	*Line width*	*Wafer cost*	*Defect /cm²*	*Area mm²*	*Dies/ wafer*	*Yield*	*Die Cost*
386DX	2	0.90	$900	1.0	43	360	71%	$4
486DX2	3	0.80	$1200	1.0	81	181	54%	$12
PowerPC 601	4	0.80	$1700	1.3	121	115	28%	$53
HP PA 7100	3	0.80	$1300	1.0	196	66	27%	$73
DEC Alpha	3	0.70	$1500	1.2	234	53	19%	$149
SuperSPARC	3	0.70	$1700	1.6	256	48	13%	$272
Pentium	3	0.80	$1500	1.5	296	40	9%	$417

From "Estimating IC Manufacturing Costs," by Linley Gwennap, *Microprocessor Report*, August 2, 1993, p. 15

Other Costs

$$\text{IC cost} = \frac{\text{Die cost} + \text{Testing cost} + \text{Packaging cost}}{\text{Final test yield}}$$

Packaging Cost: depends on pins, heat dissipation

Chip	***Die cost***	***Package pins***	***Package type***	***Package cost***	***Test & Assembly***	***Total***
386DX	**$4**	**132**	**QFP**	**$1**	**$4**	**$9**
486DX2	**$12**	**168**	**PGA**	**$11**	**$12**	**$35**
PowerPC 601	**$53**	**304**	**QFP**	**$3**	**$21**	**$77**
HP PA 7100	**$73**	**504**	**PGA**	**$35**	**$16**	**$124**
DEC Alpha	**$149**	**431**	**PGA**	**$30**	**$23**	**$202**
SuperSPARC	**$272**	**293**	**PGA**	**$20**	**$34**	**$326**
Pentium	**$417**	**273**	**PGA**	**$19**	**$37**	**$473**

RC Parasitic Parameters

$$R = \frac{r l_c}{h_c w_c}$$

r =resistivity, w_c, h_c, and l_c are width, thickness and length of the conductor.

R=resistance of a uniform slab of conducting material.

$$C = \left[1.15\left(\frac{w_c}{t_0}\right) + 2.80\left(\frac{h_c}{t_o}\right)^{0.222}\right] + \left[0.06\left(\frac{w_c}{t_0}\right) + 1.66\left(\frac{h_c}{t_o}\right) - 0.14\left(\frac{h_c}{t_o}\right)^{0.222}\right]\left(\frac{t_0}{w_{ic}}\right)^{1.34} e_s e_0 l_c$$

C=capacitance of the conductor, w_{ic}= spacing of chip interconnections,

t_0= thickness of the oxide, e_s= permitivity of free space,

e_0= dielectric constant of the insulator

Noise Crosstalk

Noise principally stems from capacitive and inductive coupling.

One of the forms of noise is crosstalk, which is a result of mutual capacitance and inductance between neighboring lines

Power Dissipation

- Temperature must be as uniform as possible over the entire chip surface.
- Heat generated must be efficiently removed from the chip surface
- A CMOS gate uses 0.003nW/MHz/gate in 'off' state and 0.8 mW/MHz/gate during its operation.
- A ECL system uses 25 mW/gate irrespective of state and operating frequency

Summary

- The three types of materials are insulators, conductors and semiconductors
- A VLSI chip consists of several layers of different materials on a silicon wafer.
- Each layer is defined by a mask
- VLSI fabrication process patterns each layer using a mask
- Complex VLSI circuits can be developed using basic VLSI devices
- Design rules must be followed to allow proper fabrication
- Several factors such as scaling, parasitic effects, yield statistics and fabrication costs, delay computation, noise and crosstalk and power dissipation play a key role in fabrication of VLSI chips