Course Structure & Scheme

For

Master of Technology

In

VLSI Design

Guru Gobind Singh Indraprastha University
Kashmere Gate, Delhi – 6 [INDIA]
www.ipu.ac.in

w.e.f. 2004 - 2005

Eligibility Condition

1. B. Tech / B.E in Electronics & Communication / Electronics / Computer Science/Information Technology or equivalent degree with 60% marks.

2. MSc (Electronics) with 60% marks.

Admission Procedure

1. Admission will be made on the basis of GATE score in the relevant field.

2. If seats remain vacant after admitting the students with valid GATE score, then the admission will be made on the basis of merit of the qualifying marks subject to minimum 60% marks in the qualifying degree.

SCHEME OF EXAMINATION
M.Tech. (VLSI Design)

First Semester Examination

Course Code	Subject Name	L/P	Credits
Theory Papers			
ITV-601	Advanced Computer Architecture	3	3
ITV-603	VLSI Technology	3	3
ITV-605	MOS Circuit Design	3	3
ITV-607	Solid State Electronics Devices	3	3
ITV-609	Digital System Design	3	3
ITV-611	Data Structure & Algorithm Analysis	3	3
Practicals/Viva-voce			
ITV-651	Lab – I	4	2
ITV-653	Lab – II	4	2
ITV-655	Lab - III	4	2
Total		**30**	**24**

SCHEME OF EXAMINATION
M.Tech. (VLSI Design)

Second Semester Examination

Course Code	Subject Name	L/P	Credits
Theory Papers			
ITV-602	Analog VLSI Design	3	3
ITV-604	Computational Methods	3	3
ITV-606	Digital Signal Processing	3	3
Electives (Choose any TWO)			
ITV-608	CMOS RF Circuit Design	3	3
ITV-610	VLSI Test & Testability	3	3
ITV-612	Low Power VLSI Design	3	3
ITV-614	Cluster & Grid Computing	3	3
ITV-616	Embedded System Design	3	3
ITV-618	Designing with ASICS	3	3
ITV-620	Real Time System & Software	3	3
ITV-622	Neural Networks	3	3
ITV-624	Digital Logic with Verilog	3	3
ITV-626	Microwave & Optoelectronic Devices	3	3
ITV-628	Project Work	3	3
Practicals/Viva-voce			
ITV-652	Lab – IV	4	2
ITV-654	Lab – V	4	2
ITV-656*	Minor Project - I	4	4
Total		**27**	**23**

*** NUES - Non University Exam System**

SCHEME OF EXAMINATION
M.Tech. (VLSI Design)

Third Semester Examination

Course Code	Subject Name	L/P	Credits
Theory Papers			
ITV-701	Algorithms for VLSI Design Automation	3	3
Electives (Choose any TWO)			
ITV-703	Process, Devices & Circuit Simulation	3	3
ITV-705	Nano Technology	3	3
ITV-707	Hardware-Software Co-design	3	3
ITV-709	Digital Image Processing	3	3
ITV-711	Cryptology and Crypto Chip Design	3	3
ITV-713	Genetic Algorithm	3	3
ITV-715	Bluetooth Technology	3	3
ITV-717	MEMS and IC Integration	3	3
ITV-719	Computer Aided VLSI Design	3	3
ITV-721	Design of VLSI System	3	3
ITV-723	Advanced Computational Methods	3	3
ITV-725	Project work	3	3
Practicals/Viva-voce			
ITV-751	Lab – VI	4	2
ITV-753	Lab – VII	4	2
ITV-755*	Seminar	0	2
ITV-757	Minor Project - II	4	8
Total		**21**	**23**

*** NUES - Non University Exam System**

SCHEME OF EXAMINATION
M.Tech. (VLSI Design)

Fourth Semester Examination

Code No.	Paper	L/P	Credits
ITV-752	Dissertation	30	30
ITV-754*	Seminar & Progress Report	10	03
ITV-756*	Comprehensive Viva	-	02
Total		**40**	**35**

***Non University Exam System**

NOTE:

1. The total number of credits of the Programme M. Tech. = 105.
2. Each student shall be required to appear for examination in all courses. However, for the award of the degree a student shall be required to earn the minimum of 100.

Elective course will be offered only if 40% students will opt for a particular course.

Code No. ITV-601	**L**	**C**
Paper: Advanced Computer Architecture	**3**	**3**

Parallel computer models:
The state of computing, Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers.
Program and network properties:
Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms
System Interconnect Architectures:
Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.
Advanced processors:
Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors
Pipelining:
Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines
Memory Hierarchy Design:
Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.
Multiprocessor architectures:
Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization,
Scalable point –point interfaces: Alpha364 and HT protocols, high performance signaling layer.
Enterprise Memory subsystem Architecture:
Enterprise RAS Feature set: Machine check, hot add/remove, domain partitioning, memory mirroring/migration, patrol scrubbing, fault tolerant system.
Text:
1. Kai Hwang, “Advanced computer architecture”; TMH.
2. D. A. Patterson and J. L. Hennessey, “Computer organization and design,” Morgan Kaufmann, 2nd Ed.
References:
1. J.P.Hayes, “computer Architecture and organization”; MGH.
2. Harvey G.Cragon,”Memory System and Pipelined processors”; Narosa Publication.

3. V.Rajaranam & C.S.R.Murthy, "Parallel computer"; PHI.
4. R.K.Ghose, Rajan Moona & Phalguni Gupta, "Foundation of Parallel Processing"; Narosa Publications.
5. Kai Hwang and Zu, "Scalable Parallel Computers Architecture"; MGH.
6. Stalling W, "Computer Organisation & Architecture";PHI.
7. D.Sima, T.Fountain, P.Kasuk, "Advanced Computer Architecture-A Design space Approach,"Addison Wesley,1997.
8. M.J Flynn, "Computer Architecture, Pipelined and Parallel Processor Design"; Narosa Publishing.
9. D.A.Patterson, J.L.Hennessy, "Computer Architecture :A quantitative approach";Morgan Kauffmann feb,2002.
10. Hwan and Briggs, " Computer Architecture and Parallel Processing"; MGH.VLSI

Code No. ITV-603	**L**	**C**
Paper: VLSI Technology	**3**	**3**

Crystal growth & wafer preparation. Processing considerations: Chemical cleaning, getting the thermal Stress factors etc.

Epitaxy

Vapors phase Epitaxy Basic Transport processes & reaction kinetics, doping & auto doping, equipments, & safety considerations, buried layers, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics, SOI structure.

Oxidation

Growth mechanism & kinetics, Silicon oxidation model, interface considerations, orientation dependence of oxidation rates thin oxides. Oxides. Oxidation technique & systems dry & wet oxidation. Masking properties of SiO2.

Diffusion

Diffusion from a chemical source in vapor form at high temperature, diffusion from doped oxide source, diffusion from an ion implanted layer.

Lithography

Optical Lithography: optical resists, contact & proximity printing, projection printing, electron lithography: resists, mask generation. Electron optics: roster scans & vector scans, variable beam shape. X-ray lithography: resists & printing, X ray sources & masks. Ion lithography.

Etching

Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & apostrophic etching, ion enhanced & induced etching, properties of etch processing. Reactive Ion Beam etching, Specific etches processes: poly/polycide. Trench etching,

Text:

1. Sze, ” Modern Semiconductor Device Physics”, John Wiley & Sons, 2000.

References:

1. B.G. Streetman, “Solid State Electronics Devices”, Prentice Hall, 2002.
2. Chen, “VLSI Technology” Wiley, March 2003.

Code No. ITV-605 **L** **C**
Paper: MOS Circuit Design **3** **3**

Introduction:
Basic principle of MOS transistor, Introduction to large signal MOS models (long channel) for digital design.

The MOS Inverter:
Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Propagation Delay, Power Consumption.

MOS Circuit Layout & Simulation:
MOS SPICE model, device characterization, Circuit characterization, interconnects simulation. MOS device layout: Transistor layout, Inverter layout, CMOS digital circuits layout & simulation

Combinational MOS Logic Design
Static MOS design: Complementary MOS, Ratioed logic, Pass Transistor logic, complex logic circuits.

Dynamic MOS design: Dynamic logic families and performances.

Sequential MOS Logic Design
Static latches, Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. Memory Design: ROM & RAM cells design

Interconnect & Clock Distribution
Interconnect delays, Cross Talks, Clock Distribution. Introduction to low power design, Input and Output Interface circuits.

BiCMOS Logic Circuits
Introduction, BJT Structure & operation, Basic BiCMOS Circuit behavior, Switching Delay in BiCMOS Logic circuits, BiCMOS Applications

Text:
1. Kang & Leblebigi “CMOS Digital IC Circuit Analysis & Design”- McGraw Hill, 2003
2. Rabey, “Digital Integrated Circuits Design”, Pearson Education, Second Edition, 2003

Reference:
1. Weste and Eshraghian, “Principles of CMOS VLSI design” Addison-Wesley, 2002

Code No. ITV-607	**L**	**C**
Paper: Solid State Electronics Devices	**3**	**3**

Semi-conductor materials- Crystal lattices, bulk crystal growth, epitaxial growth, Physical models-bohr model, quantum mechanics, atomic structure, energy bands & charge carriers in semic-conductors, carrier concentration, drift of carriers in electric and magnetic fields, diffusion of carriers.

Fabrication of P-N junctions, equilibrium conditions, forward and revers biased junctions, steady state conditions, reverse bias breakdown, transient and a.c. condition, deviation from simple theory, metal semi-conductor junction, heterojunction

P-N junction diodes, tunnel diode, photo diode, light emitting diodes and lasers. BJTs: amplification & switching: Fundamental of BJT operation, BJT fabrication, minority carier distribution & terminal currents, generalized biasing, switching, frequency limitation of transistors, heterojuction bipolar transistor, FETs: junction FET-metal semi-conductor FET-Metal insulator semiconductor FET.

Integrated circuits: fabrication of monolithic circuits, monolithic device elements, charge transfers devices, very large scale integration, testing, bonding and packaging

Lasers: stimulated emission: ruby lasers, semi-conductor lasers, other lasers, p-n-p-n switching devices, switching mechanicsm: semiconductor controller rectifier, negative conductance, Microwave devices: Transit time devices: Gunn effect and related devices.

Text/References:

1. Ben G Steetman, “Solid State Electronic Devices” PHI
2. S M Sze, “Physics of semiconductor Devices”, Willey Pub.
3. Kittel C, “Introduction to Solid State Physics”, Willey Pub.

Code No. ITV-609	**L**	**C**
Paper: Digital System Design	**3**	**3**

Specification of combinational systems using VHDL, Introduction to VHDL, Basic language element of VHDL, Behavioral Modeling, Data flow modeling, Structural modeling, Subprograms and overloading, VHDL description of gates.

Description and design of sequential circuits using VHDL, Standard combinational modules, Design of a Serial Adder with Accumulator, State Graph for Control Network, design of a Binary Multiplier, Multiplication of a Signed Binary Number, Design of a Binary Divider.

Register- transfer level systems, Execution Graph, Organization of System, Implementation of RTL Systems, Analysis of RTL Systems, Design of RTL Systems.

Data Subsystems, Storage Modules, Functional Modules, Data paths, Control Subsystems, Micro programmed Controller, Structure of a micro programmed controller, Micro instruction Format, Micro instruction sequencing, Micro instruction Timing, Basic component of a micro system, memory subsystem.

I/O subsystem, Processors, Operation of the computer and cycle time. Binary Decoder, Binary Encoder, Multiplexers and Demultiplexers,

Floating Point Arithmetic-Representation of Floating Point Number, Floating Point Multiplication.

Text:

1. J. Bhaskar, " A VHDL Primer", Addison Wesley, 1999.
2. M. Ercegovac, T. Lang and L.J. Moreno, "Introduction to Digital Systems", Wiley,2000
3. C. H. Roth, "Digital System Design using VHDL", PWS Publishing

References:

1. J.F. Wakerly, "Digital Design-Principles and Practices", PHL
2. Douglas Perry, "VHDL", MGH
3. Michae John Sebastian Smith, "Application-Specific Integrated Circuits", Addison-Wesley.
4. Z. Navabi, " VHDL-Analysis and Modeling of Digital Systems", MGH

Code No. ITV-611 | **L** | **C**
Paper: Data structure & Algorithm Analysis | **3** | **3**

	L	C
Code No. ITV-611	**L**	**C**
Paper: Data structure & Algorithm Analysis	**3**	**3**

Arrays:
Representation and basic operations, Linked list : Singly linked list, Doubly linked list and Circular linked list- definition, representation and their basic operation, Stacks and queues : insertion, deletion, Trees : Binary Search trees, AVL trees, B-trees and B+ trees: insertion, deletion, traversal (in order, preorder and post order)

Introduction to algorithm Design:
Growth of functions, Summations and Recurrences, The substitution method, the iteration method, the master method, Divide and Conquer paradigm, Dynamic programming, Greedy Algorithms.

Sorting and Order Statistics: Merge Sort, Heap sort, Quick sort, Priority Queues

Searching and Disjoint Sets:
Hash Tables, Binary Search Trees, Red-Black trees, Disjoint-set Operations - Linked list representation of disjoint sets, Disjoint set forests,

Graph Algorithms:
Representation of Graphs, Breadth First Search, Depth First Search, Topological Sort, Spanning Tree Algorithm - Kruskal's and Prim's, Shortest path Algorithm - Dijkstra's and Bellman Fort Algorithm for single pair Shortest paths, Floyd-Warshall algorithm for All pair Shortest path, Matrix multiplication modeling of All pairs shortest path problem, Min cut and Max cut Algorithms

String matching:
The naïve String Matching algorithm - Rabin-Karp Algorithm, String Matching with finite automata -Knuth Marris Pratt algorithm.

NP-Complete Problem:
Polynomial-time non-deterministic algorithms, NP-Completeness and Reducibility,NP-Completeness Proof and NP Complete problems.

Text:
1. T .H. Cormen, C. E. Leiserson, R. L. Rivest "Introduction to Algorithms", PHI.

References:
1. A .V. Aho, J . E . Hopcroft, J . D . Ulman "The Design & Analysis of Computer Algorithms", Addison Wesley.
2. V . Manber "Introduction to Algorithms – A Creative Approach", Addison Wesley.
3. Ellis Harwitz and Sartaz Sahani "Fundamentals of Computer Algorithms", Computer Science Press.
4. A. Tanenbaum, Y. Langsam and A. J. Augenstein "Data Structures Using C and C++" Prentice Hall of India.
5. Peter Linz, "An Introduction to Formal Languages and Automata", Narosa Publishing House.
6. J.E.Hopcroft & J.D.Ullman, "Introduction to Automata Theory, Languages and Computation", Addison Wesley.
7. K.L.Mishra & N.Chandrasekaran, "Theory of Computer Science", PHI.
8. John C.Martin, "Introduction to Languages and Theory of Computation", TMH

Code No: ITV-651	**P**	**C**
Lab : Lab - I	**4**	**2**

Experiment of the lab will be based on Following Paper:

Digital System Design

Code No: ITV-653	**P**	**C**
Lab : Lab – II	**4**	**2**

Experiment of the lab will be based on the following paper:

MOS Circuit Design

Code No: ITV-655	**P**	**C**
Lab : Lab – III	**4**	**2**

Experiment of the lab will be based on the following paper:

Data structure & Algorithm Analysis Design

Code No: ITV-602	**L**	**C**
Subject: Analog VLSI Design	**3**	**3**

Small Signal & large signal Models of MOS & BJT transistor. Analog MOS Process (Double Poly Process)

MOS & BJT Transistor Amplifiers:

Single transistor Amplifiers stages: Common Emitter, Common base, Common Collector, Common Drain, Common Gate & Common Source Amplifiers

Multiple Transistor Amplifier stages: CC-CE, CC-CC, & Darlington configuration, Cascode configuration, Active Cascode. Differential Amplifiers: Differential pair & DC transfer characteristics.

Current Mirrors, Active Loads & References

Current Mirrors: Simple current mirror, Cascode current mirrors Widlar current mirror, Wilson Current mirror, etc. Active loads, Voltage & current references. Analysis of Differential Amplifier with active load, supply and temperature independent biasing techniques, Frequency Response,

Operational Amplifier:

Applications of operational Amplifier, theory and Design; Definition of Performance Characteristics; Design of two stage MOS Operational Amplifier, two stage MOS operational Amplifier with cascodes, MOS telescopic-cascode operational amplifiers, MOS Folded-cascode operational amplifiers, Bipolar operational amplifiers. Frequency response & compensation.

Nonlinear Analog Circuits:

Analysis of four quadrant and variable Tran conductance multiplier, Voltage controlled oscillator, Comparators, Analog Buffers, Source Follower and Other Structures. Phase Locked Techniques; Phase Locked Loops (PLL), closed loop analysis of PLL. Digital-to-Analog (D/A) and Analog-to-Digital (A/D) Converters

OTA & Switched Capacitor filters

OTA Amplifiers. Switched Capacitor Circuits and Switched Capacitor Filters.

Text:

1. Paul B Gray and Robert G Meyer, “Analysis and Design of Analog Integrated Circuits”.
2. Behzad Razavi, “Principles of data conversion system design”, S.Chand and company Ltd, 2000. John Wiley

References:

1. D. A. Johns and Martin, Analog Integrated Circuit Design, John Wiley, 1997.
2. R Gregorian and G C Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley, 1986.
3. R L Geiger, P E Allen and N R Strader, VLSI Design Techniques for Analog & Digital Circuits, McGraw Hill, 1990.
4. Gray and Meyer,” Analysis and Design of Analog IC ”, Wiley international,1996.
5. Gray, Wooley, Brodersen, “Analog MOS Integrated circuits”, IEEE press, 1989.
6. Kenneth R. Laker, Willy M.C. Sensen, “ Design of Analog Integrated circuits and systems”, McGraw Hill, 1994.

Code No: ITV-604	**L**	**C**
Subject: Computational Methods	**3**	**3**

Functions, polynomials and their zeros. Bracketing of a root. Bisection and Newton - Raphson methods and their convergence. Iterative method for equations of the form $x = \phi(x)$.

Interpolating polynomial. Lagrange form with error. Divided differences. Hermite interpolation, Numerical differentiation and integration. Gauss quadrature. Romberg integration.

Solution of a system of linear algebraic equations by Gauss elimination and Gauss seidel methods. LU decomposition. Solution of a tridiagonal systems. Eigenvalue problem-largest and smallest eigenvalues by interation. Method of least squares.

Solution of initial value problems by Runge-Kutta, Predictor – corrector and Adam – Bashforth methods. Finite difference method for boundary value problems in ODE. Shooting method.

Solution of Laplace and Poisson equations by finite difference method (Dirichlet problem)

Text/References:

1. Kreyszig, E, "Advanced Engineering Mathematics", John Wiley, 8th ed., 2002.
2. Chapra, S.C, Canale R P "Numerical Methods for Engineers" 3rd Ed., McGraw-Hill 1998.
3. Gerald, C.F., "Applied Numerical Analysis", 6th Ed., Pearson, 1999.
4. Niyogi, P. "Numerical Analysis and Algorithms", TMH, 2003.
5. Conte, S.D. de Boor, C. "Elementary Numerical Analysis" McGraw-Hill.

Code No : ITV - 606 **L**
Subject: Digital Signal Processing **3**

Discrete time signals and systems, Z-transforms, structures for digital filters, design procedures for FIR and IIR filters. Frequency transformations: linear phase design; DFT. Methods for computing FFT. Noise analysis of digital filters, power spectrum estimation.

Signals and signal Processing: characterization & classification of signals, typical Signal Processing operations, example of typical Signals, typical Signals Processing applications.
Time Domain Representation of Signals & Systems: Discrete Time Signals, Operations on Sequences, the sampling process, Discrete-Time systems, Time-Domain characterization of LTI Discrete-Time systems, state-space representation of LTI Discrete-Time systems, random signals.
Transform-Domain Representation of Signals: the Discrete-Time Fourier Transform, Discrete Fourier Transform, DFT properties, computation of the DFT of real sequences, Linear Convolution using the DFT. Z-transforms, Inverse z-transform, properties of z-transform, transform domain representations of random signals.

Transform-Domain Representation of LTI Systems: the frequency response, the transfer function, types of transfer function, minimum-phase and maximum-Phase transfer functions, complementary transfer functions, Discrete-Time processing of random signals.

Digital Processing of Continuous-Time Signals : sampling of Continuous Signals, Analog Filter Design, Anti-aliasing Filter Design, Sample-and-hold circuits, A/D & D/A converter, Reconstruction Filter Design.

Digital Filter Structure: Block Diagram representation, Signal Flow Graph Representation, Equivalent Structures, bone FIR Digital Filter Structures, IIR Filter Structures, State-space structure, all pass filters, tunable IIR Digital filters. cascaded Lattice realization of IIR and FIR filters, Parallel all pass realization of IIR transfer function, Digital Sine-Cosine generator.

Digital Filter Design: Impulse invariance method of IIR filter design, Bilinear Transform method of IIR Filter Design, Design of Digital IIR notch filters, FIR filter Design based on truncated fonner sens, FIR filter design based on Frequency Sampling approach.

Applications of DSP.

Text / Reference:

1. Sanjit K. Mitra, “Applications DSP a Computer based approach” , TMH.
2. Allan Y. Oppenhein & Ronald W. Schater , "Digital Signal Processing”, PHI

Code No: ITV-608	**L**	**C**
Subject : CMOS RF Circuit Design	**3**	**3**

Introduction to RF design and Wireless Technology:
Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion.

RF Modulation
Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures. Direct conversion and two-step transmitters.

RF Testing
RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

BJT and MOSFET Behavior at RF Frequencies
BJT and MOSFET behavior at RF frequencies, Modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation

RF Circuits Design
Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

Text:

1. Thomas H. Lee "Design of CMOS RF Integrated Circuits" Cambridge University press 1998.

References:

1. B. Razavi "RF Microelectronics" PHI 1998
2. R. Jacob Baker, H.W. Li, D.E. Boyce " CMOS Circiut Design, layout and Simulation" PHI 1998
3. Y.P. Tsividis "Mixed Analog and Digital Devices and Technology" TMH 1996

Code No: ITV-610	**L**	**C**
Subject: VLSI Test & Testability	**3**	**3**

The need for testing, the problems of digital and analog testing, Design for test, Software testing
Faults in Digital circuits:General introduction, Controllability and Observability.. Fault models - Stuck-at faults, Bridging faults, intermittent faults

Digital test pattern generation :Test pattern generation for combinational logic circuits, Manual test pattern generation, Automatic test pattern generation - Roth's D-algorithm, Developments following Roth's D-algorithm, Pseudorandom test pattern generation, Test pattern generation for sequential circuits , Exhaustive, non-exhaustive and pseudorandom 70 test pattern Generation, Delay fault testing

Signatures and self test: Input compression Output compression Arithmetic, Reed-Muller and spectral coefficients, Arithmetic and Reed-Muller coefficients ,Spectral coefficients, Coefficient test signatures ,Signature analysis and Online self test

Testability Techniques : Partitioning and ad hoc methods and Scan-path testing , Boundary scan and IEEE standard 1149.1 ,Offline built in Self Test (BIST), Hardware description languages and test

Testing of Analog and Digital circuits : Testing techniques for Filters, A/D Converters, RAM, Programmable logic devices and DSP

Text:

1. VLSI Testing: digital and mixed analogue digital techniques Stanley L. Hurst Pub: Inspec / IEE, 1999

Code No: ITV-612 **L** **C**
Subject: Low Power VLSI Design **3** **3**

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power

Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Power estimation

Simulation Power analysis:

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation.

Probabilistic power analysis:

Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Low Power Design

Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

Logic level:

Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Low power Architecture & Systems:

Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution : Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

Algorithm & architectural level methodologies : Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Text:

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002
2. Rabaey, Pedram, “Low power design methodologies” Kluwer Academic, 1997

References:

1. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000

Code No : ITV - 614	**L**	**C**
Subject: Cluster & Grid Computing	**3**	**3**

Cluster Computing:
Parallel systems,Cluster Architecture, Parallel Paradigms,Parallel, Programming with MPI, Resource management and scheduling

Grid Computing
Grids and Grid Technologies, Programming models and Parallelization Techniques, Standard application development tools and paradigms such as message-passing and parameter parallel programming,Grid Security Infrastructure, Data Management, Application Case Study: Molecular Modelling for Drug Design and Brain Activity Analysis, Resource management and scheduling, Setting up Grid, deployment of Grid software and tools, and application execution.

Text/References:

1. R. Buyya (editor), High Performance Cluster Computing , Vol1. and Vol.2, Prentice Hall, USA, 1999.
2. I. Foster and C. Kesselman (editors), The Grid : Blueprint for a New Computing Infrastructure , Morgan Kaufmann Publishers , 1999.
3. R. Buyya, "Economic-based Distributed Resource Management and Scheduling for Grid Computing, Ph.D. Thesis, Monash University, Melbourne, Australia, April 2002

Code No. ITV – 616	**L**	**C**
Subject: Embedded System Design	**3**	**3**

Introduction to an embedded systems design:
Introduction to Embedded system, Embedded System Project Management, ESD and Co-design issues in System development Process, Design cycle in the development phase for an embedded system, Use of target system or its emulator and In-circuit emulator, Use of software tools for development of an ES.

RTOS & its overview:
Real Time Operating System: Task and Task States, tasks and data, semaphores and shared Data Operating system Services-Message queues-Timer Function-Events-Memory Management, Interrupt Routines in an RTOS environment, basic design Using RTOS.

Microcontroller:
Role of processor selection in Embedded System (Microprocessor V/s Micro-controller), 8051 Microcontroller: Architecture, basic assembly language programming concepts, Instruction set, Addressing Modes, Logical Operation, Arithmetic Operations, Subroutine, Interrupt handling, Timing subroutines, Serial data transmission, Serial data communication

Embedded system development
Embedded system evolution trends. Round - Robin, robin with Interrupts, function-One-Scheduling Architecture, Algorithms. Introduction to-assembler-compiler-cross compilers and Integrated Development Environment (IDE). Object Oriented Interfacing, Recursion, Debugging strategies, Simulators.

Networks for Embedded Systems
The I^2C Bus, The CAN bus, SHARC link Ports, Ethernet, Myrinet, Internet, Introduction to Bluetooth: Specification, Core Protocol, Cable replacement protocol.
IEEE 1149.1 (JTAG) Testability: Boundary Scan Architecture

Text:
1. Embedded Systems by Raj Kamal, TMH
2. The 8051 Microcontroller by K.J. Ayala, Penram International
3. J B Peatman, Design with PIC Microcontrollers, Prentice Hall

References:
1. An Embedded Software Primer by David E. Simon, Pearson Education
2. Designing Embedded Hardware by John Catsoulis, O'reilly
3. Embedded System Design by Frank Vahid, Tony Givargis,", John Wiley & Sons, Inc
4. Building Embedded Linux Systems by Karim Yaghmour, O'reilly
5. Programming Embedded Systems by Michael Barr, O'reilly
6. Real-time systems & software by Alan C. Shaw, John Wiley & sons, Inc.

7. Computers as Components by Wayne Wolf, Harcourt India Pvt. Ltd.
8. Embedded System Design by Peter Marwedel, Kluwer Acadeemic Pub.
9. Programming and Customizing the AVR Microcontroller by Dhananjay Gadre, MGH
10. Fundamental of Embedded software by Daniel W. Lewis, PHI
11. Bluetooth Technology by CSR Prabhu & A.P. Reddi, PHI
12. John B Peat man " Design with Microcontroller ", Pearson education Asia, 1998
13. Burns, Alan and Wellings, Andy, " Real-Time Systems and Programming Languages", Second Edition. Harlow: Addison-Wesley-Longman, 1997
14. Raymond J.A. Bhur and Donald L.Bialey, " An Introduction to real time systems: Design to networking with C/C++ ", Prentice Hall Inc. New Jersey, 1999
15. Grehan Moore, and Cyliax, " Real time Programming: A guide to 32 Bit Embedded Development. Reading " Addison-Wesley-Longman, 1998
16. Heath, Steve, " Embedded Systems Design ", Newnes 1997

Code No.: ITV–618	**L**	**C**
Subject: DESIGNING WITH ASICS	**3**	**3**

Types of ASICs – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers.

ASIC Library design: Transistors as resistors – parasitic capacitance – logical effort programmable ASIC design software: Design system – logic synthesis – half gate ASIC.

Low level design entry: Schematic entry – low level design languages – PLA tools – EDIF – An overview of VHDL and verilog.

Logic synthesis in verilog and & VHDL simulation.

ASIC Construction – Floor planning & placement – Routing.

Text / References:

1. J.S. Smith, "Application specific Integrated Circuits", Addison Wesley, 1997.

Code No.: ITV – 620 **L** **C**
Subject: Real Time Systems and Software **3** **3**

Introduction, Real-time Versus Conventional Software, Computer Hardware for Monitoring and Control, Software Engineering Issues.

Process and State-based Systems model, Periodic and Sporadic Process, Cyclic Executives, CE definitions and Properties, Foreground-Background Organiazations, Standard OS and Concurrency – Architectures, Systems Objects and Object-Oriented Structures, Abstract Data Types, General Object Classes

Requirements and Design Specifications: Classification of Notations, Data Flow Diagrams, Tabular Languages, State Machine, Communicating Real Time State Machine- Basic features, Timeing and clocks, Sementics Tools and Extensions, Statecharts-Concepts and Graphical Syntax, Semantics and Tools

Declarative Specifications: Regular Expressions and Extensions, Traditional Logics-Propositional Logic, Predicates, Temporal logic, Real time Logic

Deterministic Scheduling : Assumptions and Candidate Algorithms, Basic RM and EDF Results, Process Interactions-Prority Inversiotn and Inheritance

Execution Time Prediction: Measurement of Software by software, Program Analysis with Timing Schema, Schema Concepts, Basic Blocks, Statements and Control, Schema Practice, Prediction by optimisation, System Interference and Architectural Complexities

Timer Application, Properities of Real and ideal clocks, Clock Servers – Lamport's Logical clocks, Monotonic Clock service, A software Clock server, Clock Synchronization- Centralized Synchronization, Distributed Synchronization

Programming Languages: Real Time Language Features, Ada-Core Language, Annex Mechanism for Real Time Programming, Ada and Software Fault Tolerance, Java and Real-time Externsions, CSP and Occam

Operating Systems: Real Time Functions and Sevices, OS Architectures-Real Time UNIX and POSIX, Issues in Task management- Processes and Threads, Scheduling, Synchronization and communication

Text Book:

1. Real – Time Systems and software by Alan C. Shaw ; John Wiley & Sons Inc

Code No : ITV - 622 **L** **C**
Subject : Neural Network **3** **3**

Introduction:
History, overview of biological Neuro-System, Mathematical Models of Neurons, ANN architecture, Learning rules, Learning Paradigms-Supervised, Unsupervised and reinforcement Learning.

Supervised Learning and Neurodynamics:
Perceptron training rules, Delta, Back propagation training algorithm, Hopfield Networks, Associative Memories.

Unsupervised and Hybrid Learning:
Principal Component Analysis, Self-organizing Feature Maps, ART networks, LVQ,

Applications for VLSI Design
Applications of Artificial Neural Networks to Function Approximation, Regression, Classification, Blind Source Separation, Time Series and Forecasting.

Text:

1. Anderson J.A., "An Introduction to Neural Networks", PHI, 1999.

Reference:

1. Haykin S., "Neural Networks-A Comprehensive Foundations", Prentice-Hall International, New Jersey, 1999.
2. Freeman J.A., D.M. Skapura, "Neural Networks: Algorithms, Applications and Programming Techniques", Addison-Wesley, Reading, Mass, (1992).
3. Golden R.M., "Mathematical Methods for Neural Network Analysis and Design", MIT Press, Cambridge, MA, 1996.
4. Cherkassky V., F. Kulier, "Learning from Data-Concepts, Theory and Methods", John Wiley, New York, 1998.
5. Anderson J.A., E. Rosenfield, "Neurocomputing: Foundatiions of Research, MIT Press, Cambridge, MA, 1988.
6. Kohonen T., "Self-Organizing Maps", 2nd Ed., Springer Verlag, Berlin, 1997.
   Patterson D.W., "Artificial Neural Networks: Theory and Applications", Prentice Hall, Singapore, 1995.
7. Vapnik V.N., "Estimation of Dependencies Based on Empirical Data", Springer Verlag, Berlin, 1982.

Code No : ITV - 624	**L**	**C**
Subject: Digital Logic with Verilog Design	**3**	**3**

Introduction to logic circuits: Variables and functions, Sysnthesis using AND, OR and NOT gates, Introduction to CAD tools, Introduction to Verilog

Implementation Technology: Transistor switches, CMOS Logic, PLD, Transmission gates

Optimized Implementation of Logic Functions: Strategy for minimization , minimzation of POS, Multiple Output circuits, Analysis of Multilevel Circuits

Number Representation and Arithmetic Circuits: Positional Number representation, Addition of unsigned numbers, signed Numbers, Fast adders, Design of arithmetic circuits using CAD tools, Multiplication

Combinational Circuit Building blocks: Multiplexers, Decoder, Encoder, Code Converters, Arithmetic Comparison circuits, Verilog for combinational circuits

Design of Sequential design, Design Asynchronous Sequential Design

Text:

1. Fundamental of digital Logic with Verilog design by S. Brown & Z. Vransesic, TMH.

Code No : ITV – 626	**L**	**C**
Subject: Microwave & Optoelectronic Devices	**3**	**3**

Microwave frequencies, microwave transistor, microwave field effect transistor, tunnel diode, backward diode, and MIS tunnel diode, Transferred electron devices-Gunn Diode

Avalanche Transit Time Devices: IMPATT Diode, BARRITT Diode, DOVETT Diode, and TRAPATT Diode

Microwave Integrated Circuit: Introduction, Circuit Forms, Transmission lines for MICs, Lumped Elements for MICs, Material for MICs: Substrate, Conductor, dielectric and resistive Materials, Fabrication techniques, Typical example of fabrication, Hybrid fabrication.

Microwave tubes: Klystron, Reflex Klystron and Magnetron, Traveling wave tubes, microwave detection diodes, application of microwave

Introduction of optoelectronic devices: Photovoltaic devices, Solar Radiation, PN-Homojunction solar cells, Antireflection coatings, Ideal conversion efficiency, Spectral response, I-V Characteristics, Temperature and radiation effects, Heterojunction solar cells, Schottky barrier solar cell, Thin film and amorphous silicon solar cell, Solar arrays

Display devices: Characterization of displays, drawbacks of cathode ray tube, Flat panel display: Electro luminescence displays (Powder and thin films), Plasma display, LCD, Electronchromic display and electrophoretic display

Text/References:

1. Physics of Semiconductor Devices by S M Sze, Willy Eastern Pub.
2. Microwave Devices and Circuits by S. Y. Liao, PHI
3. Microwave Engineering and application by O.P. Gandhi, Maxwell Macmillan Pub.
4. Topic in applied physics – Vol 40 by J.I. Pankove, Springer Verlag
5. Microelectronic Devices by E. S . Yang, MGH
6. Semiconductor Devices and Integrated Electronics by A. G. Milness, CBS Pub.
7. Optoelectronics : An introduction by J. Wilson & JFB Hawkers, PHI

Code No : ITV - 628	**L**	**C**
Subject: Project Work	**3**	**3**

The student will submit a synopsis at the beginning of the semester for the approval to the school project committee in a specified format. The student will have to present the progress of the work through seminars and progress report. A report must be submitted to the school for evaluation purpose at the end of the semester in a specified format.

Code No: ITV-652	**P**	**C**
Lab: Lab. – IV	**4**	**2**

The experiments will be based on the following papers:

1. Analog VLSI Design Lab
2. Elective - I

Code No: ITV-654	**P**	**C**
Lab: Lab. V	**4**	**2**

The experiments will be based on the following Papers:

1. Digital Signal Processing Lab
2. Elective - II

Code No: ITV-656*	**P**	**C**
Lab: Minor Project - I	**4**	**4**

The student will submit a synopsis at the beginning of the semester for the approval to the school project committee in a specified format. The student will have to present the progress of the work through seminars and progress report. A report must be submitted to the school for evaluation purpose at the end of the semester in a specified format

Code No: ITV-701	**L**	**C**
Subject: Algorithm for VLSI Design Automation	**3**	**3**

Logic synthesis & verification

Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

VLSI automation Algorithms:

Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

Placement, floor planning & pin assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor plannning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

Detailed routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

Over the cell routing & via minimization: two layers over the cell routers, constrained & unconstrained via minimization

Compaction: problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction

Text:

1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.

References:

1. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
2. Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition
3. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

Code No : ITV - 703	**L**	**C**
Subject: Process, Devices & Circuit Simulation	**3**	**3**

Introduction, Main data structure & program organization, Geometrical manipulations, Ion implantation, A novel measurement technique for 2D implanted ion distributions, Introduction to partial differential equation solver, the merged multi grid method, Isothermal device modeling & simulation, Non Isothermal device modeling & simulation, hydrodynamic device modeling & simulation

Text/References

1. Circuit, Device and Process Simulation: Mathematical and Numerical Aspects by Graham F. Carey (Editor), W. B. Richardson, C. S. Reed, B. Mulvaney, John Wiley & Sons; 1 edition.
2. Process and Device Simulation for MOS-VLSI Circuits, edited by P. Antognetti, D.A. Antoniadis , Robert W. Dutton, W.G. Oldham, kluwer Academic Publisher, 2000.

Code No : ITV - 705	**L**	**C**
Subject : Nano Technology	**3**	**3**

Introduction
Introduction to nanoscale systems, Length energy and time scales, Top down approach to Nano lithography, Spatial resolution of optical, deep ultraviolet, X-ray, electron beam and ion beam lithography, Single electron transistors, coulomb blockade effects in ultra small metallic tunnel junctions

Quantum Mechanics
Quantum confinement of electrons in semiconductor nano structures, Two dimensional confinement (Quantum wells), Band gap engineering, Epitaxy, Landaeur – Buttiker formalism for conduction in confined geometries, One dimensional confinement, Quantum point contacts, quantum dots and Bottom up approach, Introduction to quantum methods for information processing.

Molecular Techniques
Molecular Electronics, Chemical self assembly, carbon nano tubes, Self assembled mono layers, Electromechanical techniques, Applications in biological and chemical detection, Atomic scale charcterization techniques, scanning tunneling microscopy, atomic force microscopy

Text:
1. Beenaker and Van Houten "Quantum Transport in Semiconductor Nanostructures in Solid state Physics" Ehernreich and Turnbell, Academic press, 1991

References:

1. David Ferry " Transport in Nano structures" Cambridge University press 2000
2. Y. Imry " Introduction to Mesoscopic Physics, Oxford University press 1997
3. S. Dutta " Electron Transport in Mesoscopic systems" Cambridge University press 1995
4. H. Grabert and M. Devoret "Single charge Tunneling" Plenum press 1992

Code No : ITV - 707	**L**	**C**
Subject : Hardware-Software Co-design	**3**	**3**

Introduction :
Motivation hardware & software co-design, system design consideration, research scope & overviews

Hardware Software back ground:
Embedded systems, models of design representation, the virtual machine hierarchy, the performance3 modeling, Hardware Software development,

Hardware Software co-design research :
An informal view of co-design, Hardware Software tradeoffs, crosses fertilization, typical co-design process, co-design environments, limitation of existing approaches, ADEPT modeling environment.

Co-design concepts :
Functions, functional decomposition, virtual machines, Hardware Software partitioning, Hardware Software partitions, Hardware Software alterations, Hardware Software trade offs, co-design.

Methodology for co-design :
Amount of unification, general consideration & basic philosophies, a framework for co-design.

Unified representation for Hardware & Software : Benefits of unified representation, modeling concepts

An abstract Hardware & Software model :
Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model

Performance evaluation:
Application of t he abstract Hardware & Software model, examples of performance evaluation

Object oriented techniques in hardware design:
Motivation for object oriented technique, data types, modeling hardware components as classes, designing specialized components, data decomposition, Processor example.

Text

1. Sanjaya Kumar, James H. Ayler "The Co-design of Embedded Systems: A Unified Hardware Software Representation", Kluwer Academic Publisher, 2002

References

1. Gomaa, Software Design Methods for Concurrent and Real-time Systems, Addison-Wesley, 1993.
2. H. Kopetz, Real-time Systems, Kluwer, 1997.
3. R. Gupta, Co-synthesis of Hardware and Software for Embedded Systems, Kluwer 1995.
4. S. Allworth, Introduction to Real-time Software Design, Springer-Verlag, 1984.
5. C. M. Krishna, K. Shin, Real-time Systems, Mc-Graw Hill, 1997.
6. Peter Marwedel, G. Goosens, Code Generation for Embedded Processors, Kluwer Academic Publishers, 1995.
7. Additional reading from selected journal papers.

Code No: ITV - 709	**L**	**C**
Paper : Digital Image Processing	**3**	**3**

Introduction And Digital Image Fundamentals
Digital Image Representation, Fundamental Steps in Image Processing, Elements of Digital image processing systems, Sampling and quantization, some basic relationships like neighbours, connectivity, Distance measure between pixels, Imaging Geometry.

Image Transforms
Discrete Fourier Transform, Some properties of the two-dimensional fourier transform, Fast fourier transform, Inverse FFT.

Image Enhancement
Spatial domain methods, Frequency domain methods, Enhancement by point processing, Spatial filtering, Lowpass filtering, Highpass filtering, Homomorphic filtering, Colour Image Processing.

Image Restoration
Degradation model, Diagnolization of Circulant and Block-Circulant Matrices, Algebraic Approach to Restoration, Inverse filtering, Wiener filter, Constrained Least Square Restoration, Interactive Restoration, Restoration in Spatial Domain.

Image Compression
Coding, Interpixel and Psychovisual Redundancy, Image Compression models, Error free comparison, Lossy compression, Image compression standards.

Image Segmentation
Detection of Discontinuities, Edge linking and boundary detection, Thresholding, Region Oriented Segmentation, Motion based segmentation.

Representation and Description
Representation schemes like chain coding, Polygonal Approximatiion, Signatures, Boundary Segments, Skeleton of region, Boundary description, Regional descriptors, Morphology.

Recognition and Interpretation
Elements of Image Analysis, Pattern and Pattern Classes, Decision-Theoretic Methods, Structural Methods, Interpretatiion.

Text:

1. Rafael C. Conzalez & Richard E. Woods, “Digital Image Processing”, AWL.
2. A.K. Jain, “Fundamental of Digital Image Processing”, PHI.

Reference:

1. Rosefield Kak, “Digital Picture Processing”,
2. W.K. Pratt, “Digital Image Processing”,

Code No : ITV - 711 | **L** | **C**
Subject : Cryptology and Crypto chip Design | **3** | **3**

Code No : ITV - 711	**L**	**C**
Subject : Cryptology and Crypto chip Design	**3**	**3**

Basic concepts:
Information system reviewed, LAN, MAN, WAN, Information flow, Security mechanism in OS,, Targets: Hardware, Software, Data communication procedures
Threats to Security:
Physical security, Biometric systems, monitoring controls, Data security, systems, security, Computer System security, communication security.

Encryption Techniques:
Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management.
Message Authentication and Hash Algorithm:
Authentication requirements and functions secue Hash Algorithm, NDS message digest algorithm, digital signatures, Directory authentication service

Firewalls and Cyber laws:
Firewalls, Design Princples, Trusted systems, IT act and cyber laws, Virtual private network

Future Threats to Network:
Recent attacks on networks, Case study

Applications
AES algorithm. Crypto chip design: Implementation of DES, IDEA AES algorithm, Development of digital signature chip using RSA algorithm

Text:
1. William Stalling "Cryptography and Network Security" Pearson Education

References:

1. Charels P. Pfleeger "Security in Computing" Prentice Hall
2. Jeff Crume "Inside Internet Security" Addison Wesley

Code No : ITV - 713 **L** **C**
Subject: Genetic Algorithm & Programming **3** **3**

Basics of biological evolution: Darwin, DNA, etc. Basics of GAs: selection, recombination and mutation. Choices of algorithm: (mu,lambda), (mu+lambda), steady-state, CHC, etc. Linkage and epistasis. The standard test functions. Fitness and objective functions: scaling, windowing etc. Representational issues: binary, integer and real-valued encodings; permutation-based encodings.Operator issues: different types of crossover and mutation, of selection and replacement. Inversion and other operators.

Constraint satisfaction: penalty-function and other methods; repair and write-back; feasibility issues. Experimental issues: design and analysis of sets of experiments by t-tests, F-tests, bootstrap tests etc.Some theory: the schema theorem and its flaws; selection takeover times; optimal mutation rates; other approaches to providing a theoretical basis for studying GA issues.Rival methods: hill-climbing, simulated annealing, population-based incremental learning, tabu search, etc. Hybrid/memetic algorithms.

Multiple-solutions methods: crowding, niching; island and cellular models. Multi-objective methods: Pareto optimisation; dominance selection; VEGA; COMOGA.

Genetic programming: functions and terminals, S-expressions; parsimony; fitness issues; ADFs. Evolving rules and rule-sets. SAMUEL and related methods. Classifier systems: the Pittsburgh and Michigan approaches. Credit allocation: bucket-brigade and profit-sharing. Hierarchic classifier systems.

Genetic planning: evolving plans, evolving heuristics, evolving planners, optimising plans. Ant Colony Optimization: Basic method for the TSP, local search, application to bin packing.

Applications: engineering optimisation; scheduling and timetabling; data-mining; neural net design; etc. Some further ideas: co-evolution; evolvable hardware; multi-level GAs; polyploid GAs.

Text/References:

1. M. Mitchell: An Introduction to Genetic Algorithms. MIT Press, 1996.
2. W. Banzhaf, P. Nordin, R. E. Keller, F. D. Francone: Genetic Programming: An Introduction. Morgan Kaufmann, 1988.
3. E. Bonabeau, M. Dorigo, G. Theraulez: Swarm Intelligence: From Natural to Artificial Systems. Oxford University Press, 1999

Code No : ITV - 715	**L**	**C**
Subject : Bluetooth Technology	**3**	**3**

Introduction to wireless technologies: WAP services, Serial and Parallel Communication, Asynchronous and synchronous Communication, FDM,TDM, TFM, Spread spectrum technology

Introduction to Bluetooth: Specification, Core protocols, Cable replacement protocol

Bluetooth Radio: Type of Antenna, Antenna Parameters, Frequency hoping

Bluetooth Networking: Wireless networking, wireless network types, devices roles and states, adhoc network, scatternet

Connection establishement procedure, notable aspects of connection establishement, Mode of connection, Bluetooth security, Security architecture, Security level of services, Profile and usage model: Generic access profile (GAP), SDA, Serial port profile, Secondary bluetooth profile

Hardware: Bluetooth Implementation, Baseband overview, packet format, Transmission buffers, Protocol Implementation: Link Manager Protocol, Logical Link Control Adaptation Protocol, Host control Interface, Protocol Interaction with layers

Programming with Java: Java Programming, J2ME architecture, Javax.bluetooth package Interface, classes, exceptions, Javax.obex Package: interfaces, classes

Bluetooth services registration and search application, bluetooth client and server application.
Overview of IrDA, HomeRF, Wireless LANs, JINI

Text:

1. Bluetooth Technology by C.S.R. Prabhu and A.P. Reddi; PHI

Code No : ITV - 717	**L**	**C**
Subject : MEMS and IC Integration	**3**	**3**

Overview of CMOS process in IC fabrication, MEMS system-level design methodology, Equivalent Circuit representation of MEMS, signal-conditioning circuits, and sensor noise calculation.

Pressure sensors with embedded electronics(Analog/Mixed signal): Accelerometer with transducer,Gyroscope,RF MEMS switch with electronics,Bolo meter design.

RF MEMS, and Optical MEMS

Text/References:

1. Gregory T.A. Kovacs, Micromachined Transducers Sourecbook, The McGraw-Hill, Inc. 1998
2. Stephen D. Senturia, Microsystem Design, Kluar Publishers, 2001
3. Nadim Maluf, An Introduction to Microelectromechanical Systems Engineering, Artech House, 2000.
4. M.H. Bao, Micro Mechanical Transducers, Volume 8, Handbook of Sensors and Actuators, Elsevier, 2000.
5. Masood Tabib-Azar, Microactuators, Kluwer, 1998.
6. Ljubisa Ristic, Editor, Sensor Technology and Devices, Artech House, 1994
7. D. S. Ballantine, et. al., Acoustic Wave Sensors, Academic Press, 1997
8. H. J. De Los Santos, Introduction to Microelectromechanical (MEM) Microwave Systems, Artech, 1999.
9. James M.Gere and Stephen P. Timoshenko, Mechanics of Materials, 2nd Edition, Brooks/Cole Engineering Division, 1984

Code No : ITV - 719 **L** **C**
Subject : Computer aided VLSI Design **3** **3**

Code No : ITV - 719	**L**	**C**
Subject : Computer aided VLSI Design	**3**	**3**

Hardware description languages; Verifying behaviour prior to system construction simulation and logic verification; Logic Synthesis PLA based synthesis and multilevel logic synthesis; Logic optimization; Logic Simulation Compiled and event simulators; Relative advantages and disadvantages; Layout Algorithms Circuit partitioning, placement, and routing algorithms; Design rule verification; Circuit Compaction; Circuit extraction and post-layout simulation; Automatic Test Program Generation; Combinational testing D-Algorithm and PODEM algorithm; Scan-based testing of sequential circuits; Testability measures for circuits

Text / Reference:

1. “Algorithm and Data Structures for VLSI Design”, Christophn Meinel & Throsten Theobold
2. “Evolutionary Algorithm for VLSI”, Rolf Drechsheler

Code No : ITV -721 | **L** | **C**
Subject: Design of VLSI System | **3** | **3**

VLSI System Design methodology:
Structure Design, Strategy, Hierarchy, Regularity, Modularity, Locality. System on Chip Design options: Programmable logic and structures, Programmable interconnect, programmable gate arrays, Sea of gate and gate array design, standard cell design, full custom mask design.
Chip Design Methods :
Behavioral synthesis, RTL synthesis, Logic optimization and structural tools layout synthesis, layout synthesis, EDA Tools for System
DesignDesign capture tools:
HDL Design, Schematic Design, Layout Design, Floor planning and Chip Composition. Design Verification Tools: Simulation Timing Verifiers, Net List Comparison Layout Extraction, Design Rule Verification.
Data Path Sub System Design :
Introduction, Addition, Subtraction, Comparators, Counters, Boolean logical operations, coding, shifters, Multiplication, Parallel Prefix computations.
Array Subsystem Design
SRAM, Special purpose RAMs, DRAM, Read only memory, Content Addressable memory, Programmable logic arrays.
Control Unit Design :
Finite State Machine (FSM) Design, Control Logic Implementation: PLA control implementation, ROM control implementation.
Special purpose Subsystems
Packaging, power distribution, I/O, Clock, Transconductance amplifier, follower integrated circuits, etc.
Design Economics :
Nonrecurring and recurring engineering Costs, Fixed Costs, Schedule, Personpower, example
VLSI System Testing & Verification
Introduction, A walk through the Test Process, Reliability, Logic Verification Principles, Silicon Debug Principles, Manufacturing Test Principles, Design for Testability, Boundary Scan.
VLSI Applications
Case Study: RISC microcontroller, ATM Switch, etc.

Text:

1. Neil H.E. Weste, Davir Harris, "CMOS VLSI Design: A Circuits and system perspectives" Pearson Education 3rd Edition.

References:

1. Wayne, Walf, "Modern VLSI design: System on Silicon" Pearson Education, Second Edition
2. Pucknull, "Basic VLSI Design" PHI 3rd Edition

Code No : ITV -723 **L** **C**
Subject: Advanced Computational Methods **3** **3**

Solution of two or more nonlinear equations by iterative methods (Picard and Newton's methods) Spline interpolation, cubic splines, Chebyshev polynomials, Minimax approximation.

Eigenvalues and vectors of a real symmetric matrix – Jacobi method. Eigenvalue problem for ordinary differential equations.

Numerical solution of a parabolic equation. Explicit method, simple implicit method and Crank-Nicholson method. Stability.

Numerical Solution of elliptic problems. Dirichlet and Neumann problems (Cartesian and Polar coordinates)

Numerical solution of hyperbolic equations. Explicit method. Method of characteristics. Stability.

The finite element method – Ritz, collocation and Galerkin methods. Boundary value problems for ordinary differential equations. Shape functions. Assembly of element equations.

Text/References:

1. Smith G. D. "Numerical Solution of Partial Differential Equation", Oxford, 1965.
2. Chapra, S.C, Canale R P "Numerical Methods for Engineers" 3rd Ed., McGraw-Hill 1998.
3. Kreyszig, E, "Advanced Engineering Mathematics", John Wiley, 8th ed., 2002.
4. Gerald, C.F., "Applied Numerical Analysis", 6th Ed., Pearson, 1999.
5. Niyogi, P. "Numerical Analysis and Algorithms", TMH, 2003.
6. Conte, S.D. de Boor, C. "Elementary Numerical Analysis" McGraw-Hill.
7. Strang, G., Fix, G.J. "An Analysis of Finite Element Method" Prentice Hall, 1973.
8. Jain M. K. "Numerical Solution of Differential Equations" Wiley Eastern 1979.

Code No : ITV - 725	**L**	**C**
Subject: Project Work	**3**	**3**

The student will submit a synopsis at the beginning of the semester for the approval to the school project committee in a specified format. The student will have to present the progress of the work through seminars and progress report. A report must be submitted to the school for evaluation purpose at the end of the semester in a specified format.

Code No: ITV-751	**P**	**C**
Lab: Lab. – VI	**4**	**2**

The experiments will be based on the following paper:

1. Algorithm for VLSI Design Automation

Code No: ITV-753	**P**	**C**
Lab: Lab. VII	**4**	**2**

The experiments will be based on the following Papers:

1. Elective – I
2. Elective - II

Code No: ITV-755*	**P**	**C**
Lab: Seminar	**-**	**2**

Seminar will be based on Minor Project- II.

Code No: ITV-757	**P**	**C**
Lab: Minor Project - II	**4**	**8**

The student will submit a synopsis at the beginning of the semester for the approval to the school project committee in a specified format. The student will have to present the progress of the work through seminars and progress report. A report must be submitted to the school for evaluation purpose at the end of the semester in a specified format

Code No: ITV-752	**P**	**C**
Subject: Dissertation	**30**	**30**

The student will submit a synopsis at the beginning of the semester for the approval from the school project committee in a specified format. Synopsis must be submitted within a two weeks. The first defense, for the dissertation work, should be held with in a one month. Dissertation Report must be submitted in a specified format to the school for evaluation purpose.

Code No: ITV-754*	**P**	**C**
Subject: Seminar & Progress Report	**10**	**03**

The student will have to present the progress of the project work through seminars and progress reports at the interval of four weeks.

Code No: ITV-756*	**P**	**C**
Subject: Comprehensive Viva	**-**	**02**