Methods to Characterize Parasitic Inductance and Resistance of Modern VRM

ON Semiconductor®

APPLICATION NOTE

Abstract: for the purpose of modeling modern VRM, parasitics of VRM must be fully characterized. This paper presents experiment methods to characterize fast switching modern VRM. Results of parasitics, including inductance and resistance, of fast switching VRM are provided.

Introduction

Modern voltage regulator modules (VRM) for microprocessors have developed to a very high efficiency, very high current density and very high switching frequency level. MOSFETs for modern VRM have been advanced to very fast switching speed, 5 ns −10 ns. Fast switching, on one hand, requires extremely low MOSFET capacitances. On the other hand, switching of MOSFETs, including both turn−on and turn−off, are strongly affected by parasitic inductances of power switching loop and MOSFET gate driving loop, as well as parasitic gate resistance. Parasitic inductance of power switching loop partially determines maximum di/dt of switching loop. [1].

For fast switching VRM, trench MOSFETs gain its popularity due to its super high channel density [2], and therefore achieving very low RDSon with low cost. However, trench design incorporates a shield function to protect channel oxide from excessive drain voltage. This shield gate feature results in a parasitic shield resistance from drain to source, in series with output capacitance [3]. Usually this shield resistance of trench MOSFETs is unknown to users. In order to precisely predict performance of MOSFETs in high switching synchronous buck converter, shield resistance of MOSFETs must be characterized.

Some application issues, like shoot through [4], are dominated by parasitic inductances of application circuit, as well as parasitic capacitances of MOSFETs. In order to fully understand and control these application issues, parasitic inductances and resistance must be fully characterized.

NTMFD4C85 is one of the most recent developed trench MOSFETs for the application of fast switching VRM. A fast switching VRM with NTMFD4C85 as semiconductor switching component are fully characterized in this paper. Characterization results of parasitic inductances and resistances are included in this paper.

Overall, for modern VRM, there are there parasitic inductances that must be characterized:

1. Lumped high side gate inductance
2. Lumped low side gate inductance
3. Total switching loop inductance and its distributions in power switching loop

Besides parasitic inductances, there are four resistances that must be characterized. They are:

1. Lumped resistance in high side gate driving loop
2. Lumped resistance in low side gate driving loop
3. Lumped shield resistance of high side MOSFET
4. Lumped shield Resistance of low side MOSFET

Methodology to Characterize Parasitic Inductance and Resistance

A VRM is shown in Figure 1. For modern low voltage MOSFETs used in VRM, common source inductance between gate driving loop of high side MOSFET and power switching loop is minimized to zero. This feature can be identified in MOSFET datasheet.
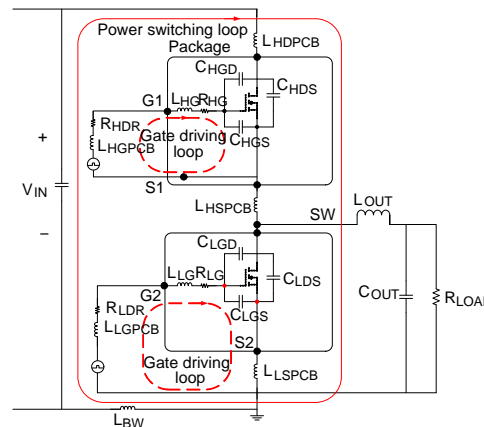

Figure 1. A VRM with Parasitics

The methodology to characterize inductance of gate driving loop and power switching loop is by characterizing ringing frequency of gate voltage first. Then calculate loop inductance based on ringing FREQUENCY of RLC circuit. This is a commonly used method to experimentally estimate ringing inductance.

The methodology to characterize resistance of gate driving loop is by creating a strong ringing in gate loop first, and then characterizes ringing inductance in gate driving loop based on ringing frequency. After that, characterize damping resistance based on damping profile of ringing waveforms. Shield resistance of MOSFETs is characterized in the same way.

This methodology characterizes parasitic inductance with relatively good accuracy. The method to characterize resistance is not as accurate as inductance. However, it provides a very reasonable result to start with.

Steps to Characterize Inductance in Gate Drive Loop

Steps to characterize resistance in gate driving loop are:

1. Turn−on gate driving circuit without turn on input power of VRM.
   Input power will cause interactions between gate circuit and power switching circuit, especially for the case of gate driver voltage is comparable with input voltage.
2. Measure gate voltage waveforms at the gate pin of MOSFET package.
   A certain amount of ringing can be observed in the gate voltage waveform. Usually gate resistance is around 2 Ω, which results in well damped gate resonance. Even though, it is obvious to identify the ringing frequency of gate circuit.
3. Calculate total gate inductance of driver loop by Equation 1.

$$L = \frac{\left(\frac{T_S}{2 \times \pi}\right)^2}{C} \qquad \text{(eq. 1)}$$

Here, "C" is the input capacitance of MOSFET, which is characterized in a standard tester in lab.

For modern VRM, the inductance in gate driving loop is typically around 10 nH to 20 nH, depending on PCB layout. Gate inductance higher than 20 nH could cause shoot through problem and harm system efficiency of synchronous buck converter.

Steps to Characterize Lumped Resistance in Gate Driving Loop

Steps to characterize lumped gate resistance in gate driving loop are:

1. Insert a wire between gate pin of MOSFET package and driving pin of MOSFET driver.
   By inserting a wire, gate inductance is significantly increased, so that strong ringing could be measured at gate pin of package. The resistance of the inserted wire must be far less than parasitic gate resistance, which is typically 1−5Ω.
2. Measure voltage waveforms at both terminals of the inserted wire.
   The difference between waveforms at both terminals of inserted wire is the inductance voltage in a RLC resonance circuit.
3. Calculate total resonance inductance of driver loop by Equation 1.
4. Fitting the outline of ringing waveform of the inserted wire.
   The outline of resonant voltage of inductor is expressed by Equation 2.

$$V = A \times e^{\frac{R}{2L}t} \qquad \text{(eq. 2)}$$

Here, two parameters, A and R/2L, need to be characterized by fitting curve profile. Theoretically, value of "A" is proportional to inductance of inserted wire to total parasitic inductance of the gate driving loop. The theoretical equation for A is expressed by Equation 3.

$$A = \frac{L_{WIRE}}{L_{LOOP}} \times V_{DR} \qquad \text{(eq. 3)}$$

Here, V_{DR} is driver voltage of MOSFET.

In curve fitting, both "A" and "R/2L" can be determined.

For a regular MOSFET driver, current sourcing resistance and current sinking resistance are different, which leads to the turn−on damping resistance is different from turn−off damping resistance. Both resistances can be characterized through the procedures 1 to 4.

Steps to Characterize Parasitic Inductance of Power Switching Loop

Inductance of Power Switching loop is characterized though the similar process in the previous section. Basically, by characterizing the frequency of phase node ringing, loop inductance could be calculated.

The power switching loop is a high frequency loop. For modern VRM, di/dt and dv/dt could be as high as 12V(A)/ns, the test ground of such a high frequency circuit must be as close to high frequency ground as possible, which is the ground terminal of input capacitors.

Characterize Total Inductance of Power Switching Loop:

Steps to characterize lumped parasitic inductance of power switching loop are:

1. Turn−on gate driving circuit and input power
   let the whole circuit working in the conditions in which characterization is performed.
2. Measure voltage waveforms of drain pin of low side MOSFET package
3. Calculate total resonance inductance of driver loop by Equation 1.

Characterize Inductance Distribution of Power Switching Loop

Why are distributions of switching loop inductance so important? Some part of switching loop inductance, called common source inductance, is shared by gate driving loop and power switching loop, are extremely important for switching characteristics. Common source inductance not only slows down switching speed of MOSFET, but also causes ringing in gate loop, which as a result may cause shoot though in some situations.

For MOSFETs in modern VRM, common source inductance is minimized to zero by using a separate gate driving pin. However, for low side MOSFET, it is rare to design separate driving pin due to ZV switching nature of low side MOSFET. PCB trace inductance at source side of

low side MOSFET might be coupled into driver loop. Due to these reasons, it is very important to characterize parasitic inductance distributions in power switching loop.

Steps to characterize parasitic inductance distribution of power switching loop inductance are:

1. Turn−on MOSFET driver and input power let VRM working in the conditions in which characterization is performed.
2. Measure voltage waveforms of interested points in power switching loop.
   There are several points that must be measured.
   a. The first is ground terminal of input capacitances, which is also high frequency ground.
   b. The second is the ground of driver, which detects where gate driving circuit is connected in power switching loop.
   c. The third is the source pin of low side MOSFET, which is to measuring common source inductance of low side MOSFET.
   d. The fourth is phase node.
   e. The fifth is the driving pin of high side MOSFET.
   f. The sixth is the drain pin of high side MOSFET.
   g. The seventh is the high voltage terminal of input capacitance.
3. Calculate the ringing voltage of parasitic inductance of each loop segment by subtracting waveforms at its both terminals.
4. Parasitic inductance of each segment is proportional to the ringing amplitude of each section. The parasitic loop inductance in power switching loop is distributed to each segment by the ratio of ringing amplitude.

Here, the ground of probe must be the high frequency ground during test. Other grounding points would introduce noise and error in measured waveforms [5].

Characterize Lumped Shield Resistance of MOSFETs

Steps to Characterized shield resistance of MOSFETs are:

1. Turn−on MOSFET driver and input power.
   Let the circuit working in the conditions in which characterization is performed.
2. Measure waveforms at source pin of low side MOSFET package.
3. Calculate total damping resistance of switching loop by Equations 2 and 3, which is the shield resistance of MOSFET.

Damping resistance usually varies by design. For trench MOSFET technology, there is a gate shield design, which causes shield resistance. Shield resistance behaves like RC snubber with output capacitances. Damping resistance of low voltage MOSFET is quite high, usually 1 Ω. For other design, like LDMOSFET, shield resistance is not designed. In this case, damping resistance of MOSFET is usually small, about 0.1 Ω or less.

Characterize Modular Board with NTMFS4C85N

A board with dual MOSFET NTMFD4C85 (30 V) is characterized. The pin connection of NTMFD4C85 is shown in Figure 2. Obviously, the pin 2 of NTMFD4C85 is the pin decoupling power switching current and driving current of high side MOSFET. Pin 2 is closely contacted with source of high side MOSFET inside package. Capacitances of NTMFD4C85 [6] are shown in Table 1.
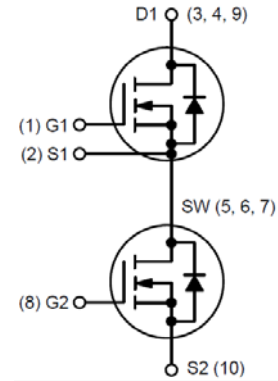

Figure 2. Circuit Diagram of NTMFD4C85

Table 1. CAPACITANCES OF NTMFD4C85

	Parameters	Value
High side MOSFET	Ciss at VDS = 0 V, VGS = 0 V	2 nF
	Coss at VDS = 12 V, VGS = 0 V	1.4 nF
Low side MOSFET	Ciss at VDS = 0 V, VGS = 0 V	6.6 nF
	Coss at VDS = 12 V, VGS = 0 V	4.3 nF

Gate Inductance Characterization

Follow steps through 1 through 3 in the section describing how to characterize inductance in the gate driving loop, the gate waveform recorded and shown in Figure 3.
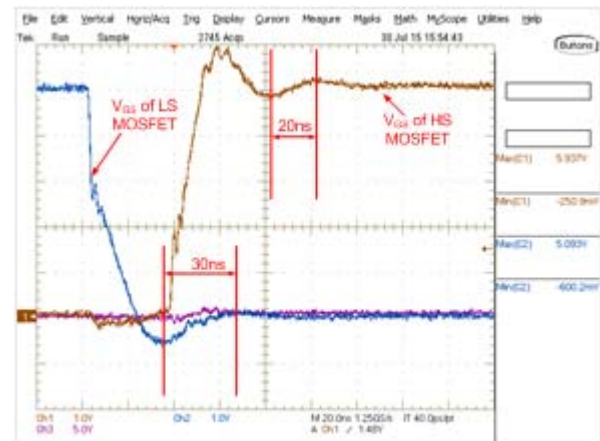

Figure 3. Turn−off and Turn−on Gate Waveforms of Low Side and High Side MOSFET

From Figure 3, it can be measured that ringing period is 40 ns for high side and 60 ns for low side. As it is measured in datasheet, Input capacitance Ciss for high side MOSFET at Vin = 0 V and VGS = 0 V is 2 nF, which gives high side gate resonance inductance 20.265 nH based on Equation 1. Input capacitance of low side is 6.6 nH in datasheet at the experiment conditions, which gives gate inductance of 13.8 nH for low side MOSFET based on Equation 1.

Total Resistance in Gate Driving Loop

Gate resistance is characterized by fitting ringing profile. In the case of not enough ringing, an external inductance is inserted in the circuit. Usually, parasitic inductance of a copper wire is big enough to be inserted in gate driving loop.

Follow steps 1 through 4 in the section describing how to characterize lumped resistance in the gate driving loop, the gate ringing waveforms of high side MOSFET are captured, shown in Figure 4.
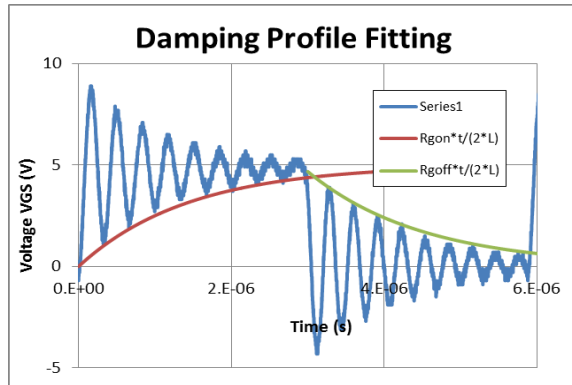
Figure 4. Gate Ringing Waveforms of High Side MOSFET

The ringing period when VGS = 5 V is 312 ns. Based on Equation 1, ringing inductance is calculated to be 1297 nH. Based on Equation 2, by fitting damping profile of the ringing, the damping resistance is calculated to be 1.6 Ω, which is the total turn−on resistance of MOSFET gate driving loop, which include resistance in MOSFET driver, resistance in MOSFET package, and external agate resistance designed by users.
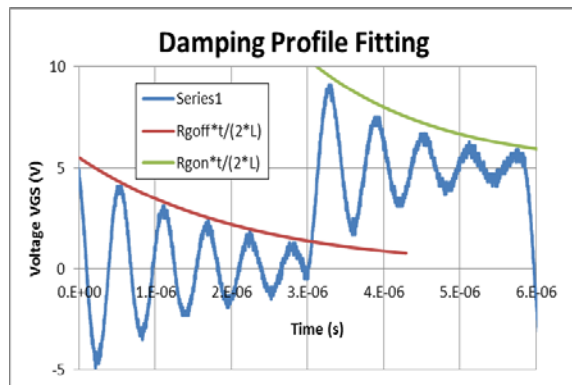
Figure 5. Gate Ringing Waveforms of Low Side MOSFET

The ringing period when VGS = 0 V is 320 ns. Follow the same steps, the total resistance in gate driving loop for MOSFET turn−off is calculated to be 1.8 Ω.

Here, pay attention to the fact that the total turn−on gate resistance is different from total turn−off gate resistance. The main difference comes from the driver, in which current sourcing resistance is different from current sink resistance.

The gate ringing waveforms of low side MOSFET is shown in Figure 5. In the same way, the total gate resistance of low side MOSFET is characterized to be 1.4 Ω for turn−on and 1.1 Ω for turn−off.

Power Switching Loop Inductance

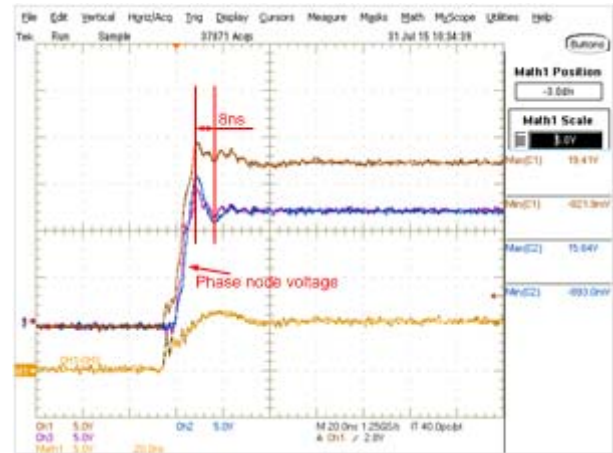**Switching Loop Inductance Characterization**

Figure 6. Waveform of Phase Node

Phase node waveform of characterization board is shown in Figure 6. From Figure 6, the phase node ringing period is measured 16 ns. Based on Coss of low die MOSFET, which is shown in Table 1, switching loop inductance is calculated to be 1.51 nH.

Inductance Distribution of Switching Loop

The inductance distribution of power switching loop is a key for understanding performance of VRM during switching intervals. For switching loop, seven interested points are measured, as shown in Figures 7 and 8. These seven points are:

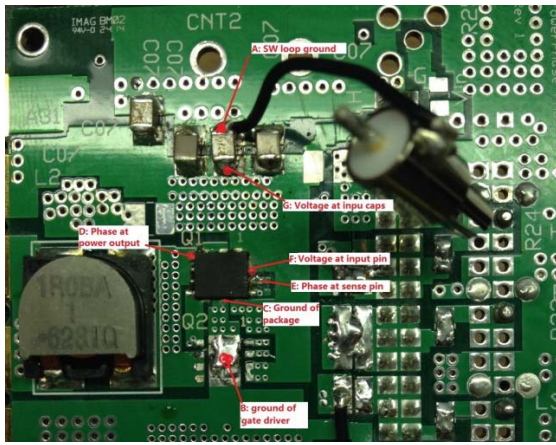|	
Point A	Ground of input capacitors
Point B	Ground of MOSFET driver
Point C	Ground of MOSFET package
Point D	Phase node pin of package at output inductance terminal
Point E	Phase node pin for gate driving of high side MOSFET
Point F	Input voltage pin at the drain pin of high side MOSFET
Point G	Input voltage terminal of input capacitors

Figure 7. Interested Points of Evaluation Board

Subtracting waveforms of two interested points gives voltage WAVEFORM on parasitic inductance between the two interested points. The parasitic inductance value of each segment is proportional to ringing voltage amplitude at the same time interval, as shown in Figure 9.
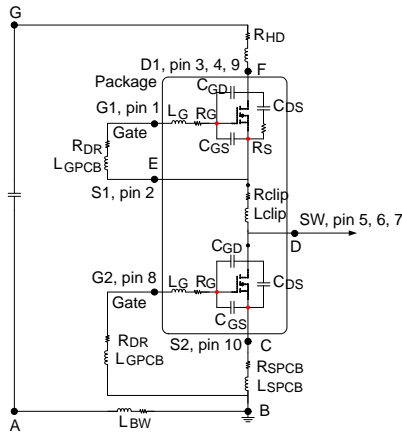

Figure 8. Interested Points in Circuit Schematic

Pay attention to that high side inductance and low side inductance have opposite di/dt, which make measured voltage on high side branch have peaks, while for low side branch inductance voltage have valleys.

Based on measurements in Figure 9, at the same time interval, marked as green box, $|B-A| = 1.75$ V, $|C-B| = 1.75$ V, $|E-D| = 1$ V, $|F-E| = 0$ V, $|G-F| = 1$ V. Based on this ratio, the inductance from input capacitance (point G) to drain pin of high side MOSFET (point F) is 1.51 nH x 1 / (1.75 + 1.75 + 1 + 1) = 0.27 nH, which is equivalent to the inductance from source of high side MOSFET (point E) to drain of low side MOSFFET (point D). The parasitic inductance from source of low side MOSFET (point C) to ground of low side driver (point B) is 1.51 nH x 1.75 / (1.75 + 1.75 + 1 + 1) = 0.45 nH, which is the same with inductance from ground of low side driver (point B) to source of input capacitance (point A).

Here, pay attention to that there no inductance between point C and D due to output capacitance of low side MOSFET dominates this section.

Shield Resistance of MOSFETs

Follow steps 1 and 2 in the section to characterize lumped shield resistance of MOSFETs, waveforms at ground pin of package (point C) is shown in Figure 10.
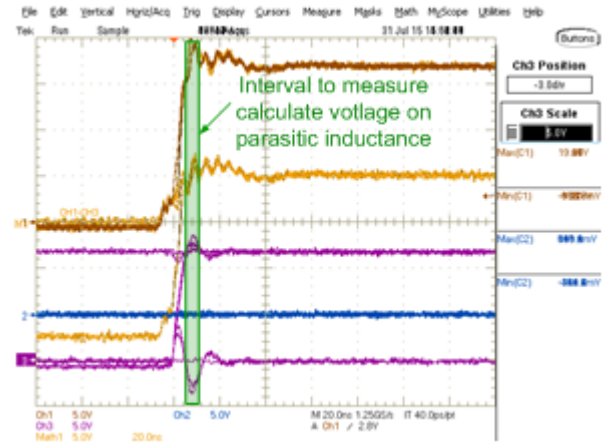
Figure 9. Voltage Waveforms at Interested Points of Evaluation Board

In Figure 10, the interval from 0s to 3e−7s is high side on; the interval from 3e−7s to 5e−7s is the interval of low side on. When high side is on, shield resistance of low side MOSFET is the damping resistance; when low side is on, the shield resistance of high side MOSFET is the damping resistance.
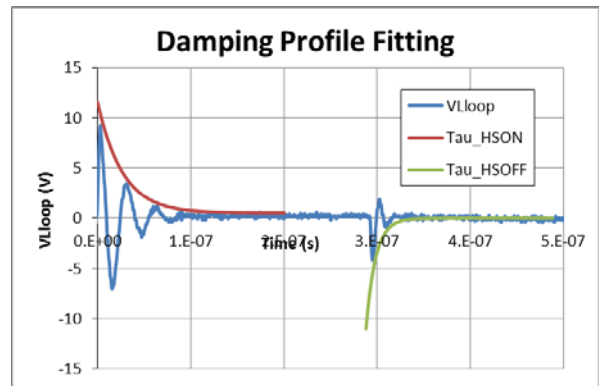

Figure 10. Voltage Waveform at Ground Pin of Package

In Figure 10, the ringing period when high side is on is 28.2 ns. Based on Equation 1, ringing inductance is calculated to be 4.685 nH. By fitting the ringing profile with Equation 2, damping resistance of switching loop is calculated to be 0.35 Ω, which is the shield resistance of low side MOSFET.

When low side is on, ringing period of voltage at ground pin is 14 ns. In the same way with the case of high side is on, damping resistance is switching loop is 0.7 Ω, which is the shield resistance of high side MOSFET.

Of course, shield resistance only exists in trench MOSFET. In the case of no shield feature is designed in MOSFET, damping resistance mostly come from gate resistance. In this case, no shield resistance needs to be characterized.

Table 2. CHARACTERIZATION RESULTS OF VRM WITH NTMFD4C85

Parameters	Value	
High side MOSFET	Rg(tot)(Turn−on)	1.6 Ω
	Rg(tot)(Turn−off)	1.8 Ω
	Lg(tot)	20.265 nH
	Rshield	0.7 Ω
Low side MOSFET	Rg(tot)(Turn−on)	1.4 Ω
	Rg(tot)(Turn−off)	1.1 Ω
	Lg(tot)	13.8 nH
	Rshield	0.35 Ω
Switching loop inductance	Loop(tot)	1.51 nH
	B−A	0.47 nH
	C−B	0.47 nH
	E−D	0.27 nH
	F−E	0 nH
	G−F	0.27 nH

Final circuit with all parasitics characterized is shown in Figure 11, which is the starting point for circuit simulation of VRM.
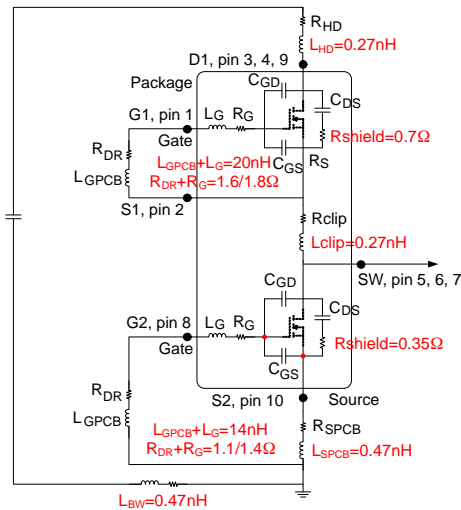
Figure 11. Circuit with All Parasitics Characterized

Comments about this circuit:

For modern VRM, the layout of power switching loop is optimized to very low parasitic loop inductance, typically 1−2 nH. For such a low loop inductance, di/dt and dv/dt are so high that they could reach 12V(A)/ns. On one hand, such a high di/dt and dv/dt means extremely fast switching speed and therefore high efficiency for VRM. On the other hand, it causes significant overstress on MOSFET and high risk of shoot through. Un−optimized circuit layout could easily cause these application issues and reduces efficiency of VRM.

Due to the discrete configuration of MOSFET driver and MOSFETs, parasitic inductance of gate driving CIRCUIT is relatively high, typically 10 nH to 20 nH. Such a high inductance require high gate resistance to achieve critical damping condition for gate driving circuit, which means gate resistance should be around 1−2 Ω typically. This high gate resistance limits gate driving speed, which of course will limit efficiency of VRM. To overcome this problem, MOSFETs in industry tend to integrate driver with MOSFET in one package, will significantly reduce parasitic inductance of gate driving loop. This integration is the trend of MOSFETs for modern VRM.

Conclusions

Method to characterize parasitic inductances and resistances of modern VRM is presented in this application note. Following the method in this application note, a VRM with advanced low voltage MOSFET NTMFD4C85N is characterized. Circuit features of modern VRM are revealed to be extremely low switching loop inductance, but high gate inductance for both high side and low side MOSFETs, which limits minimum gate resistance and switching loss of MOSFET. This shield resistance is revealed to be a well suited snubber for phase node ringing.

REFERENCES

1. An inductive−switching loss model accounting for source inductance and switching loop inductance, Zhiyang Chen Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty−Ninth Annual IEEE Page(s): 497 – 504

2. Performance Analysis of Trench Power MOSFETs in High−Frequency Synchronous Buck Converter Applications, Xiong Yali, Cheng Xu, Wang Xiangcheng, Kumar Pavan, Guo Lina, Z. John Shen, International Journal of Power Management Electronics 01/2008;

3. Internal self−damping optimization in trench power FETs for high−frequency conversion, Roig, J. ; Tong, C.−F. ; Bauwens, F. ; Gillon, R. ; Massie, H. ; Hoggatt, C. Applied Power Electronics Conference and Exposition (APEC), 2014

4. Characterization of Cdv/dt Induced Power Loss in Synchronous Buck DC−DC Converters, Qun Zhao and Goran Stojcic, APEC 2004

5. Accurate Performance Predictions of Power MOSFETs in High Switching Frequency Synchronous Buck converters for VRM, Loìpez, T., Elferich, R., Power Electronics Specialists Conference, IEEE, 15−19 June 2008, pp 1566 – 1572

6. Datasheet: http://www.onsemi.com/pub_link/Collateral/NTM FD4C85N−D.PDF

PUBLICATION ORDERING INFORMATION