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Investigation of electrical properties of In/$ZnIn_2Te_4$/n-Si/Ag diode

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Abstract. In/$ZnIn_2Te_4$/n-Si/Ag diode structure was fabricated by the thermal deposition of a $ZnIn_2Te_4$ thin film on n-Si wafer substrate with Ag metal back contact. The structural characteristics of the film were investigated in terms of composition, X-ray diffraction and topographic measurements. The diode structure was completed by evaporating In metal on the film surface as a top contact. The diode parameters as saturation current, barrier height, ideality factor and series resistance values were determined from the semi-logarithmic forward bias current–voltage characteristics of the diode. According to the assumption of the thermionic emission model, the ideality factor was found higher than unity and it was also observed that the barrier height and ideality factor showed a temperature-dependent profile resulting from the non-ideality in the current–voltage behaviour of the diode. As a result, the model was modified by considering inhomogeneous barrier formation and Gaussian distribution was expected to be dominant on 1.37 eV mean barrier height with a deviation of 0.18. In addition, the voltage dependence of these Gaussian diode parameters was investigated. The forward and reverse bias capacitance and conductance measurements showed that there was a slight change in capacitance values with frequency whereas the conductance values decreased with increase in frequency. In addition to the current–voltage analysis, the distribution of density of interface states and the values of series resistance were evaluated as a function of bias voltage and frequency.

Keywords. Thin film; thermal evaporation; thermionic emission.

1. Introduction

Among II–VI group of compounds, the structure of zinc telluride (ZnTe) has been a focus of interest as an attractive material for a variety of electronic applications [1–3]. It is a direct band gap material with a high absorption coefficient and therefore, it has attracted attention as a highly suitable material for the fabrication of optoelectronic devices such as green light emitting diodes [4], electro-optic broadband detector [5] and it is also used in the generation of broadband mid-infrared radiation [6]. In photovoltaic applications, to obtain higher efficiency, ZnTe thin film buffer layers are used in CdTe-based diodes [7] and since it is a wide band gap material, it can be used as a window film layer in tandem solar cells [2]. On the other hand, due to high resistive behaviour, in recent years, the dopants from group-I (Ag, Cu) and group-III (Al, Ga and In) have been used to tune its electronic properties [8–10]. In this case, there are several studies on its ternary analogous as $ZnIn_2Te_4$ (ZIT) introducing In to this binary compound of ZnTe [11–17]. It is a ternary alloy which belongs to $A^{II}B_2^{III}C_4^{VI}$ chalcopyrite family where A = Zn, Cd, Hg; B = In, Ga; C = Se, S, Te [13,18,19]. In recent years, many studies have reported growing interest in this group of compounds due to their potential device applications. In the literature, there are several studies on material characteristics of $CuInTe_2$, $AgInTe_2$, $CdIn_2Te_4$, $HgIn_2Te_4$ and also $ZnIn_2Te_4$ [20–26]. However, this type of investigation would primarily require a rigorous study of Si-based heterojunction. Based on similar studies on ZnTe–Si diode [2,27], the present paper reports one such attempt of preparation and characterization of the In/ZIT/Si/Ag diode.

With very little information about the properties of ZIT, it is known that it crystallizes into a structure belonging to the tetragonal space group S_4^2 with lattice parameters $a = 6.1$ Å and $c = 12.6$ Å and it can be classified as an ideal chalcopyrite structure with the ratio of these lattice parameters, $c \sim 2a$ [14,16]. Being a defective chalcopyrite type structure, most of the studies have been focussed on the material properties, especially optical behaviour and electronic band structure. In addition to these studies, with optimizing the material characteristics of the layers, it can be used in electronic applications. The performance of the fabricated devices mostly depends on the formation of barrier, parasitic resistance effects on the current flow and also a possible interface layer and the distribution of the interface states at the junction. Therefore, a detailed analysis of the diode structure extracting its main diode parameters is essential to understand the current conduction process.

In this work, ZIT thin films were deposited by using its elemental evaporation sources in an optimized stacked layer

sequence. It is a simple and low cost thin film deposition method common to achieve the desired stoichiometry in films with control on each layer deposition and therefore, contributes to the final structure. Towards the aim of investigating the electrical characteristics of the In/ZIT/Si/Ag heterostructure, film layer was deposited on n-Si wafer substrate with Ag back contact. To the best of our knowledge, In/ZIT/Si/Ag diode has not been reported yet and in the present work, experimental current–voltage (I–V) behaviour of the diode is detailed with extracting barrier parameters, and approximated to the pre-dominant conduction mechanism on the current flow through the junction under the effect of change in temperature. Additionally, capacitance and conductance profiles depending on bias voltage and frequency were investigated to discuss the possible interfacial state and series resistance effects in the diode.

2. Experimental

The ZIT thin films were prepared by using a physical vapour deposition system having four furnace type effusion cells. For the thin film deposition process, the desired ternary compound was grown using a multi-stage process involving the sequential evaporation of elemental Zn, In and Te sources. The layer thickness optimization of each evaporation source was carried out by conducting several deposition cycles to be sure about the sequential growth parameters of each layer. Firstly, the growth of each element was carried out separately. Evaporation source power and growth rate were adjusted by measuring the thickness of each growth after deposition. Then, the final parameters were obtained by comparing the thicknesses of *in-situ* quartz crystal reading and actual thickness reading using a Dektak 6 M profilometer. During the deposition, the substrate temperature was kept constant at about 200°C. To obtain the stoichiometric compound, the source fluxes were adjusted using the temperature control of the effusion cells to maintain constant evaporation rates during the deposition of the optimized stacked sequence of the layers, following the order of Te/In/Zn with a top Te-film layer. Therefore, the study given in this paper includes the results of the typical samples within the analyses carried out on the several different deposited samples. The result of energy dispersive X-ray spectroscopy (EDS) analysis at 10 kV for the ZIT layer is presented as an inset in figure 1a. The presented spectrum showed that the film layer was composed of the constituent elements and the atomic percentages obtained from the quantitative analysis of this spectrum were in stoichiometry and no trace of any impurity atoms was detected.

In this work, about 500 nm ZIT thin film layers were deposited on a 600 μm thick, (111) oriented n-type (P-doped) crystalline Si wafer with the resistivity value of 1–10 (Ω cm). Before the film deposition, the complete back side of the Si wafer substrate was thermally coated with Ag metal to form an ohmic contact and then subsequent annealing treatment was performed at 450°C under the nitrogen atmosphere to enhance the contact formation on the substrate surface. Stoichiometry of the atomic composition of the deposited film layer was verified by a Zeiss HD15 model scanning electron microscope equipped with an EDS system. Additionally, X-ray diffraction (XRD) measurements were carried out by a benchtop Rigaku Miniflex XRD analyzer with 1.54 Å CuKα radiation. The surface morphology of the thin films was studied by atomic force microscopy (AFM) using a Veeco Multimode V system. To complete the diode, the front surface of the obtained ZIT/Si/Ag was deposited with a 200 nm In top contact layer through a shadow mask in a circular dot contact shape of 0.2 mm diameter by a thermal evaporation method. After this deposition, the complete structure was annealed at 100°C under a nitrogen atmosphere to improve the adhesion of the top metal contact on the ZIT film surface. The electrical characteristics of the In/ZIT/Si/Ag heterostructure were analysed by temperature-dependent current–voltage (I–V) and frequency-dependent capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements. The I–V measurements were carried out by using a Keithley 2401 sourcemeter as a source/measure unit and CTI-cryogenics model 22 refrigerator system combined with a model SC helium compressor to scan the diode temperature from 220 to 360 K with the help of a Lakeshore DRC-91C controller. In addition, C–V and G/ω–V measurements were performed by using a Hewlett Packard 4192A LF model impedance analyzer under room temperature conditions.

3. Results and discussion

The XRD pattern of the film revealed the polycrystalline nature of the tetragonal structure along with the (112) main orientation direction (figure 1a). The high intensity reflection was obtained at a major peak $2\theta \cong 25°$ indicating the preferred orientation and the second characteristics peak indexed as (220) at about $2\theta \cong 42°$ was also observed in the diffraction profile [15,17]. Except for these characteristic peaks, there were no other extra diffraction peaks in the XRD pattern coming from the formation of additional mixture of crystalline phases different than the expected ternary structure. AFM measurements were used to construct the topographic profile of the film surface. With several measurements, the homogeneity of the surface was confirmed with uniform and nearly smooth characteristics as shown in figure 1b.

To characterize the electrical properties of the fabricated ZIT/Si diode prepared with Ag back and In front metal contacts, the temperature-dependent I–V measurements were carried out in the temperature interval of 220–360 K. As shown in figure 2, the fabricated structure demonstrates a good rectifying behaviour indicating a typical Schottky diode over a wide range of ambient temperature. In an ideal case, the current flow mechanism through a diode usually follows

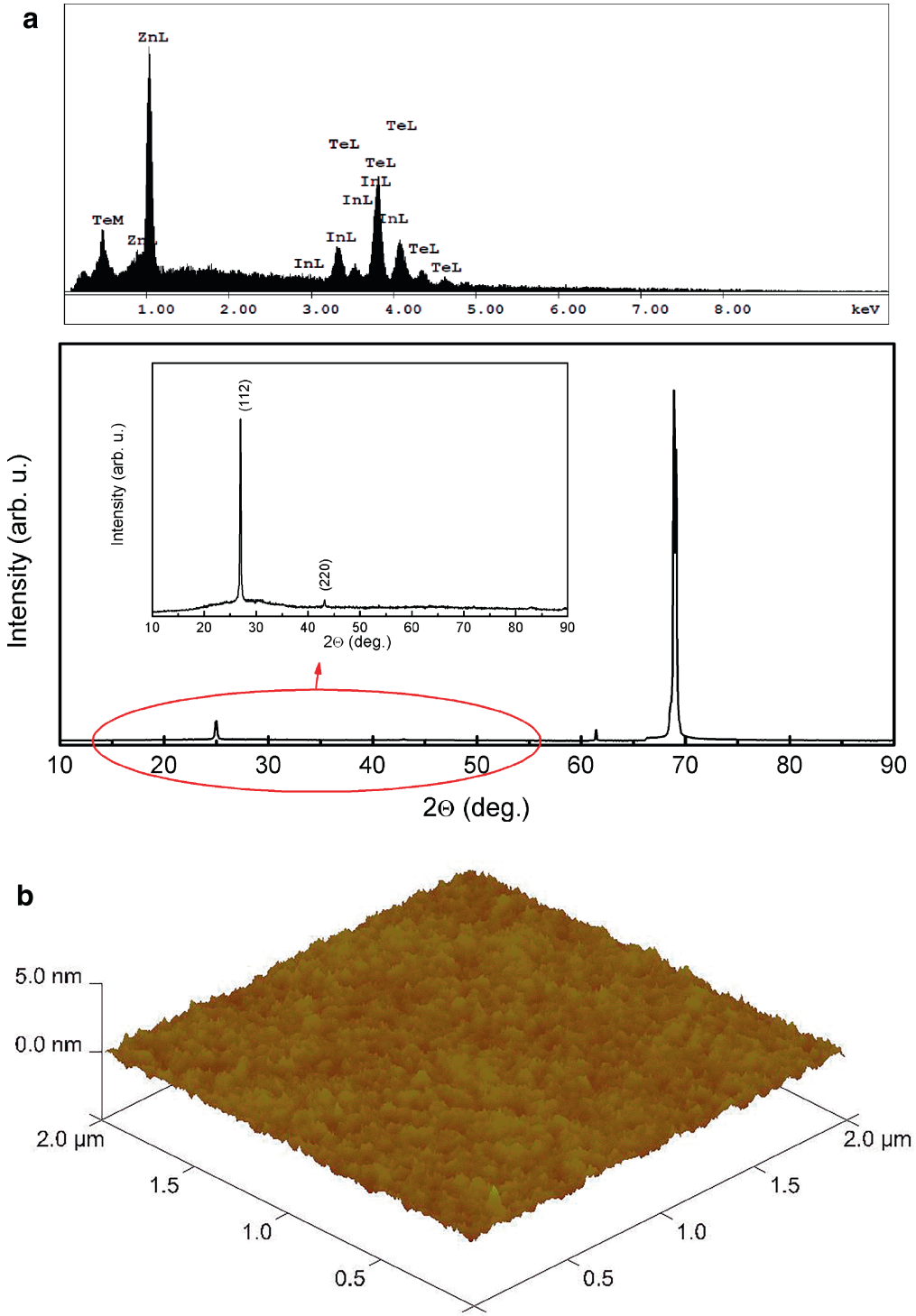

Figure 1. (**a**) XRD profile for the crystalline structure and (**b**) three-dimensional surface image for the morphological analyses of the film layer.

the model proposed with a thermionic emission (TE) mechanism [28]. According to this approach, the forward current in an exponential behaviour related to the bias voltage is assumed as the conduction that can occur mainly due to TE of majority carriers in the diode with carrier diffusion. This relation between forward bias voltage (V) and resulting current (I) flow in the diode can be approximated with the voltage-independent barrier height and ideality factor, to

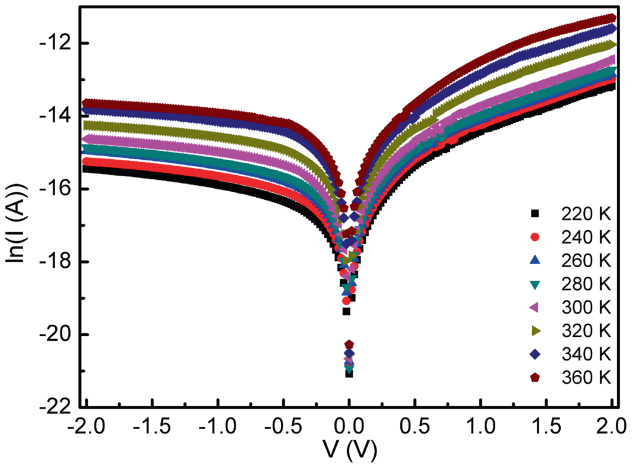

Figure 2. Semi-logarithmic plots of forward and reverse bias current–voltage characteristics of the diode at different ambient temperatures.

obtain an insight into the diode behaviour and the electrical parameters as:

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right], \tag{1}$$

where I_0 is the reverse saturation current at zero-bias, q the electronic charge, k the Boltzmann constant, T the applied diode temperature in Kelvin and n the dimensionless ideality factor that determines the deviation from pure TE approximation. Since it was derived from the assumption that the barrier height is much larger than temperature term, this expression was used in the case of the current through the junction at a forward bias $V \geq 3kT$ to neglect the reverse current contribution [28]. In addition, since it is based on the pure TE approximation with unity n, a possibility of the deviation from this model is usually added with the term n in which the variation from the unity can be attributed to the contribution of the other conduction mechanisms to the carrier transport in the junction region and the presence of the interfacial states. From the experimental I–V data, I_0 values were found as a result of the straight line fitting process of semi-logarithmic forward bias I–V plot at zero-voltage (table 1) and its temperature dependence can be expressed by,

$$I_0 = AA^*T^2\exp\left(\frac{-q\Phi_{B0}}{kT}\right) \tag{2}$$

where A is the effective diode area, A^* the effective Richardson constant and Φ_{B0} the zero-bias barrier height. Following this analysis, the temperature-dependent Φ_{B0} values were calculated by using equation (2) with the expected A^* value for effective semiconducting layer at each T region. The experimental values of Φ_{B0} were found in increasing the behaviour in the range from 0.53 to 0.88 with increase in T as given in table 1.

From I–V relationship of an ideal diode structure, n generally has a value in the interval of 1 and 2 depending on whether diffusion or recombination current dominates the current flow [28–30]. However, practically, it can help to evaluate the ideality of the fabricated diode structure and also examine the possible current transport mechanism in this diode structure by applying the $I-V$ relation given in equation (1). The values of n were obtained from the slope of the linear region in $\ln I-V$ (figure 2) plot depending on applied T as,

$$n = \frac{q}{kT}\left(\frac{\mathrm{d}V}{\mathrm{d}\ln(I)}\right), \tag{3}$$

and the results are listed in table 1. In the experimental case, n is expected to be in a value greater than unity due to the effect of series resistance R_s, possible interfacial thin native oxide layer, and non-uniformity in the barrier with a wide distribution of barrier patches [31]. As listed in table 1, the values of Φ_{B0} and n were found in strong temperature behaviour and with decrease in T, the observations on the decrease in Φ_{B0} and increase in n values can be the indication of a particular distribution of interface states and native insulator layer in the junction region [31–33]. According to the results of the I–V analysis, the conduction mechanism operating in this

Table 1. Calculated electrical parameters of the diode by using TE model.

Temperature (T in K)	Saturation current (I_0 in A)	Barrier height (Φ_{B0} in eV)	Ideality factor (n)	Series resistance (R_s in Ω)
360	1.12×10^{-7}	0.88	2.96	12.9
340	7.26×10^{-8}	0.84	3.12	13.1
320	4.63×10^{-8}	0.80	3.27	14.5
300	2.77×10^{-8}	0.76	3.46	16.6
280	1.55×10^{-8}	0.72	3.70	20.8
260	1.25×10^{-8}	0.67	3.95	22.6
240	6.11×10^{-9}	0.62	4.28	23.8
220	3.29×10^{-9}	0.56	4.64	27.4

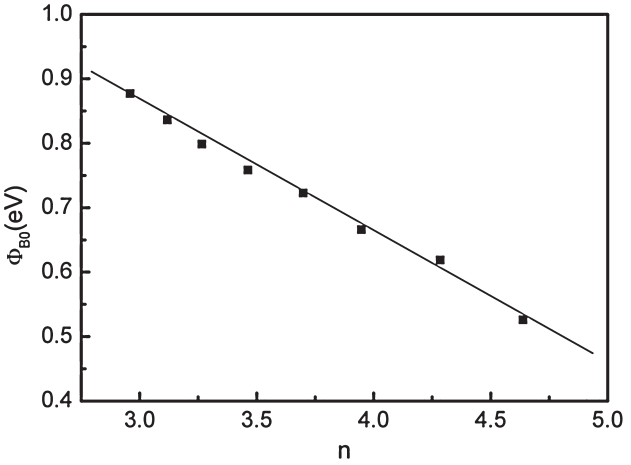

Figure 3. Relation between zero-bias barrier height and ideality factor of the diode at each working temperature step.

structure could be predominated by TE; however, due to the high values of n, it can also be attributed to the inhomogeneity in the barrier with the existence of low barrier patches [34,35]. In the high T region, increase in T can provide sufficient energy to the carriers to overcome the barrier height which also takes higher values depending on T. On the other hand, at low T region, carriers cannot gain sufficient energy from T, and therefore, the carriers can pass through the low barrier distributed in the junction at lower temperatures.

Additionally, apart from the ideal case, due to the experimental nature, the parasitic resistances can cause the voltage drop and affect the performance of the diode. It is noted that the diode parameters were calculated using TE from the low bias region, in which the I–V relation is linear without the resistance effect. These values can be determined at the higher bias voltage region where they reach a saturation value for each temperature step [36]. Therefore, in the downward curvature of the forward bias region, the values of R_s were calculated by parasitic resistance analysis as proposed by Cheung and Cheung [37]. In fact, the effects of these resistances can be observed in the output characteristics of the diode in which it mainly occurs due to the resistance of the diode material and metallic contact and it is responsible for the ohmic loss in the diode [28,38]. The obtained values as a function of temperature are listed in table 1, and the experimental analysis shows that these values decrease with increasing T as a consequence of an increase in the number or density of the free charge carriers, either by bond breaking or by the de-trapping mechanism [35]. As a linear relationship between Φ_{B0} and n was observed, it was used to investigate the degree of barrier height variation under the consideration of Tung's model [39]. As shown in figure 3, the analysis of the straight line of the plot Φ_{B0} *vs.* n at $n = 1$ gave the value for a laterally homogeneous barrier height around 1.20 eV. As a result, the decrease of Φ_{B0} and increase of n especially at lower temperatures can be explained by the possible causes depending on the inhomogeneity in barrier height and distribution of interface state density (D_{it}) [40].

Although the dominant mechanism was approximated to be a TE model, the obtained abnormal I–V characteristic of the diode can be modelled by considering the fluctuations due to the barrier inhomogeneity and suggesting Gaussian distribution (GD) in barrier height with a mean barrier height $\bar{\Phi}_{B0}$ and standard deviation σ_0 [29,32,33,35]. Based on this approach, the total current flow through the barrier at forward bias voltage can be re-written with the modified barrier expression as,

$$I = AA^*T^2\exp\left[\left(-\frac{qV}{kT}\right)\left(\bar{\Phi}_{B0} - \frac{q\sigma_0^2}{2kT}\right)\right] \times\exp\left(\frac{qV}{n_{ap}kT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right], \quad (4)$$

with modified reverse saturation current expression as

$$I_0 = AA^*T^2\exp\left(-\frac{q\Phi_{ap}}{kT}\right), \quad (5)$$

where Φ_{ap} and n_{ap} are the apparent barrier height and apparent ideality factor, respectively. According to this model, the inhomogeneous barrier height formation in the diode can be expressed as:

$$\Phi_{ap} = \bar{\Phi}_{B0} - \frac{q\sigma_0^2}{2kT}, \quad (6)$$

and in this relation σ_0 indicates the deviation from the homogeneity of barrier height in the diode. To examine the barrier height as a Gaussian function, the relation between Φ_{B0} and $q/2kT$ is plotted as shown in figure 4a, and it is expected to be in a straight line behaviour. As shown in figure 4a, the parameters of the GD in barrier height, $\bar{\Phi}_{B0}$ and σ_0 were found from the intercept and the slope of this plot as 1.37 eV and 0.18, respectively. As a result of this analysis, the deviation from the mean is about 13% and since σ_0 is not small compared to the mean value, can be the indication of effect of an interfacial layer with inhomogeneities having a single GD of barrier height in the diode [35,41]. As expressed in equation (4), the voltage effect in n values can be formulated by the bias-dependent Gaussian coefficients as,

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT}, \quad (7)$$

where n_{ap} is a voltage-independent parameter. In this case, both the Gaussian parameters are assumed to be bias-dependent in which ρ_2 and ρ_3 are the bias voltage coefficients of $\bar{\Phi}_{B0}$ and σ_0, respectively. Additionally, these coefficients can be used to discuss the voltage deformation of the barrier height distribution in the diode. The observed linear relation found in the $\left(n^{-1} - 1\right)$ *vs.* $q/2kT$ plot (figure 4b) presents the

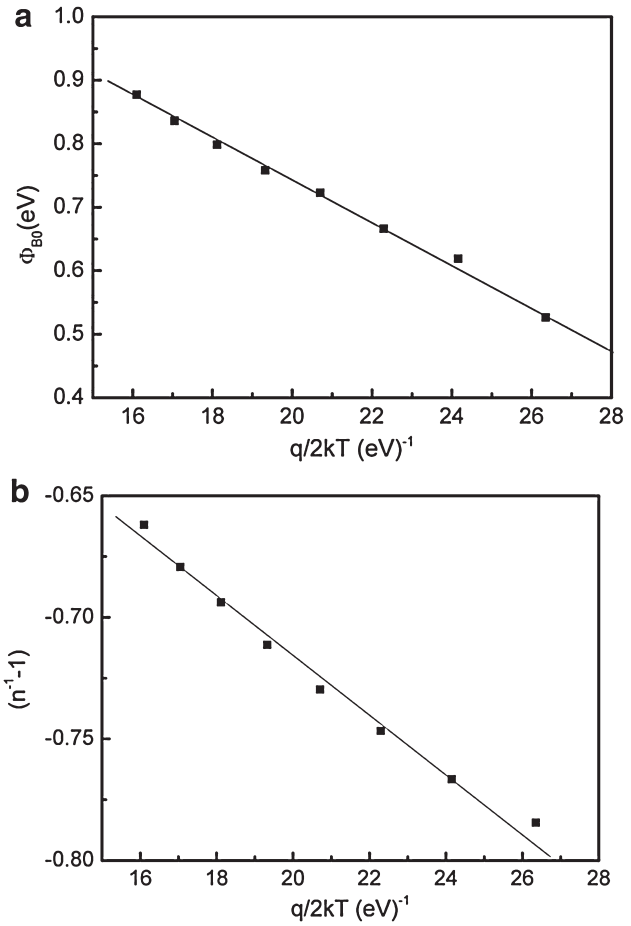

Figure 4. The variation in (**a**) zero-bias apparent barrier height and (**b**) ideality factor of the diode with inverse temperature at different ambient temperatures.

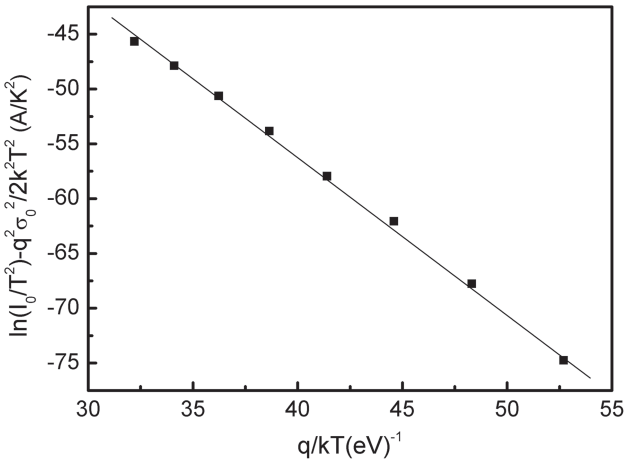

Figure 5. Richardson plot of the $\ln(I_0/T^2) - (q^2\sigma_0^2)/(2k^2T^2)$ *vs.* q/kT for the diode.

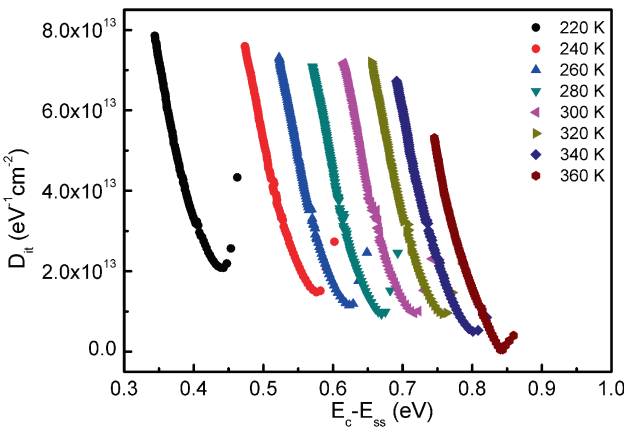

Figure 6. The energy distribution of the interface states obtained from the forward bias current–voltage characteristics of the diode at different ambient temperatures.

temperature dependence of n, and from the slope and intercept of the fitting process ρ_2 and ρ_3 were determined as 0.0119 and -0.4767, respectively.

Mainly as a result of high T dependence of n, the conventional Richardson plot is not expected to be in a straight line [42]. Although the main parameters were assumed by using TE model (equation (1)), due to the observed variations in Φ_{B0} and n with T, in accordance with the assumed model related to the barrier inhomogeneity, A^* can be approximated from the modified current relation given in equation (4) as,

$$\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_0^2}{2k^2T^2}\right) = \ln\left(AA^*\right) - \frac{q\bar{\Phi}_{B0}}{KT}. \tag{8}$$

As a result of the linear relation found in the modified activation energy plot (figure 5) [43], $\bar{\Phi}$ and modified A^* values were approximated as about 1.38 eV and 117.9 A cm^{-2} K^{-2} in close agreement with the expected values from the analysis of equation (4) and the literature studies [28,32]. Thus, the compatible values found in the analysis of A^* can be the indication of the achievement in TE theory with GD of inhomogeneous barrier height to explain the transport mechanism in the fabricated diode structure.

As mentioned in the analysis of the possible transport mechanism, the higher value of n can be attributed to the deviation from TE model. With the assumption of the inhomogeneous barrier formation in the diode, it can be due to the nature of interfacial layer, distribution of interface traps and their restructuring and reordering depending on the temperature variations [41,44]. Considering the Card and Rhoderick's model, the density distribution curves of the interface state $D_{\rm it}$ in equilibrium with the semiconductor can be determined from the forward bias I–V characteristics at each T [45]. The distribution profiles of the calculated $D_{\rm it}$ values as a function the energy of interface states with respect to the conduction band, $E_{\rm c} - E_{\rm ss}$ are shown in figure 6 for each T. As shown in this figure, the values of $D_{\rm it}$ take lower values with increasing temperature under the effect of localized trap levels [46].

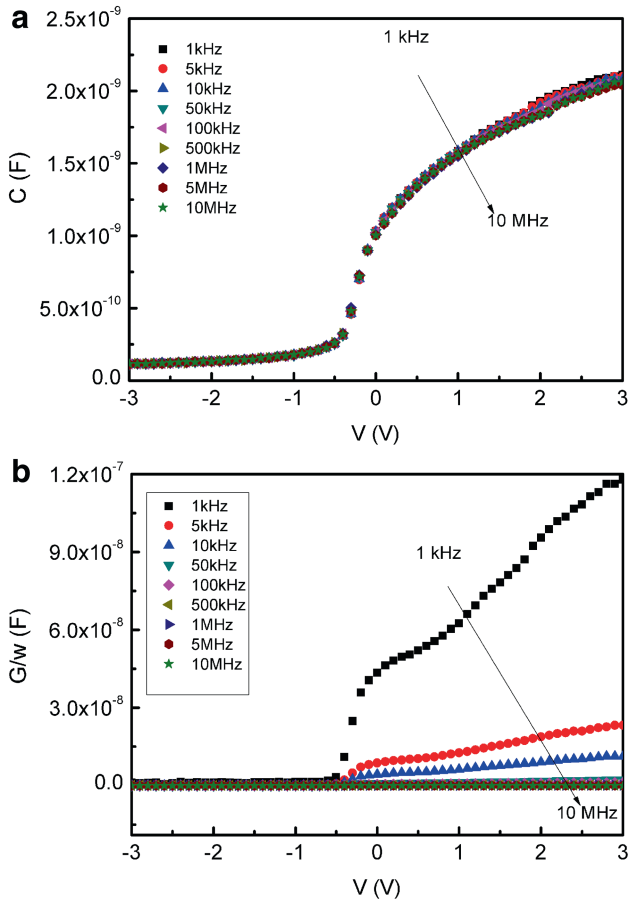

Figure 7. Forward and reverse biases: (**a**) capacitance–voltage and (**b**) conductance–voltage plots of the diode at room temperature.

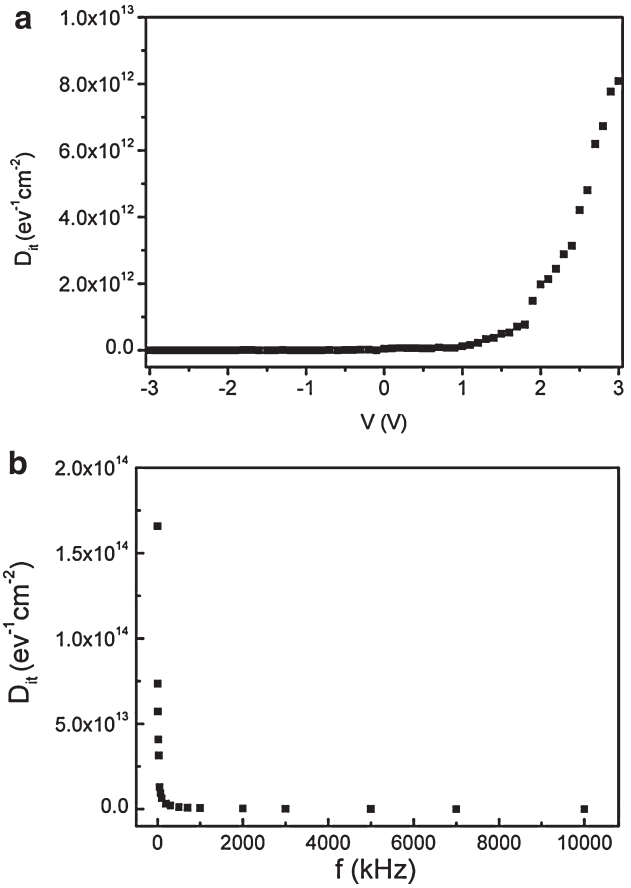

Figure 8. Density of interface state profiles obtained by (**a**) high–low frequency capacitance and (**b**) Hill–Coleman models.

In the case of electrical measurements, the capacitance–voltage (C–V) and conductance–voltage (G/ω–V) profiles of the diode as a function of applied frequency at room T are shown in figure 7. As given in these figures, these values demonstrate variation as a function of the bias voltage, and although there is a slight response in the $C-V$ behaviour to the change in the frequency, $G/\omega-V$ values increases with decrease in frequency. With the frequency dispersion observed in $G/\omega-V$ values, it can be concluded that the effect of series resistance is not small enough to be neglected and that it becomes effective as compared to the interface states due to low impedance of the diode. Additionally, these capacitive and conductive behaviours may be different at the frequency spectra, depending on the relaxation time of interface states and the frequency of the ac signal [47]. The capacitive effect of the interface states was observed at lower frequencies in which they can follow the applied AC signal. On the other hand, at sufficiently high frequencies, these values reach a constant value as the indication of ineffective behaviour of the interface states does not contribute to the total diode capacitance [28]. In addition to the analysis from I–V data, the distribution of D_{it} can be evaluated by using both high–low frequency capacitances ($C_{HF}-C_{LF}$) and Hill–Coleman methods as a reason of these observed fluctuations [48–51].

According to the $C_{HF}-C_{LF}$ model, the interfacial layer capacitance is assumed to be in a series connection with the capacitance of the interface states and the space charge capacitance. Thus, the effect of D_{it} on the capacitance behaviour (C_{it}) can be described as,

$$C_{it} = \left[\frac{1}{C_{LF}} - \frac{1}{C_i}\right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_i}\right]^{-1}, \tag{9}$$

where C_{HF} and C_{LF} are the highest and lowest capacitance values measured, and C_i is the capacitance of the interfacial layer [48–50]. As illustrated in figure 8a, D_{it} values calculated by applying $C_{HF}-C_{LF}$ model, increase with increase in bias voltage and its distribution profile can be the indication of the continuum or bands of interfacial states [32,52]. In addition to these voltage-dependent D_{it} values, frequency-dependent profile was investigated by Hill–Coleman method as,

$$C_{it} = \frac{(G_m/\omega)_{max}}{\left((G_m/\omega)_{max}/C_i\right)^2 + (1 - C_m/C_i)^2}, \tag{10}$$

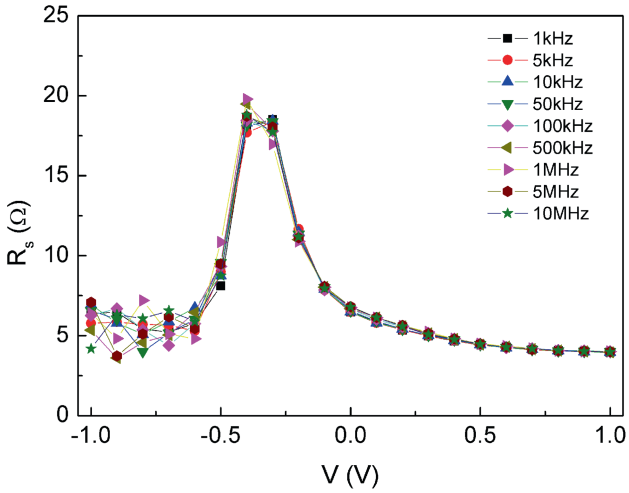

Figure 9. Frequency dependence of series resistance of the diode derived from the frequency-dependent room temperature capacitance and conductance measurements.

where C_m and G_m are the experimental (measured) capacitance and conductance values, respectively [51]. As a result of this analysis, D_{it} values were found in exponentially decreasing behaviour with increase in the applied frequency as a consequence of response of these states to the variation in frequency. Moreover, in the strong accumulation region, at the high frequency values, the frequency dependence of R_s is discussed from the admittance characteristics of the diode from the following relation [53],

$$R_s = \frac{G_m}{(G_m)^2 + (\omega C_m)^2}. \quad (11)$$

On the contrary to the parasitic resistance calculation at the saturation region, this expression gives the values for all bias voltages. From this analysis, the obtained values are given in figure 9 as a function of frequency, and these experimental values of R_s are slightly depending on frequency could be attributed to the insulator layer and the distribution D_{it} [54].

4. Conclusions

The polycrystalline ZIT thin film was uniformly deposited on n-Si and the obtained In/ZIT/Si/Ag diode structure was characterized in terms of temperature-dependent I–V and frequency-dependent C–V and G/ω–V measurements. Φ_{B0} and n were derived from the prediction on ideal TE model and in addition to the high n values from the unity, these values were found in temperature-dependent characteristics. As a result of this abnormal forward bias I–V behaviour, the current conduction mechanism was modelled by TE, considering GD distribution in the barrier height. This modification was attributed to the presence of the interfacial layer at the junction interface, a distribution of the patches with inhomogeneity in the barrier, the R_s effect. Therefore, including the assumption with Gaussian function, the parameters were found to be in good agreement with the literature. The distribution profile of D_{it} obtained from I–V measurements showed a decreasing behaviour with increase in T and the experimental values were found to be in good agreement with C–V analysis. It was observed that the variation in the applied frequency slightly affects the capacitance values and the higher values at low frequencies can be the indication of the effects of the interface states.

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